Deadline 6 月 18 号

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备注团队名称和人员

研究内容：

通过 matlab 建模或者 cadence（MOS 管级/verilogA 级，工艺不限）构建一个时钟交织 Pipelined-SAR ADC，pipelined 级数不限，时钟校准通道数≥4 条，精度≥12 位，TI-ADC 总采样率≥2GS/s，自己手动添加以下误差和失配，例如采样时钟 jitter 范围 100fs~5ps，timing skew 范围 200fs~5ps, inter-stage gain error±10%等（以上参数仅供参考），通过静态分析方法和动态分析方法分析：TI mismatch (gain mismatch, offset mismatch and timing skew), pipelined-SAR ADC 级间增益误差（inter-stage gain error），第一级 SAR ADC 电容失配（capacitor-DAC mismatch），比较器失调，时钟 jitter 等的影响。选择一种 time skew 校准方法进行 timing skew 误差检测并分析。建模、仿真验证、撰写完整分析报告，在 cadence 里面完成仿真验证的有额外 bonus 分数。

分析方法：

静态特性分析：转移特性曲线/统计方法；动态特性分析：FFT

Tips：ISSCC 等论文很多有 slides，讲的比 conference paper 更详细

部分 Timing skew 校准方法参考文献（不限于以下方法）：

[1] B. Razavi, “Design considerations for interleaved ADCs,” IEEE J. SolidState Circuits, vol. 48, no. 8, pp. 1806–1817, Aug. 2013.
[2] H. Wei, P. Zhang, B. D. Sahoo, and B. Razavi, “An 8 bit 4 GS/s 120 mW CMOS ADC,” IEEE J. Solid-State Circuits, vol. 49, no. 8, pp. 1751–1761, Aug. 2014.
[3] M. El-Chammas and B. Murmann, “A 12-GS/s 81-mW 5-bit timeinterleaved flash ADC with background timing skew calibration,” IEEE J. Solid-State Circuits, vol. 46, no. 4, pp. 838–847, Apr. 2011.
[4] J. Song, K. Ragab, X. Tang, and N. Sun, “A 10-b 800-MS/s timeinterleaved SAR ADC with

fast variance-based timing-skew calibration,”IEEE J. Solid-State Circuits, vol. 52, no. 10, pp. 2563–2575, Oct. 2017.
[5] N. Le Dortz et al., “22.5 A 1.62GS/s time-interleaved SAR ADC with digital background mismatch calibration achieving interleaving spurs below 70dBFS,” in Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC), Feb. 2014, pp. 386–388
[6] L. Luo, S. Chen, M. Zhou, and T. Ye, “A 0.014 mm2 10-bit 2GS/s timeinterleaved SAR ADC with low-complexity background timing skew calibration,” in Proc. Symp. VLSI Circuits, Jun. 2017, pp. C278–C279.
[7] C.-Y. Lin, Y.-H. Wei, and T.-C. Lee, “A 10-bit 2.6-GS/s time-interleaved SAR ADC with a digital-mixing timing-skew calibration technique,”IEEE J. Solid-State Circuits, vol. 53, no. 5, pp. 1508–1517, May 2018.
[8] M. Gu, Y. Tao, X. He, Y. Zhong, L. Jie and N. Sun, "A 1-GS/s 11-b Time-Interleaved SAR ADC With Robust, Fast, and Accurate Autocorrelation-Based Background Timing-Skew Calibration," in IEEE Journal of Solid-State Circuits, vol. 60, no. 2, pp. 421-431, Feb. 2025, doi: 10.1109/JSSC.2024.3421363.
[9] Y. Cao, M. Zhang, Y. Zhu, R. P. Martins and C. -H. Chan, "A 12-GS/s 12-b 4× Time-Interleaved ADC Using Input-Independent Timing Skew Calibration With Global Dither Injection and Linearized Input Buffer," in IEEE Journal of Solid-State Circuits, vol. 59, no. 12, pp. 4211-4224, Dec. 2024