Enclustra User Schematics

Mercury XU8 Revision 2.1

Disclaimer

User schematics do not include proprietary Enclustra design elements, such as power supply circuits.
These circuits use optimized designs which are extremely compact and remain proprietary to Enclustra.
The user manual provides all necessary information to use the module and its interfaces.

User schematics are provided after purchase of Enclustra hardware, and may also be provided in certain cases before purchase, to assist in product evaluation.
No part of the schematics may be copied or modified without written permission from Enclustra.

Full schematics, including a full bill-of-materials, may be available through the purchase of a hardware licence for the product in question.
Please contact Enclustra Sales for more information.

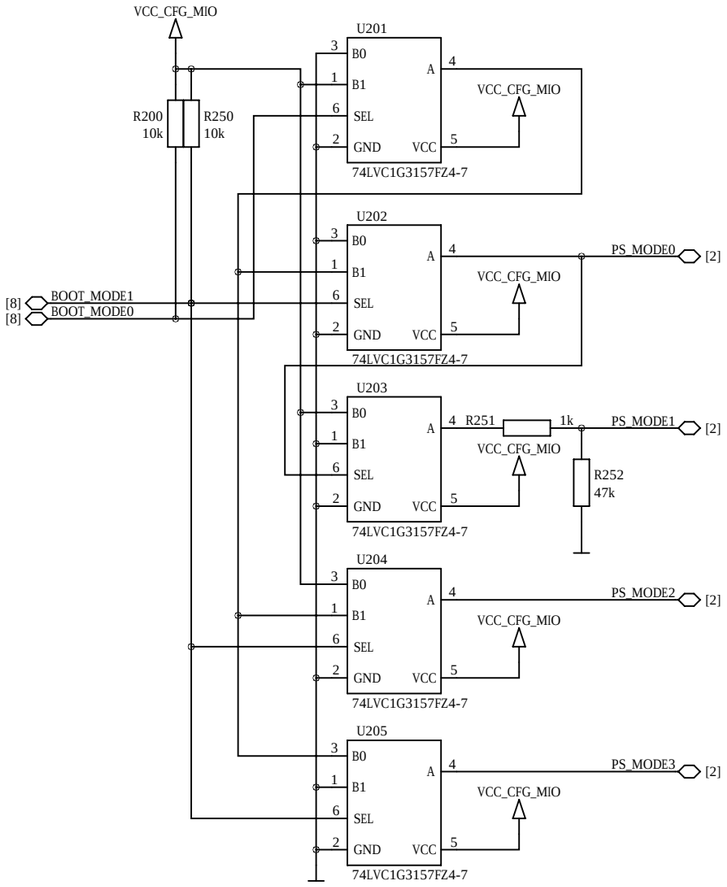
Note: DNE = Do Not Equip (parts not equipped by default)

Mercury+ XU8 SoC Module

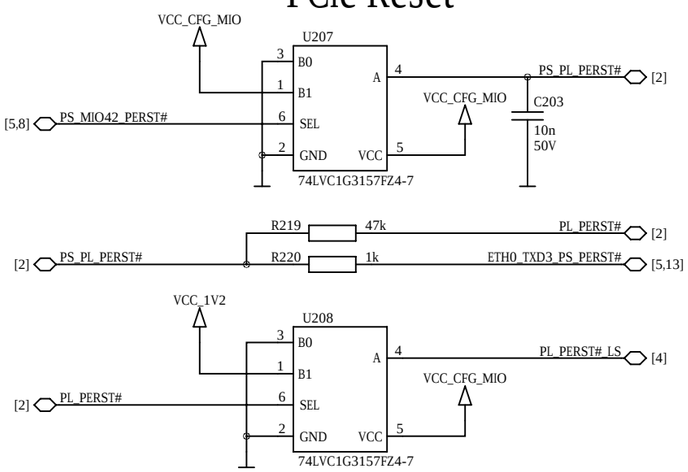
Revision 2.1

ENCLUSTRA	Copyright © 2019 by Enclustra GmbH	Sheet Name 01_COVER	Customer No 0000	Revision R2.1	DNE = do not equip	Confidential	
	Company Enclustra FPGA Solution Center	Project Mercury+ XU8	Project No 466	Designed MHEI	Date 17 Jan 2020	Sheet/sheets 1 / 22	

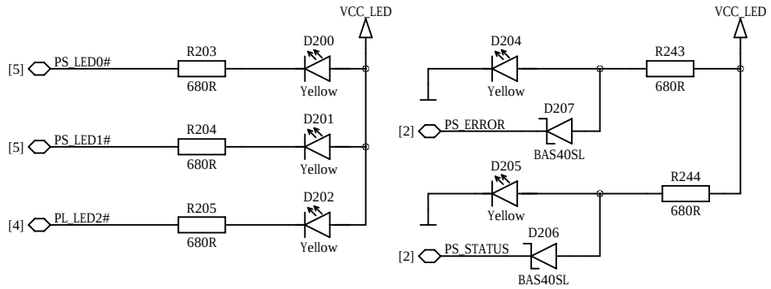
Boot Mode Selection



PCIe Reset



User LEDs

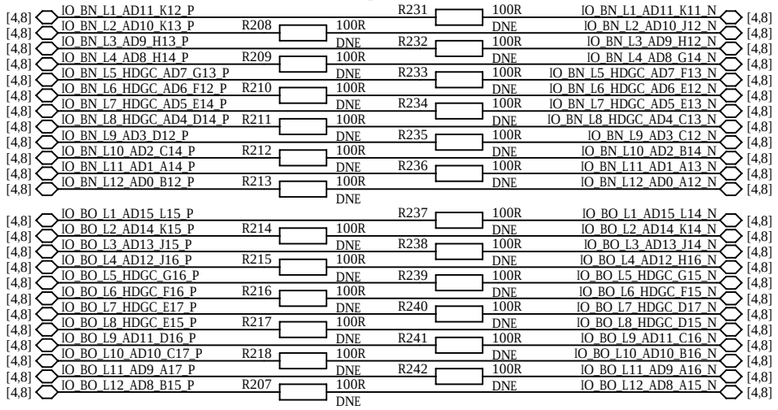


LED Power

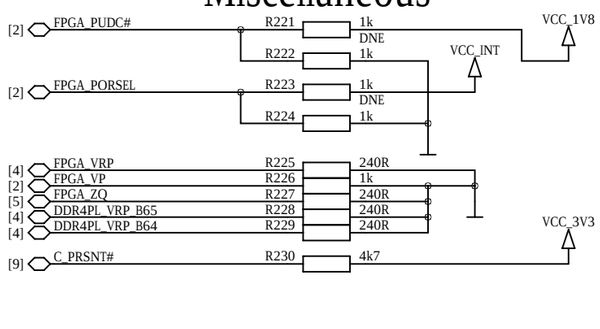
This part is intentionally left blank.

HD Bank Termination

optional



Miscellaneous

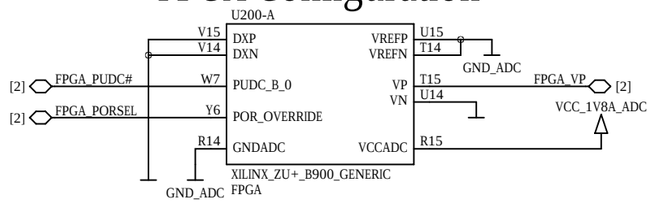


Boot Modes

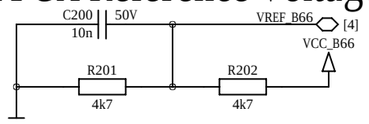
	Boot Mode		Mode Straps	Configuration	
	1	0	PS_MODE	PL Boot	PS Boot
eMMC Mode	0	0	0110	PS	eMMC
SD Mode LS (not supported)	0	1	1110	PS	SDIO (with level shifter)
QSPI Mode	1	0	0010	PS	QSPI
SD Mode (default)	1	1	0101	PS	SDIO
JTAG Mode (*)	1	0	0000	PS	JTAG

SD Mode LS mode may be supported in the future. It requires VCC_CFG_MIO of 1.8V.
(*) Short-circuit R252 to enable JTAG mode

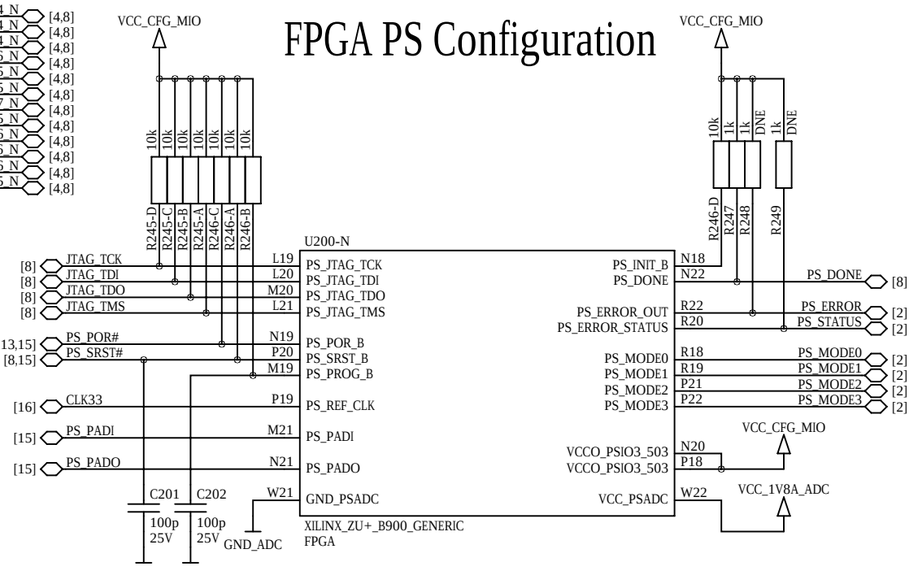
FPGA Configuration



FPGA Reference Voltage

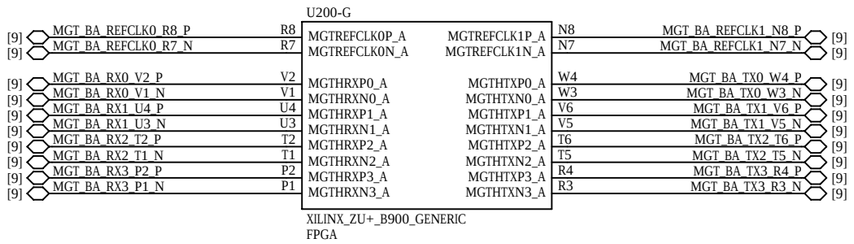


FPGA PS Configuration



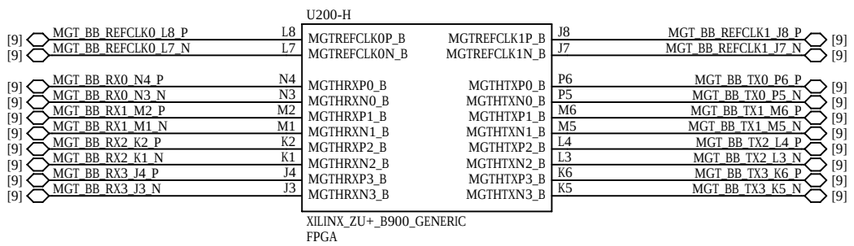
FPGA MGT Bank A

Bank 223 on ZU4/ZU5 | Bank 224 on ZU7



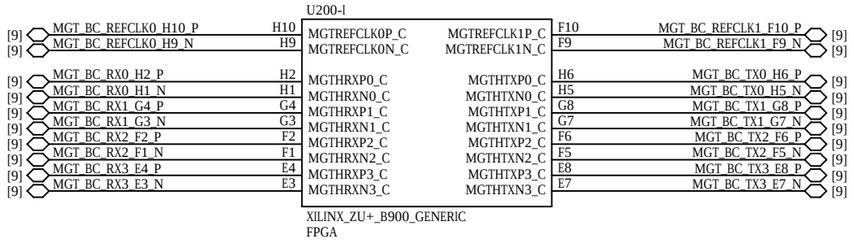
FPGA MGT Bank B

Bank 224 on ZU4/ZU5 | Bank 225 on ZU7



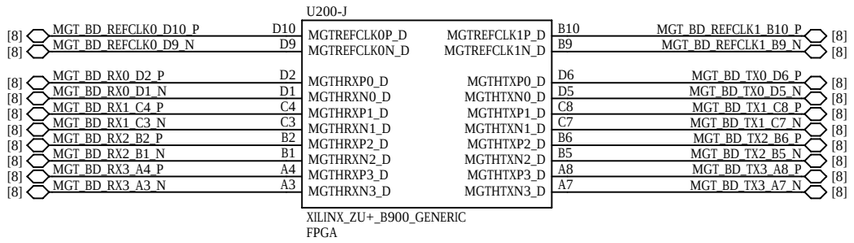
FPGA MGT Bank C

Bank 225 on ZU4/ZU5 | Bank 226 on ZU7

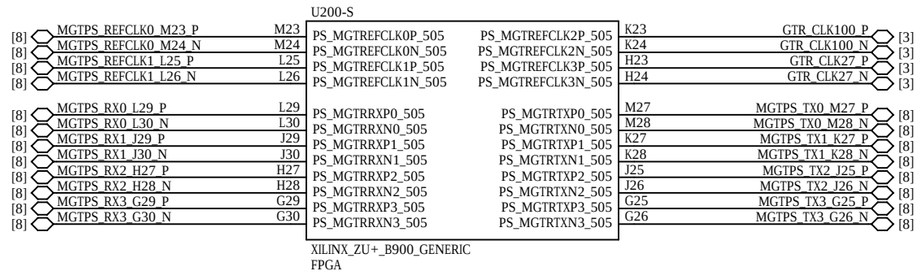


FPGA MGT Bank D

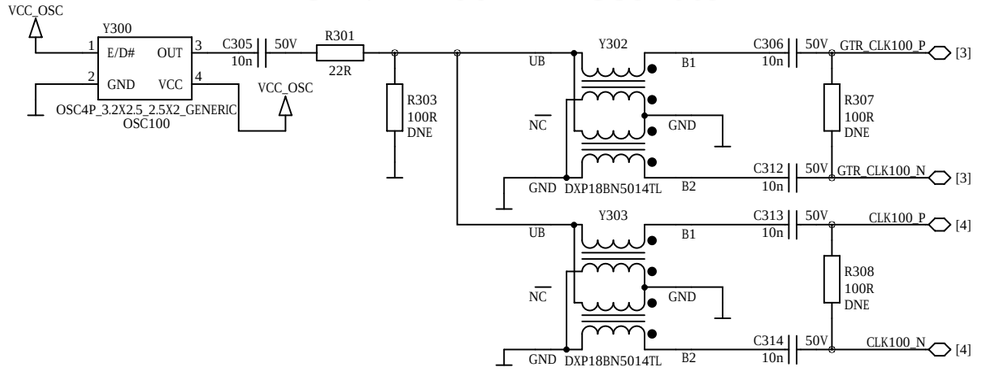
Bank 226 on ZU4/ZU5 | Bank 227 on ZU7



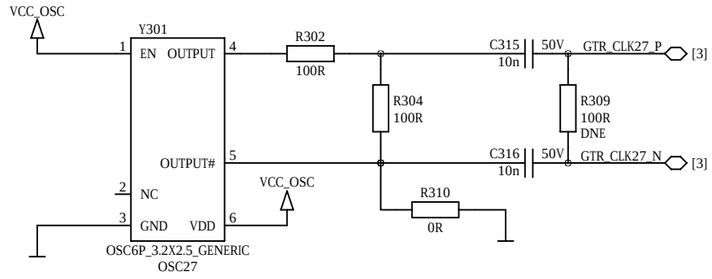
FPGA PS GTR Bank 505



GTR/PL 100 MHz Oscillator



GTR 27 MHz Oscillator

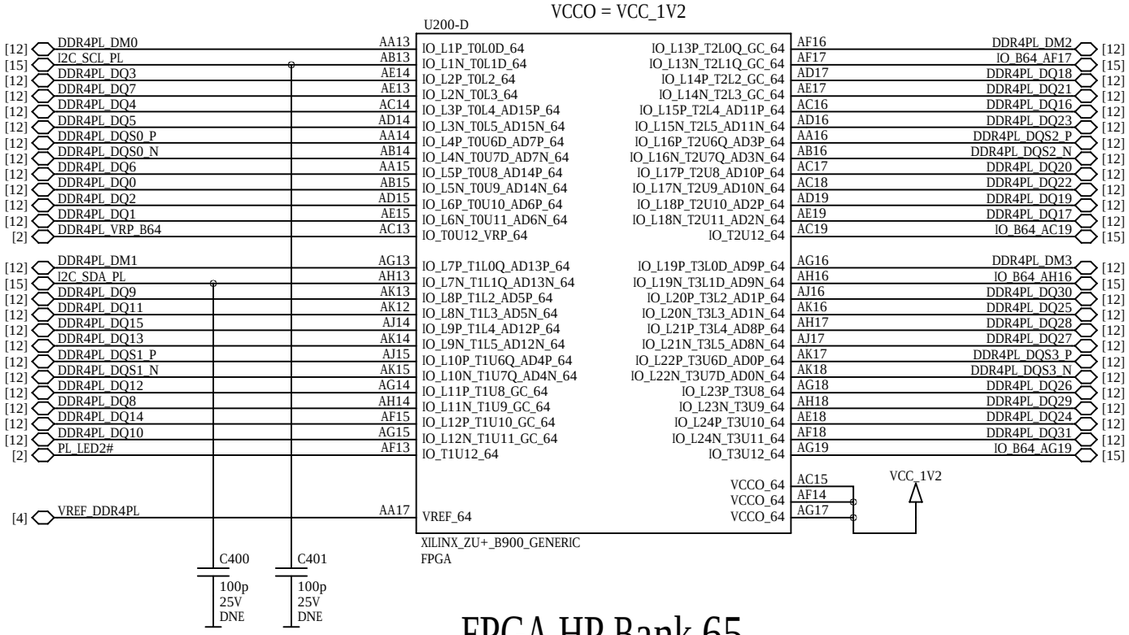


GTR Oscillator Power Filters

This part is intentionally left blank.

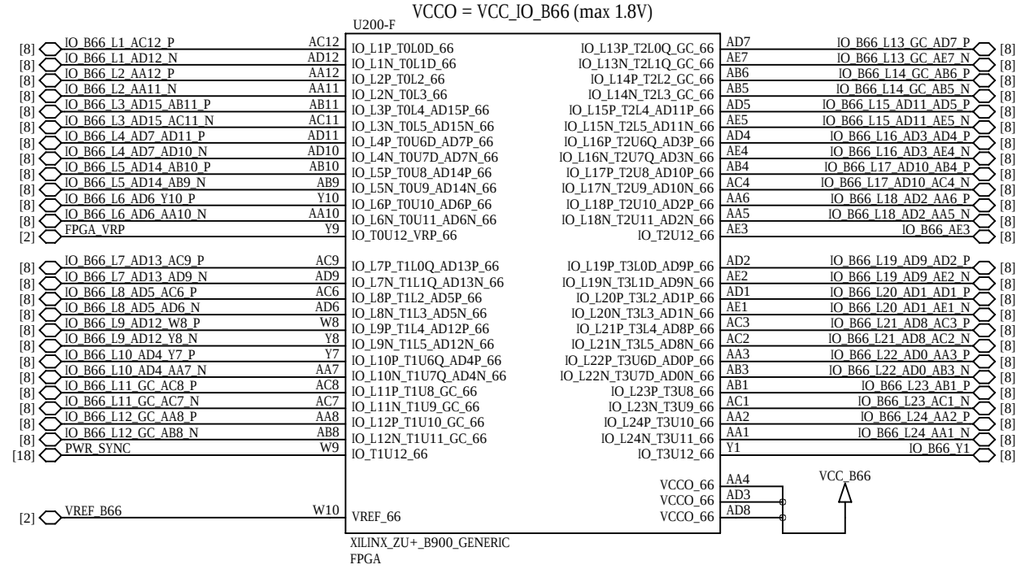
FPGA HP Bank 64

VCCO = VCC_1V2



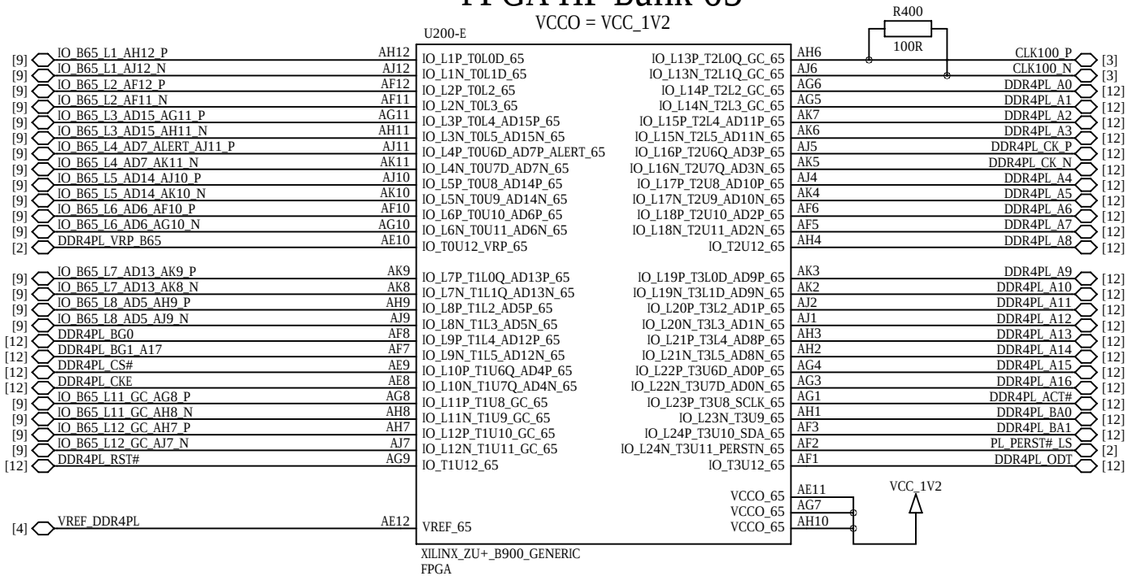
FPGA HP Bank 66

VCCO = VCC_IO_B66 (max 1.8V)



FPGA HP Bank 65

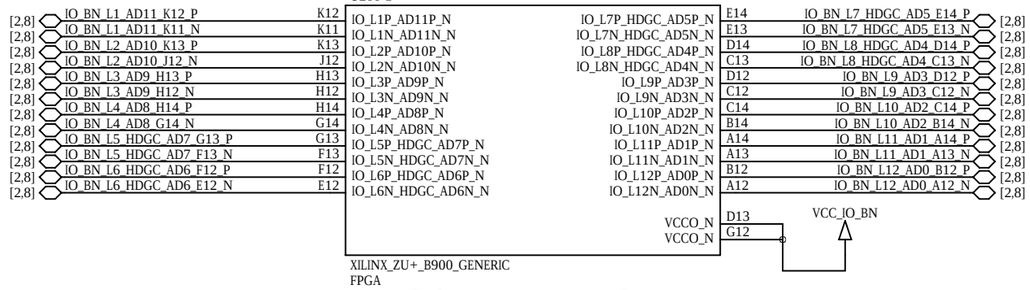
VCCO = VCC_1V2



FPGA HD Bank N

VCCO = VCC_IO_BN (max 3.3V)

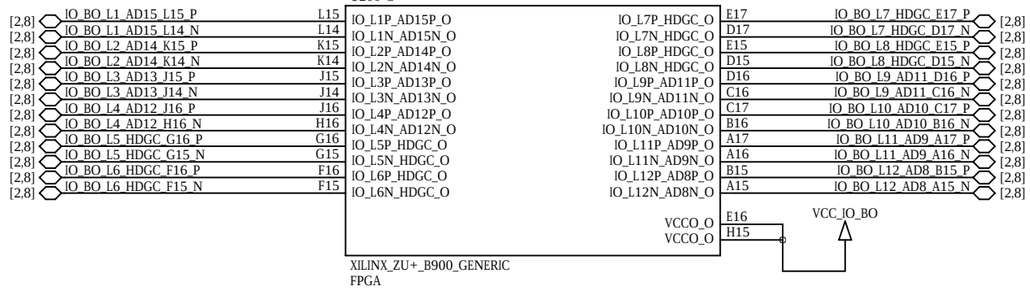
Bank 46 on ZU4/ZU5 | Bank 47 on ZU7



FPGA HD Bank O

VCCO = VCC_IO_BO (max 3.3V)

Bank 45 on ZU4/ZU5 | Bank 48 on ZU7

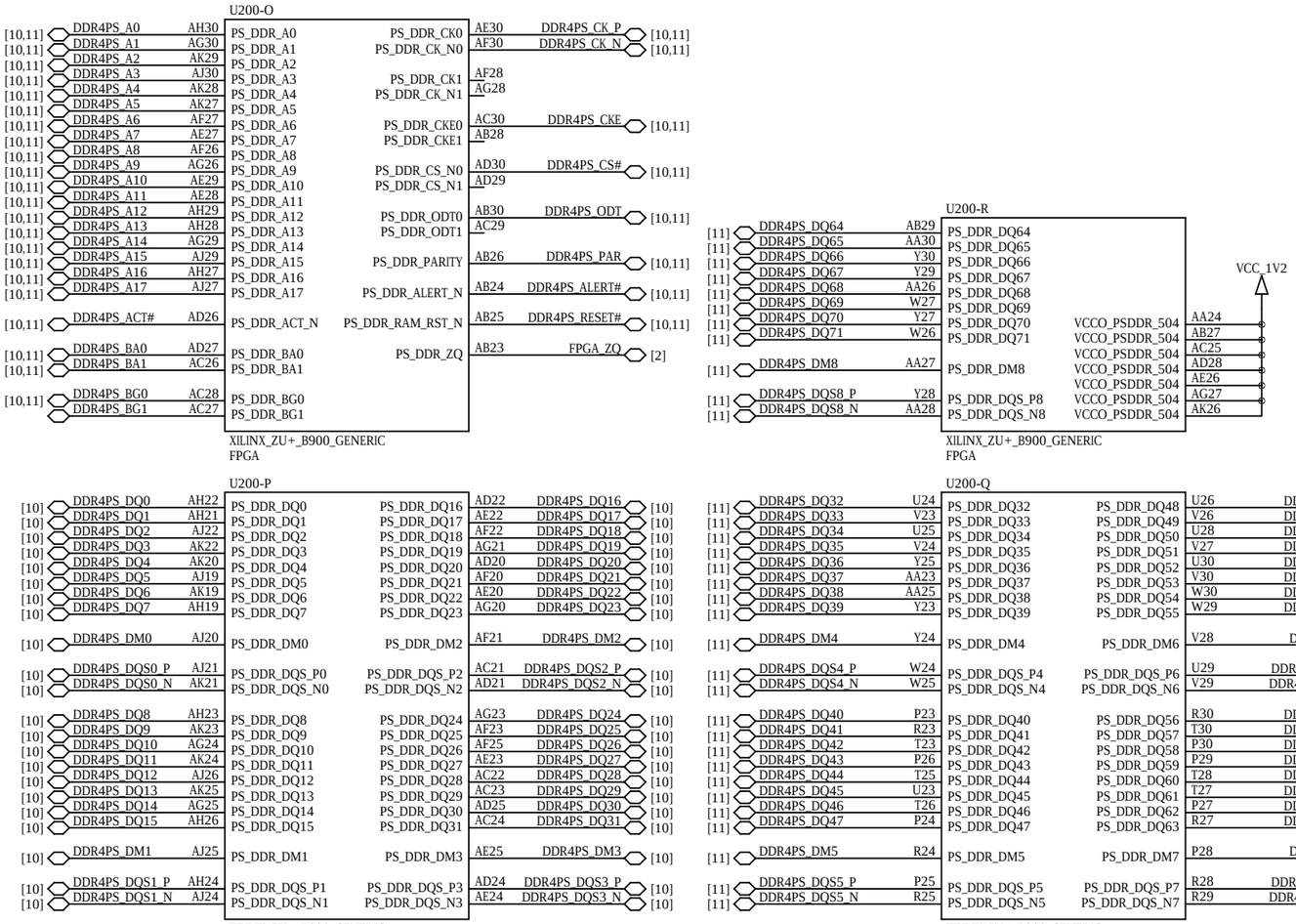


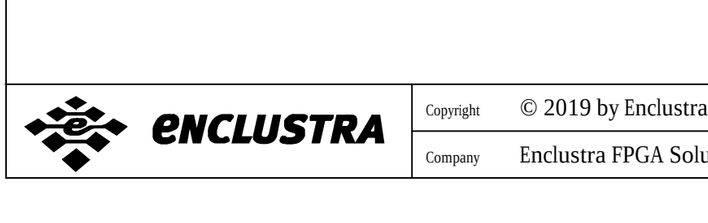
Company	Enclustra FPGA Solution Center	Project	Mercury+ XU8	Project No	466	Designed	MHEI

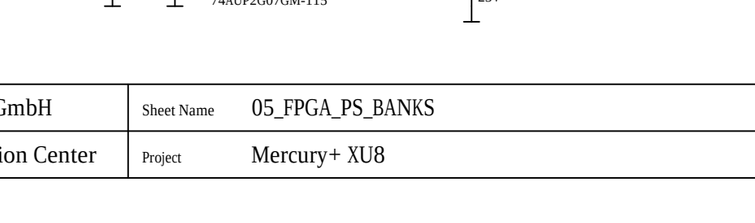
Sheet Name	04_FPGA_IO_BANKS	Customer No	0000	Revision	R2.1	DNE = do not equip	Confidential
Date	17 Jan 2020	Sheet/sheets	4 / 22				

FPGA PS DDR Bank 504

VCCO = VCC_1V2

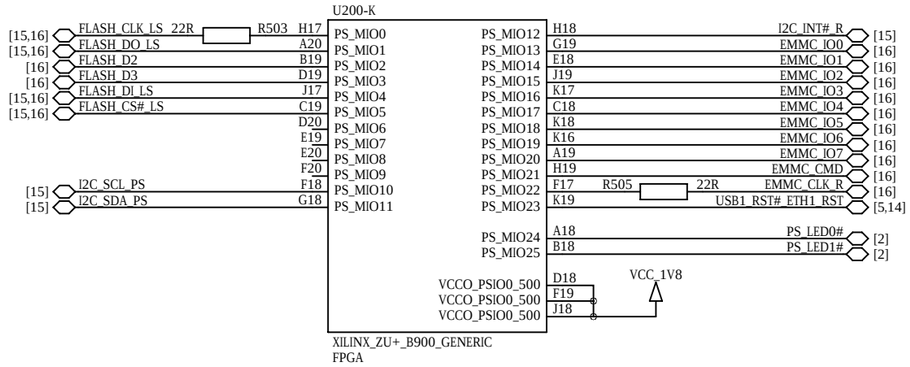






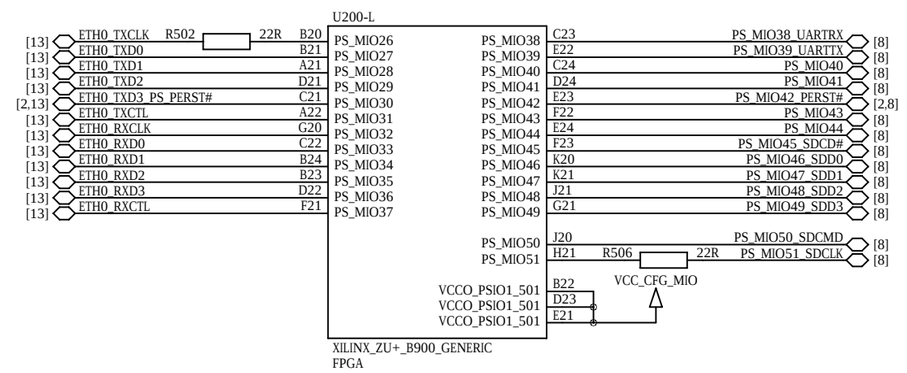
FPGA PS Bank 500

VCCO = VCC_1V8



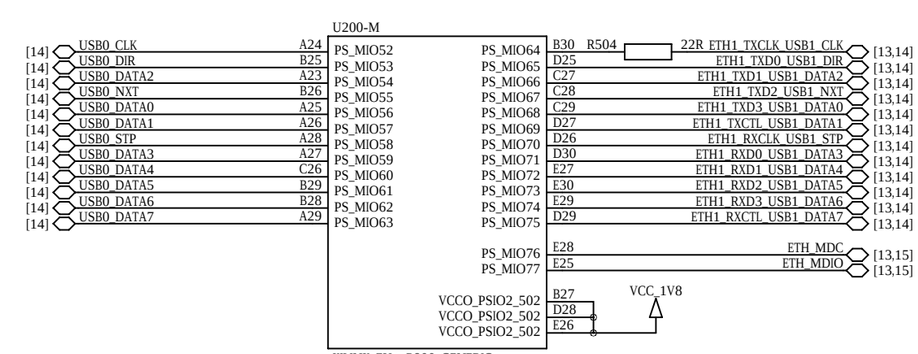
FPGA PS Bank 501

VCCO = VCC_CFG_MIO



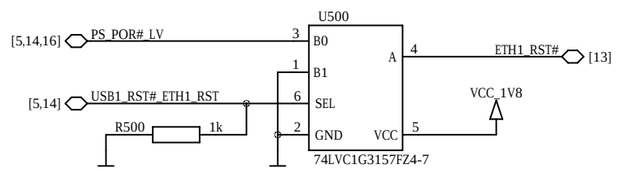
FPGA PS Bank 502

VCCO = VCC_1V8

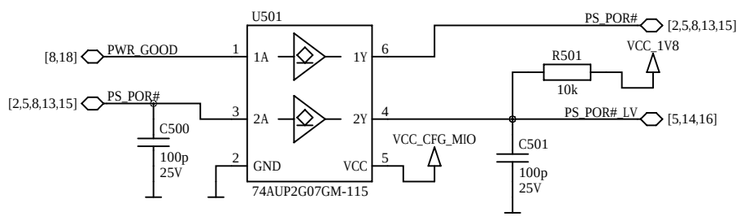


USB1/ETH1 Selection

default is ETH1 enabled, USB1 in reset

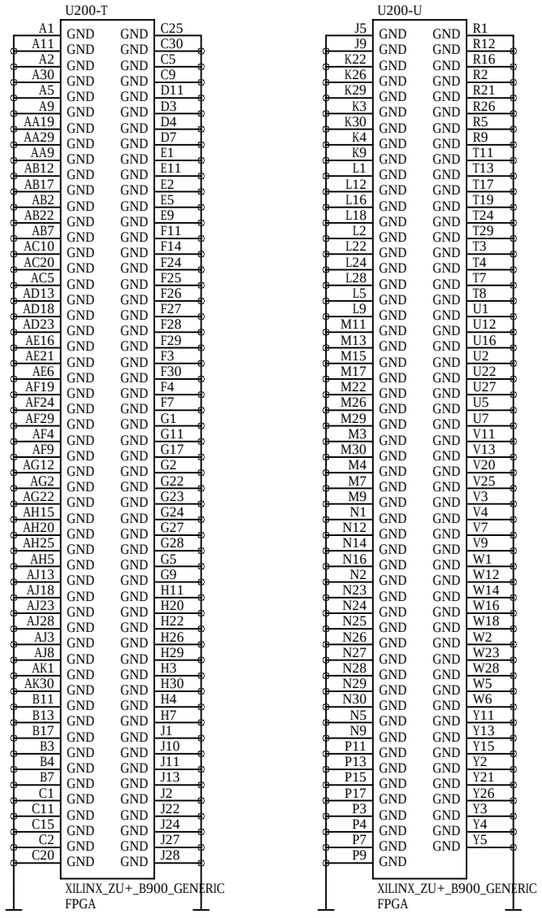


Reset Circuit

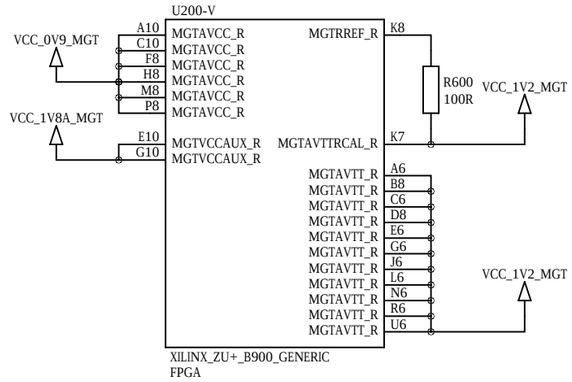


ENCLUSTRA	Copyright	© 2019 by Enclustra GmbH	Sheet Name	05_FPGA_PS_BANKS	Customer No 0000	Revision R2.1	DNE = do not equip	Confidential
	Company	Enclustra FPGA Solution Center	Project	Mercury+ XU8	Project No 466	Designed MHEI	Date 17 Jan 2020	Sheet/sheets 5 / 22

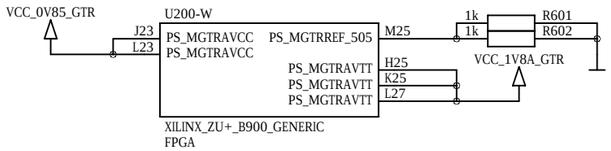
FPGA Ground



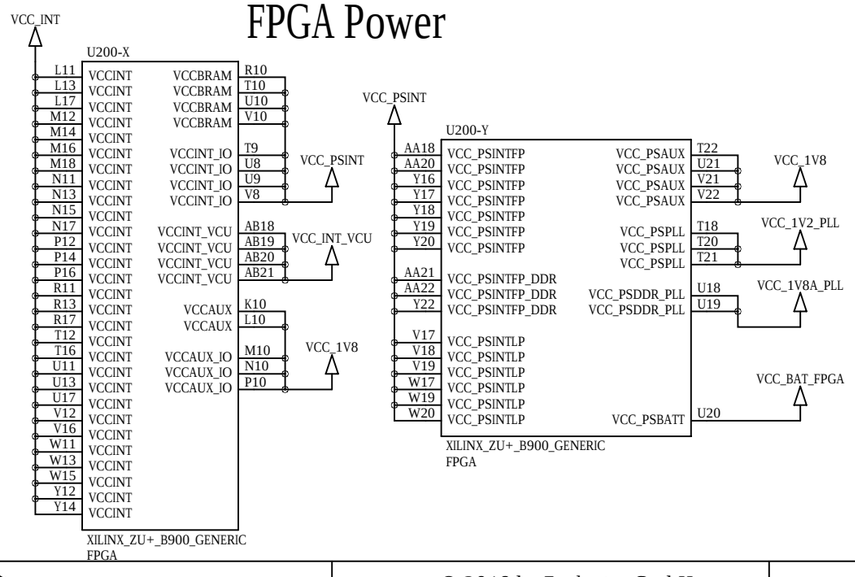
FPGA MGT Power



FPGA GTR Power



FPGA Power

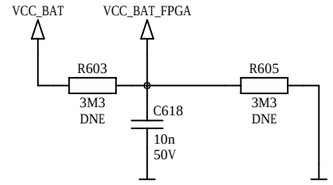


MGT Power Filters

not included in user schematics

This part is intentionally left blank.

FPGA Battery Voltage

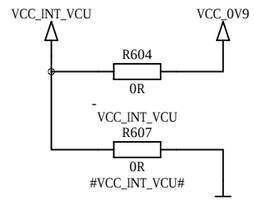


ADC Power

not included in user schematics

This part is intentionally left blank.

FPGA Power



PLL and GTR Power Filters

not included in user schematics

This part is intentionally left blank.

ENCLUSTRA	Copyright	© 2019 by Enclustra GmbH	Sheet Name	06_FPGA_POWER	Customer No	0000	Revision	R2.1	DNE = do not equip	Confidential
	Company	Enclustra FPGA Solution Center	Project	Mercury+ XU8	Project No	466	Designed	MHEI	Date 17 Jan 2020	Sheet/sheets 6 / 22

FPGA Decoupling

not included in user schematics

This part is intentionally left blank.

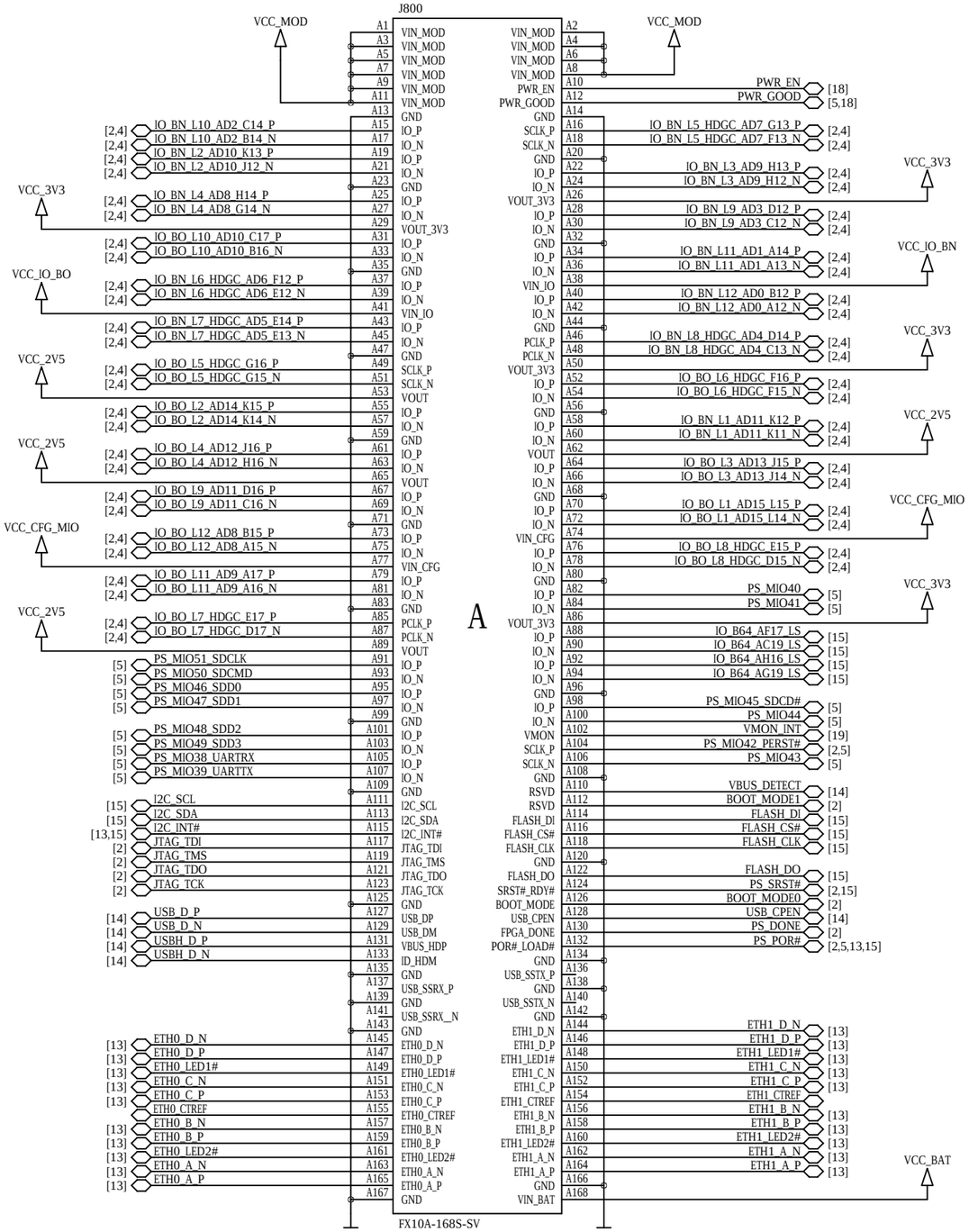
Power Decoupling

not included in user schematics

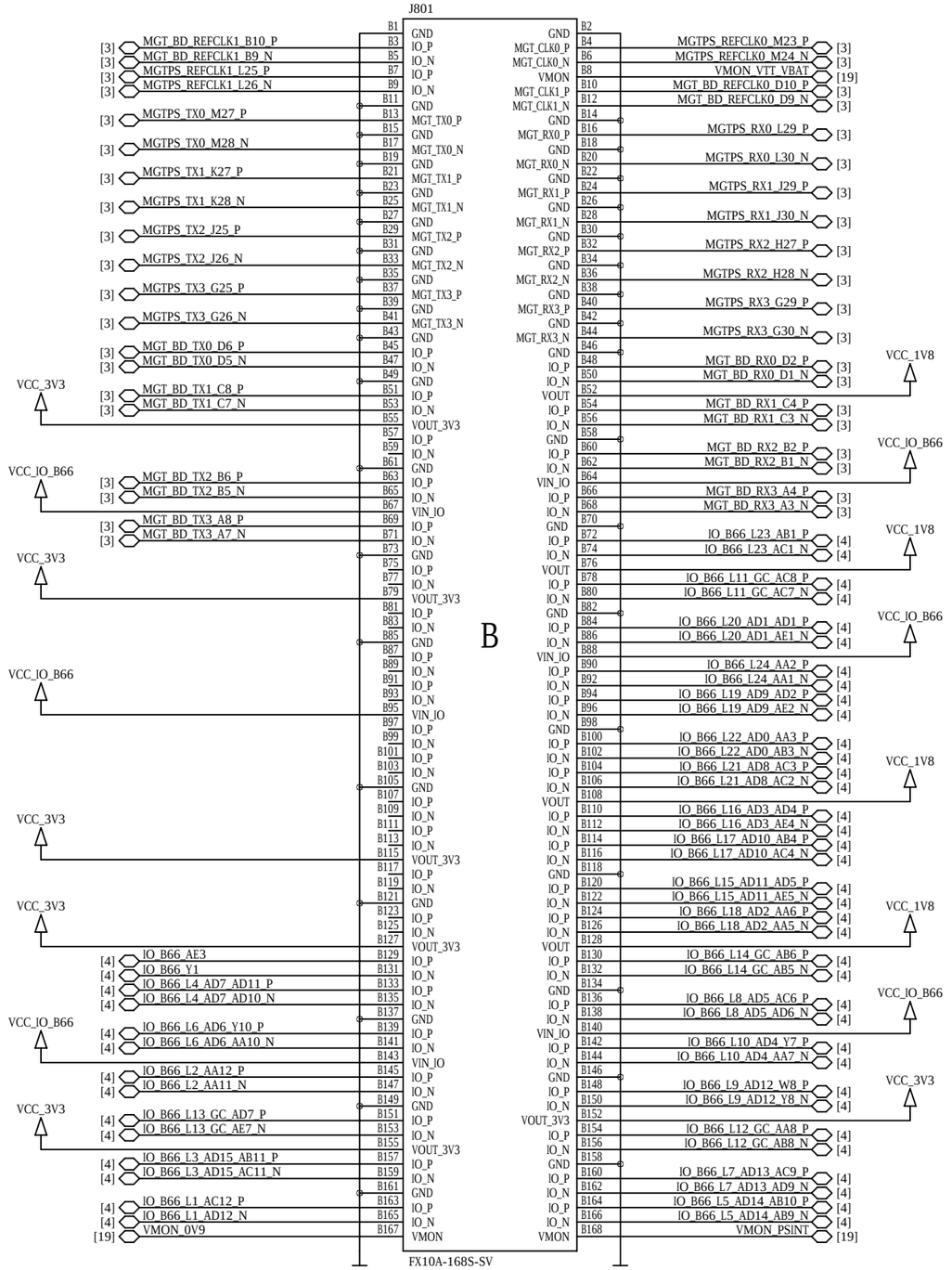
This part is intentionally left blank.

ENCLUSTRA	Copyright	© 2019 by Enclustra GmbH	Sheet Name	07_POWER_DECOUPLING	Customer No	0000	Revision	R2.1	DNE = do not equip	Confidential
	Company	Enclustra FPGA Solution Center	Project	Mercury+ XU8	Project No	466	Designed	MHEI	Date 17 Jan 2020	Sheet/sheets 7 / 22

Module Connector A

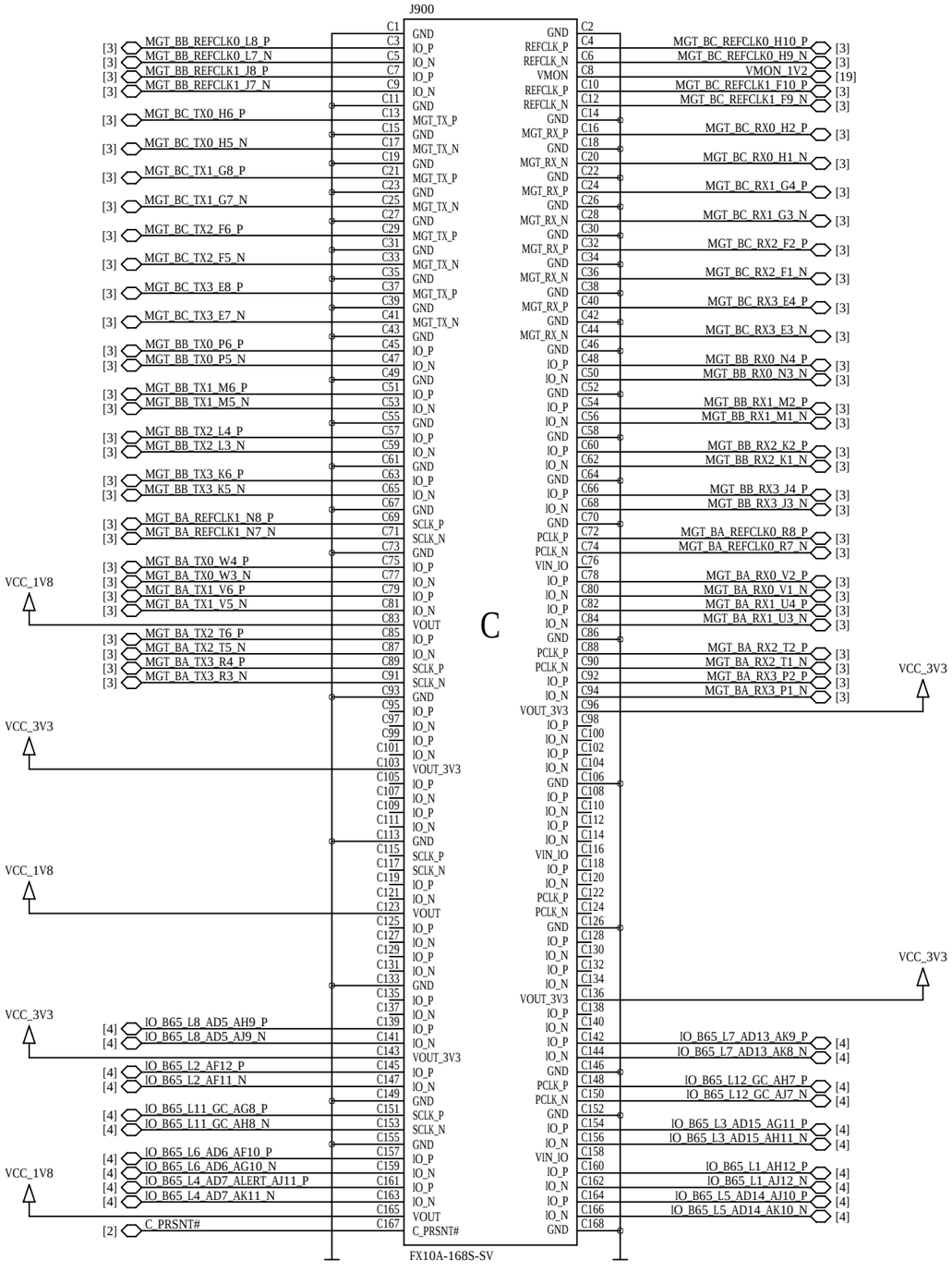


Module Connector B



ENCLUSTRA	Copyright	© 2019 by Enclustra GmbH	Sheet Name	08_MODULE_CONNECTORS_A_B	Customer No	0000	Revision	R2.1	DNE = do not equip	Confidential
	Company	Enclustra FPGA Solution Center	Project	Mercury+ XU8	Project No	466	Designed	MHEI	Date 17 Jan 2020	Sheet/sheets 8 / 22

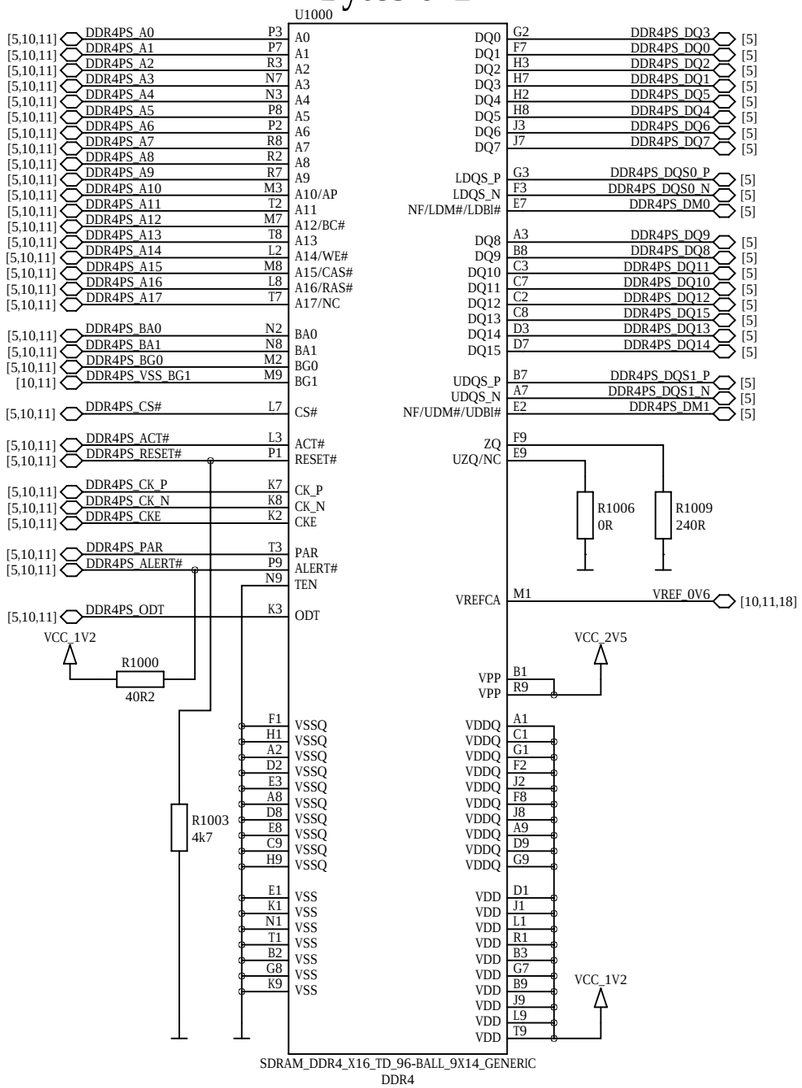
Module Connector C



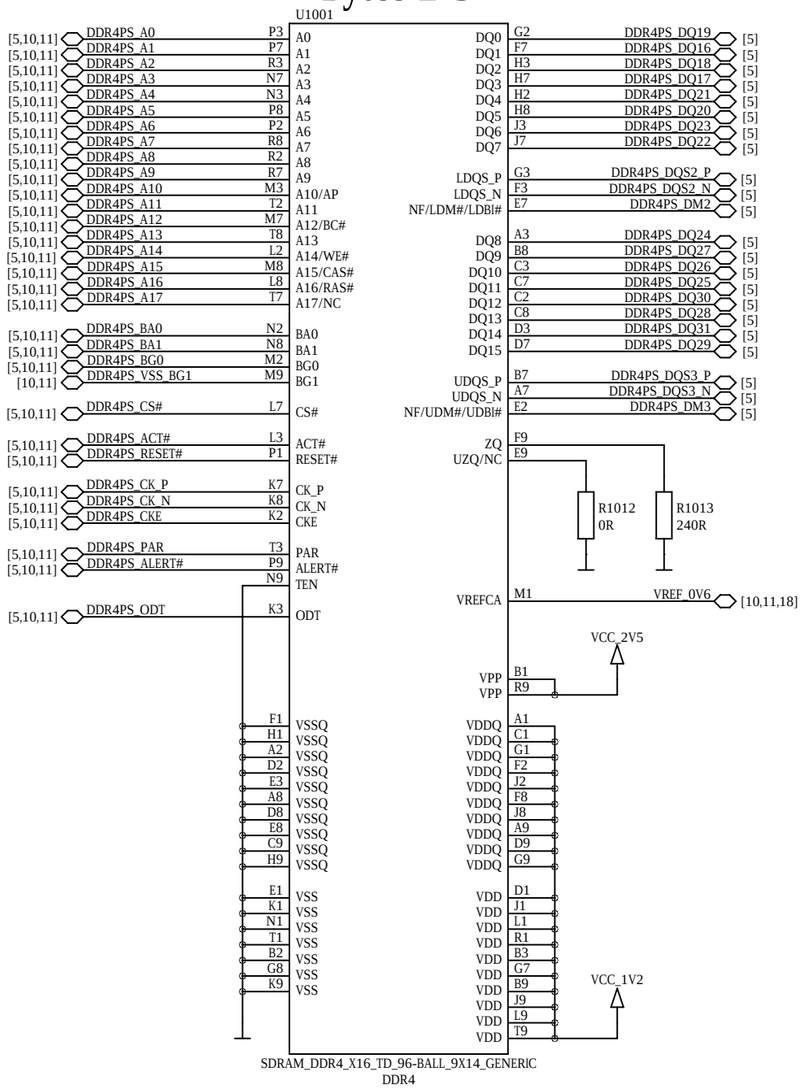
ENCLUSTRA	Copyright	© 2019 by Enclustra GmbH	Sheet Name	09_MODULE_CONNECTOR_C	Customer No	0000	Revision	R2.1	DNE = do not equip	Confidential
	Company	Enclustra FPGA Solution Center	Project	Mercury+ XU8	Project No	466	Designed	MHEI	Date 17 Jan 2020	Sheet/sheets 9 / 22

PS DDR4 SDRAM

Bytes 0-1



Bytes 2-3



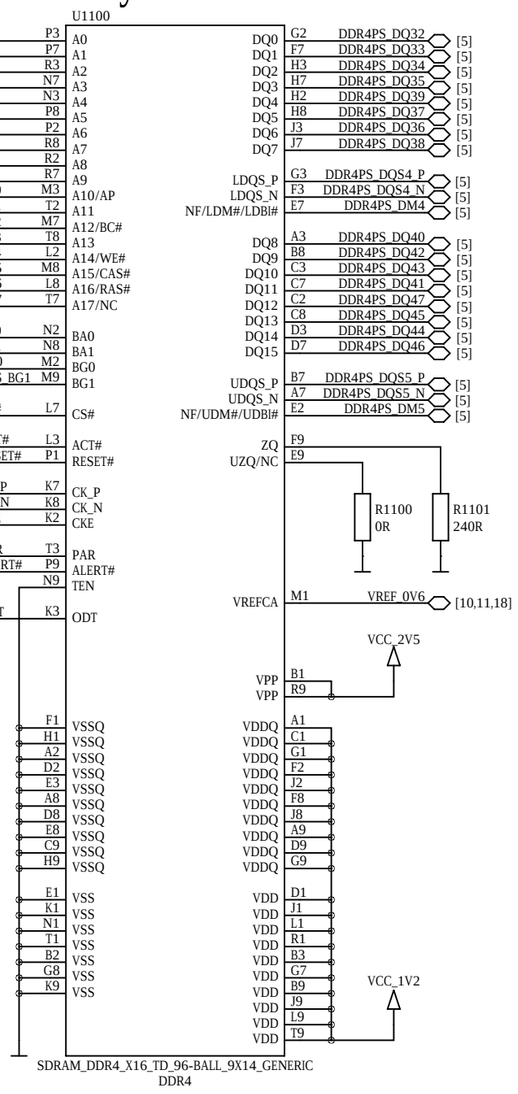
DDR4 Termination

not included in user schematics

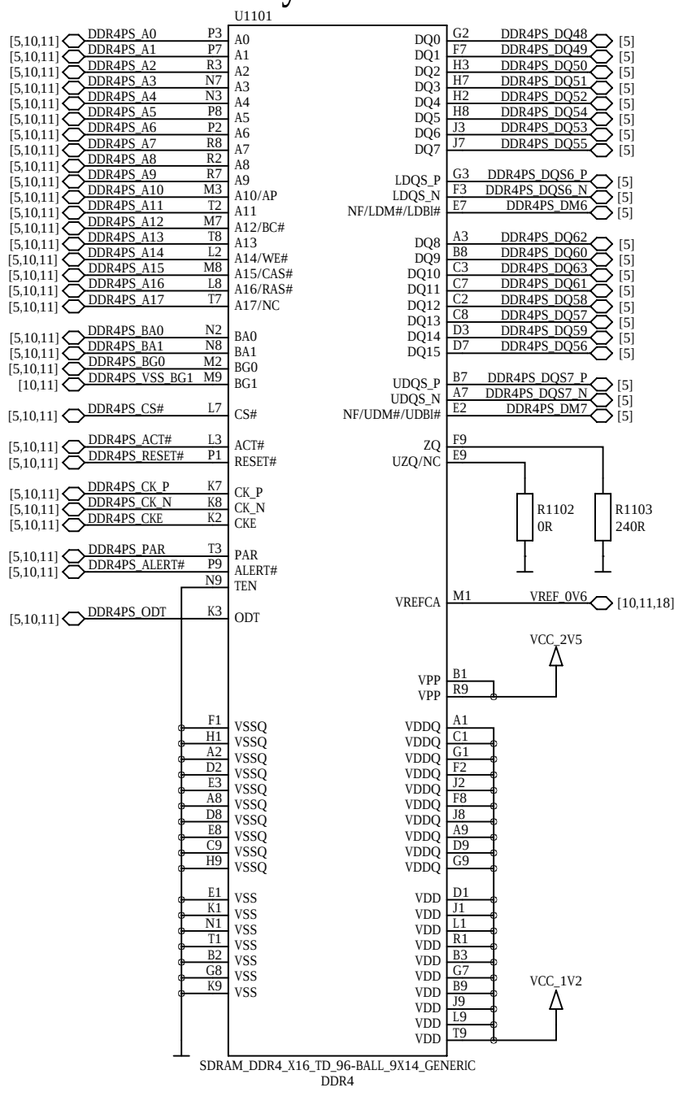
This part is intentionally left blank.

PS DDR4 SDRAM

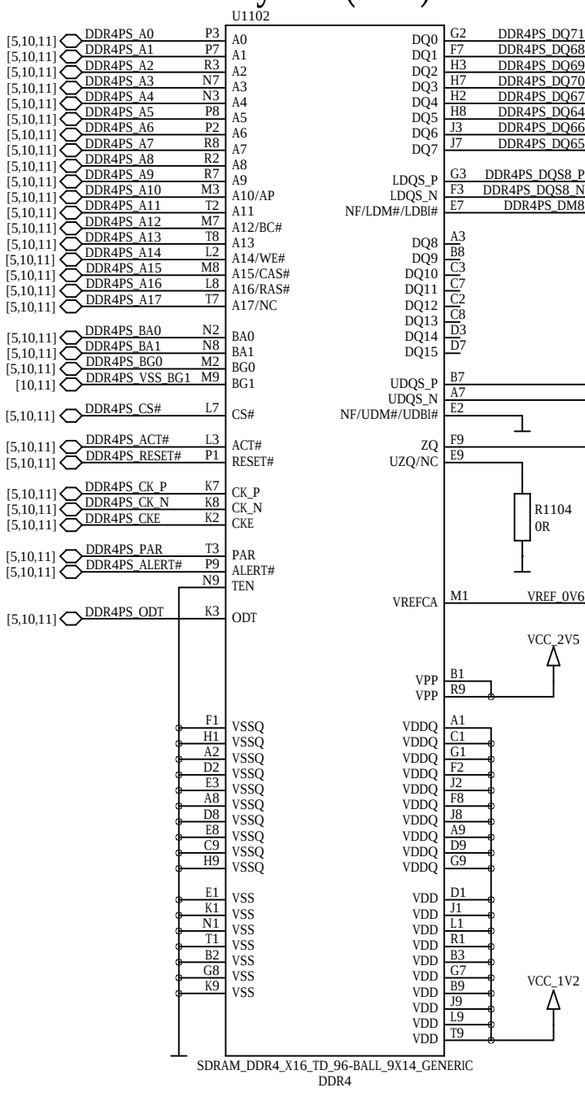
Bytes 4-5



Bytes 6-7



Byte 8 (ECC)

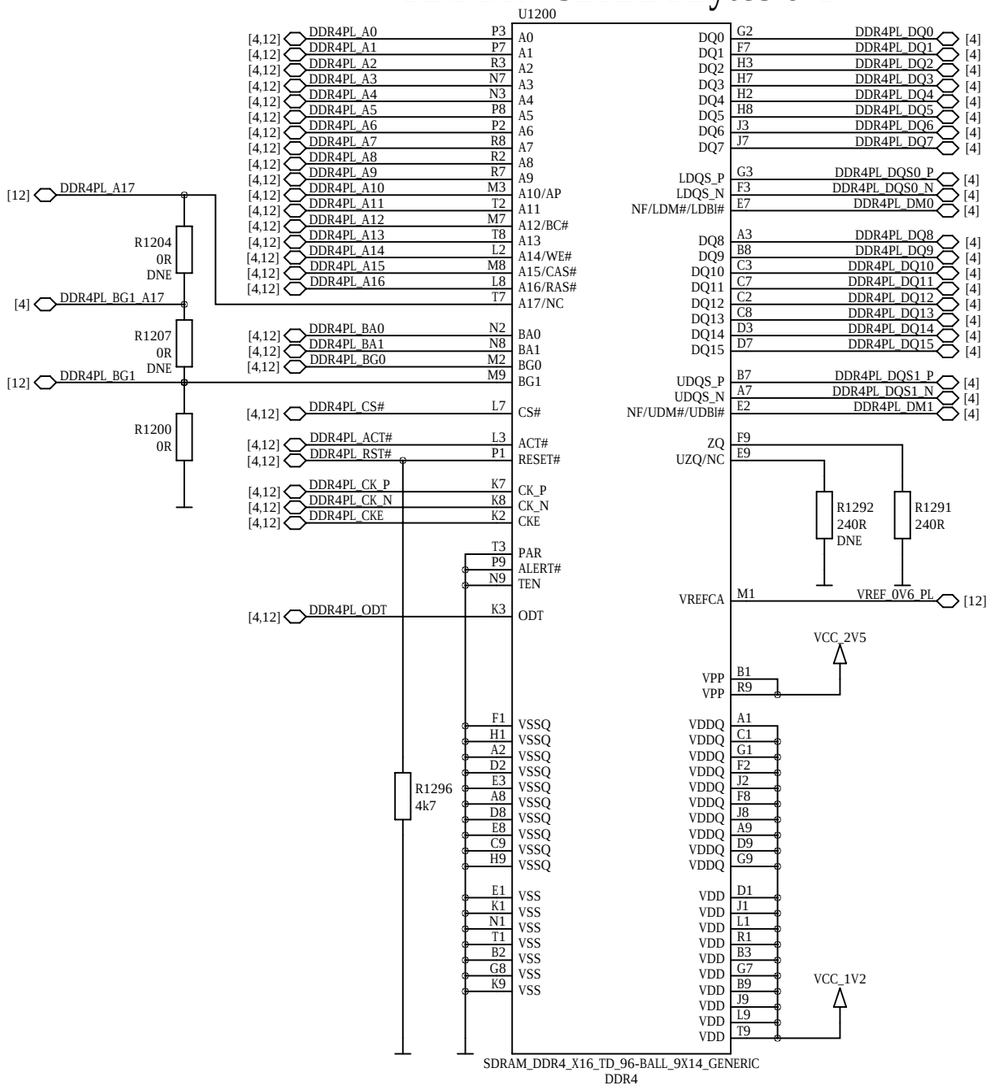


DDR4 Decoupling

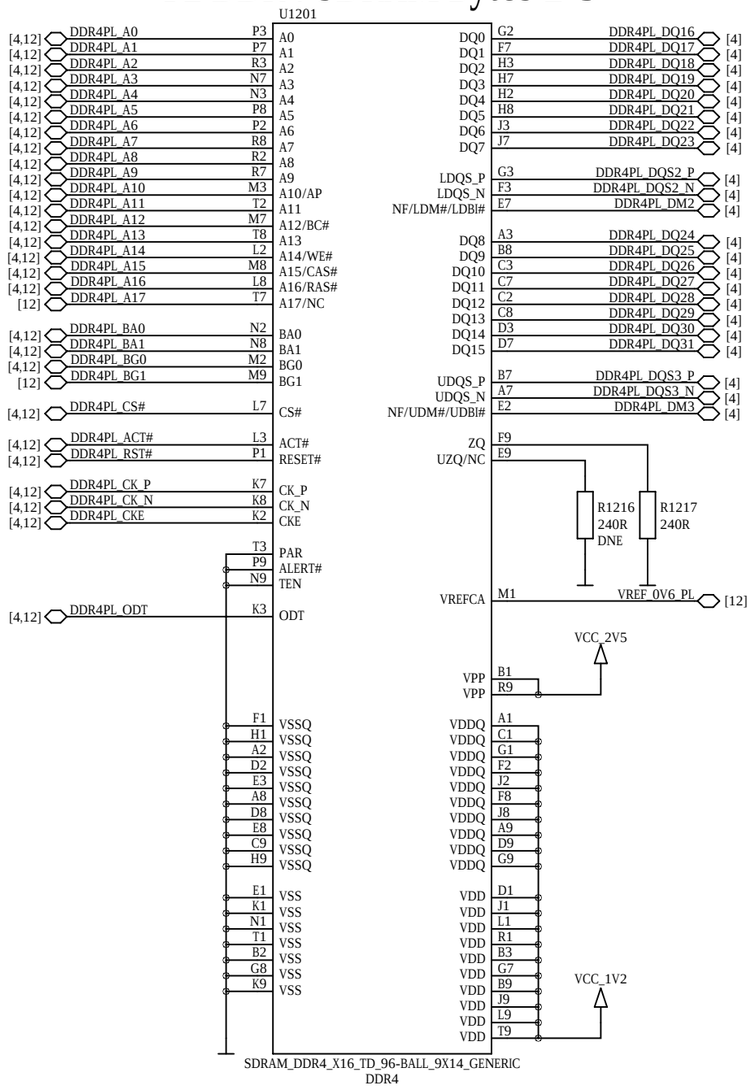
not included in user schematics

This part is intentionally left blank.

PL DDR4 SDRAM Bytes 0-1



PL DDR4 SDRAM Bytes 2-3



DDR4 Termination

not included in user schematics

This part is intentionally left blank.

PL DDR4 Reference Voltage

not included in user schematics

This part is intentionally left blank.

PL DDR4 Decoupling

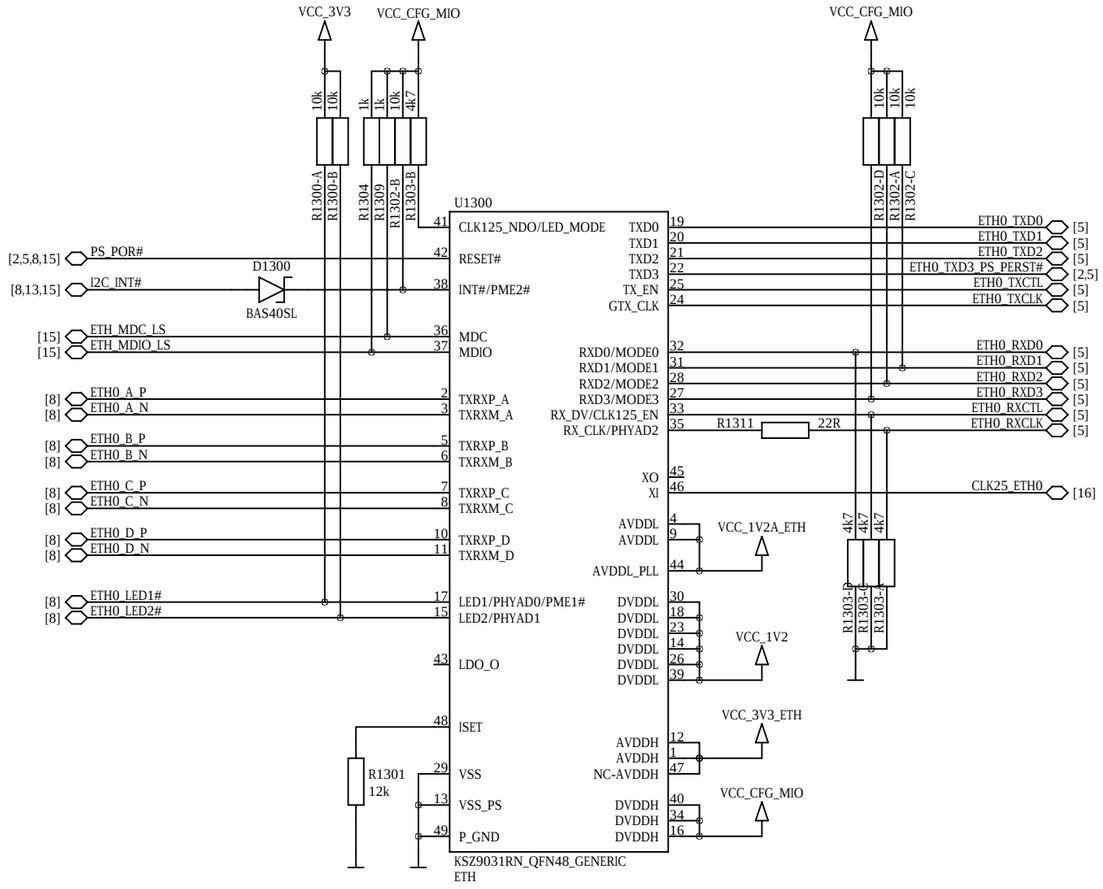
not included in user schematics

This part is intentionally left blank.

ENCLUSTRA	Copyright	© 2019 by Enclustra GmbH	Sheet Name	12_PL_DDR4_SDRAM	Customer No	0000	Revision	R2.1	DNE = do not equip	Confidential
	Company	Enclustra FPGA Solution Center	Project	Mercury+ XU8	Project No	466	Designed	MHEI	Date 17 Jan 2020	Sheet/sheets 12 / 22

Gigabit Ethernet PHY 0

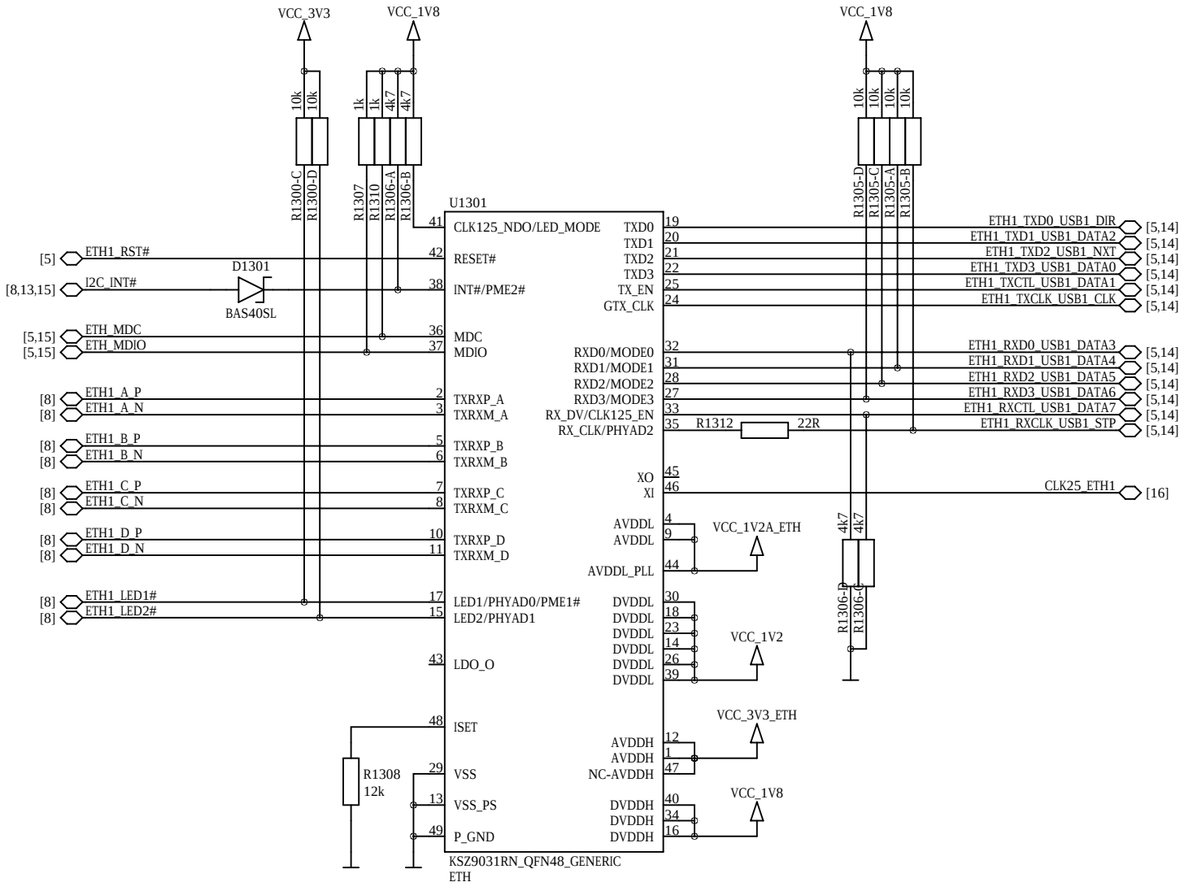
not available when using PS PCIe



MODE<3:0> = 1110 -> RGMII, all capabilities
LED_Mode Pull up = Single LED
PhyAddress <2:0> = 011 -> 3
LED1 and LED2 are active low

Gigabit Ethernet PHY 1

not available when using USB1



MODE<3:0> = 1110 -> RGMII, all capabilities
LED_Mode Pull up = Single LED
PhyAddress <2:0> = 111 -> 7
LED1 and LED2 are active low

Ethernet Power Filters

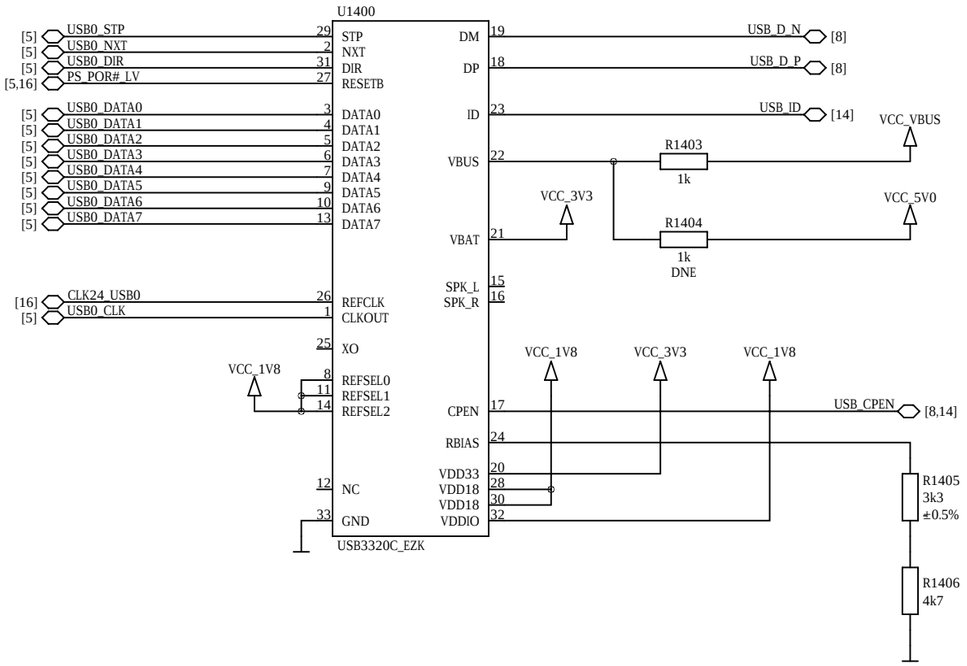
not included in user schematics

This part is intentionally left blank.

ENCLUSTRA	Copyright	© 2019 by Enclustra GmbH	Sheet Name	13_GIGABIT_ETHERNET_PHYS	Customer No	0000	Revision	R2.1	DNE = do not equip	Confidential
	Company	Enclustra FPGA Solution Center	Project	Mercury+ XU8	Project No	466	Designed	MHEI	Date 17 Jan 2020	Sheet/sheets 13 / 22

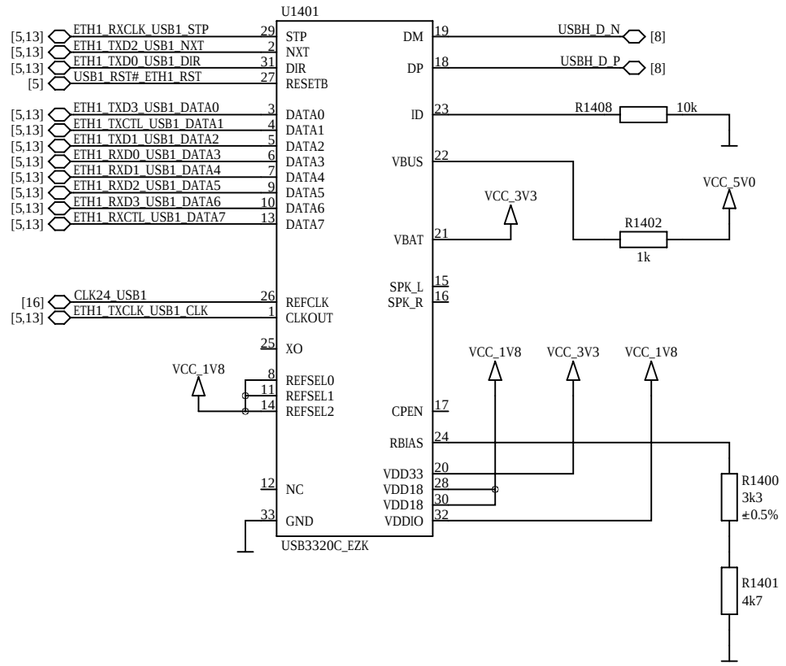
USB 2.0 Device/Host PHY 0

A-Device ID=GND, B-Device ID=Float, Not Used ID=VDD33

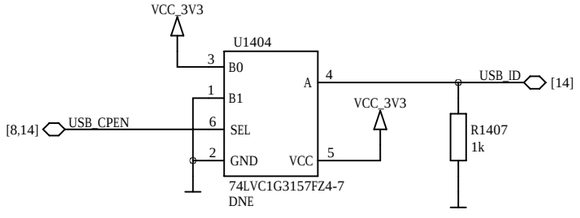


USB 2.0 Host PHY 1

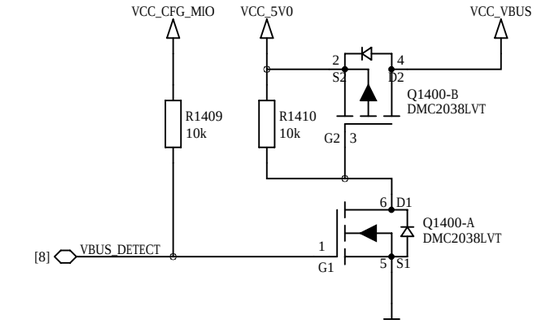
not available when using Ethernet 1



USB 2.0 Host/Device Mode



USB 2.0 VBUS Detect



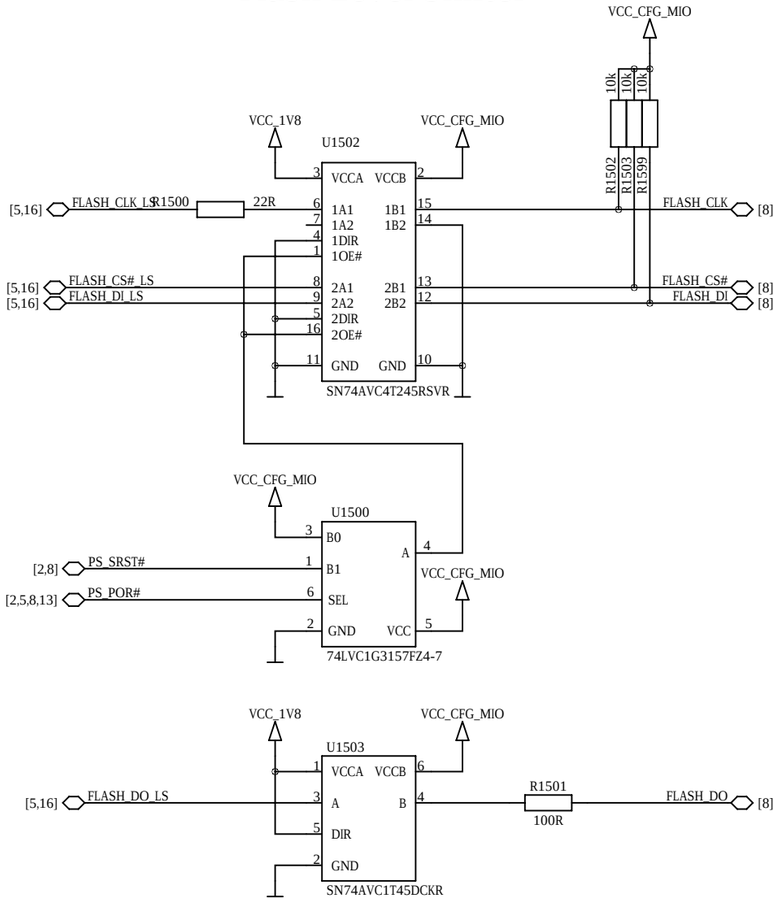
USB 2.0 Power Decoupling

not included in user schematics

This part is intentionally left blank.

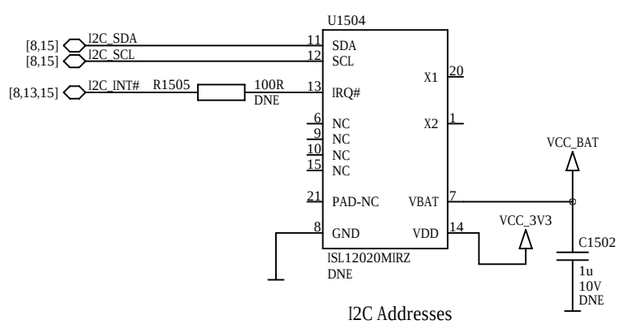
ENCLUSTRA	Copyright	© 2019 by Enclustra GmbH	Sheet Name	14_USB2_PHYS	Customer No	0000	Revision	R2.1	DNE = do not equip	Confidential
	Company	Enclustra FPGA Solution Center	Project	Mercury+ XU8	Project No	466	Designed	MHEI	Date	17 Jan 2020	Sheet/sheets	14 / 22

Flash Level Shifter



Real-time Clock

optional

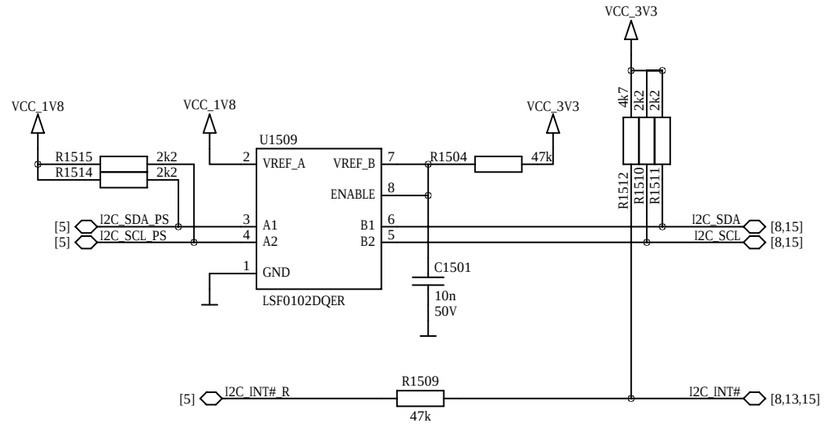


I2C Addresses

RTC registers: 1 1 0 1 1 1 1 Rw

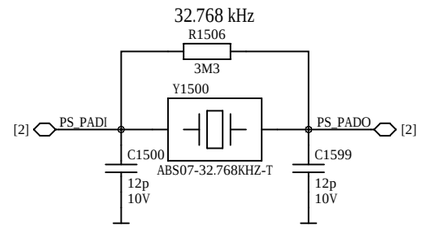
User SRAM: 1 0 1 0 1 1 1 Rw

PS I2C Level Shifter

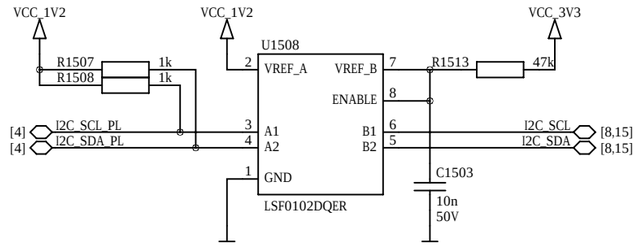


RTC Crystal

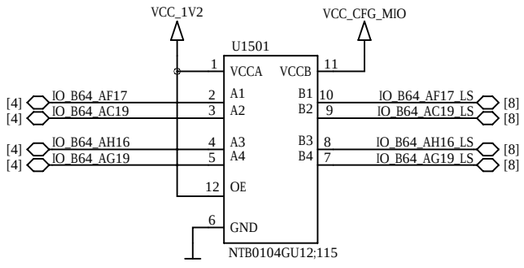
32.768 kHz



PL I2C Level Shifter

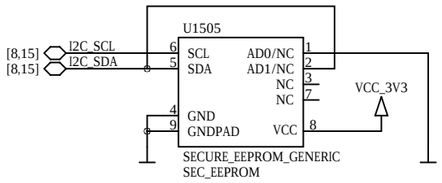


IO Level Shifter



Secure EEPROM

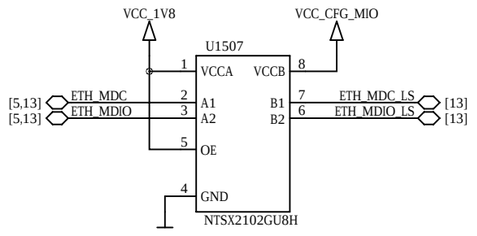
for Enclustra use only



ATSHA204A-MAHDA-T I2C Address: 1 1 0 0 1 0 0 Rw

DS28CN01U-A00+ I2C Address: 1 0 1 1 1 0 0 Rw

MDIO Level Shifter

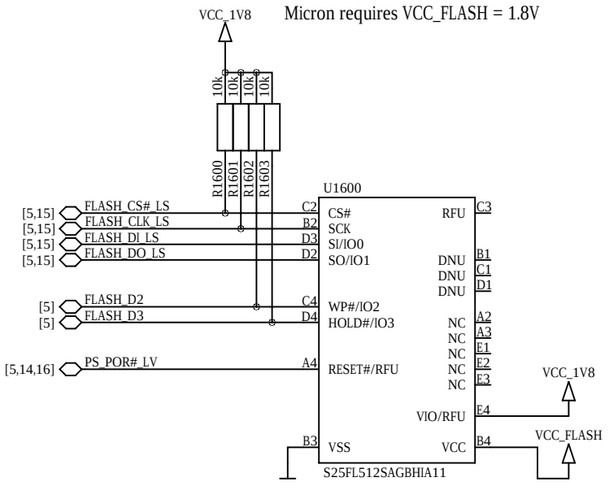


ENCLUSTRA	Copyright	© 2019 by Enclustra GmbH	Sheet Name	15_LEVEL_SHIFTERS_EEPROM	Customer No	0000	Revision	R2.1	DNE = do not equip	Confidential
	Company	Enclustra FPGA Solution Center	Project	Mercury+ XU8	Project No	466	Designed	MHEI	Date 17 Jan 2020	Sheet/sheets 15 / 22

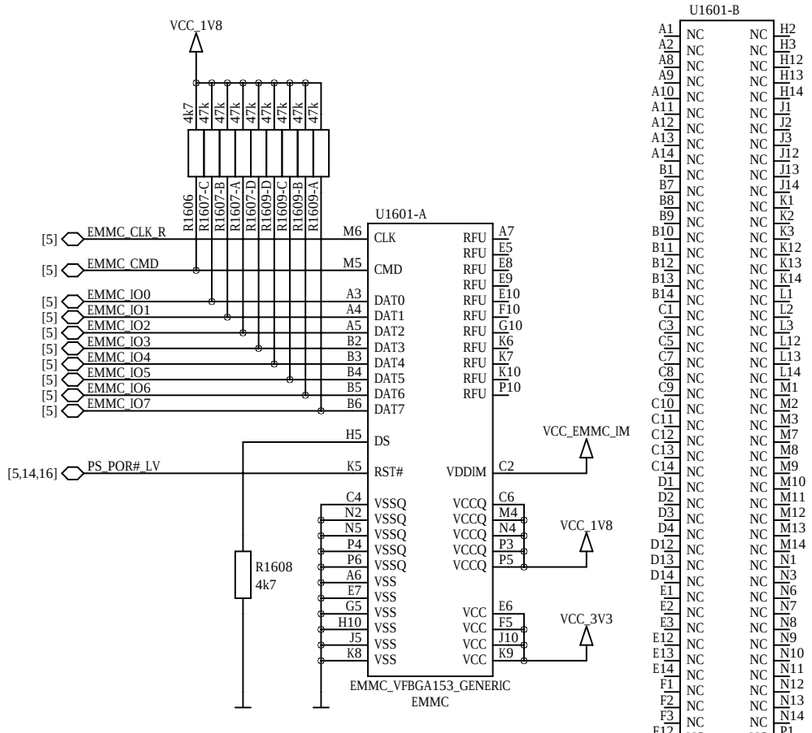
Quad SPI Flash

pin compatible with Micron N25Q512A11G1240F

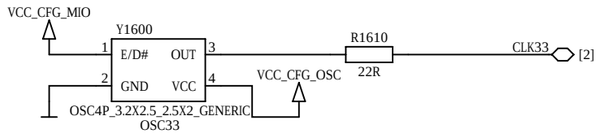
Micron requires VCC_FLASH = 1.8V



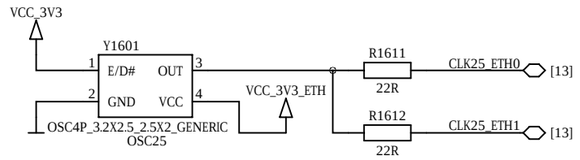
eMMC Flash



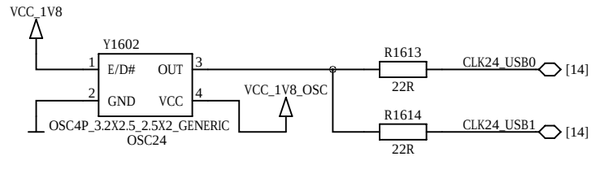
PS 33.3 MHz Oscillator



ETH 25 MHz Oscillator



USB 24 MHz Oscillator



Oscillator Power Filters

not included in user schematics

This part is intentionally left blank.

Quad SPI Power

not included in user schematics

This part is intentionally left blank.

eMMC Power

not included in user schematics

This part is intentionally left blank.

Company	Enclustra FPGA Solution Center	Project	Mercury+ XU8	Project No	466	Designed	MHEI
Sheet Name	16_EMMC_QSPI_FLASH_OSC	Customer No	0000	Revision	R2.1	DNE = do not equip	Confidential
Date	17 Jan 2020	Sheet/sheets	16 / 22				

Dual Buck Converter

channel 1: 3.3V 6A 5% channel 2: 1.2V 6A 5%

not included in user schematics

This part is intentionally left blank.

Supported Voltage Ranges

Power Rail	Direction	Range	Tolerance
VCC_MOD	input	5 - 15V	±5%
VCC_CFG_MIO	input	1.8 - 3.3V	±5%
VCC_IO_BN	input	1.2 - 3.3V	±5%
VCC_IO_BO	input	1.2 - 3.3V	±5%
VCC_IO_B66	input	1.0 - 1.8V	±5%
VCC_BAT	input	2.7 - 3.6V *	-
VCC_1V8	output	1.8V	±5%
VCC_2V5	output	2.5V	±5%
VCC_3V3	output	3.3V	±5%

When using VCC_IO_BN, VCC_IO_BO at 3.3V, the tolerance is -5% +3%.

* Voltage range valid for LDO assembly option for VCC_BAT_FPGA (default assembly variant).

Buck Converter

0.72/0.85/0.9V 35A 3%

not included in user schematics

This part is intentionally left blank.

Input Power Filter

not included in user schematics

This part is intentionally left blank.

LDO 5.0V 0.15A

not included in user schematics

This part is intentionally left blank.

ENCLUSTRA	Copyright	© 2019 by Enclustra GmbH	Sheet Name	17_POWER_INT_3.3V_1.2V_5.0V	Customer No	0000	Revision	R2.1	DNE = do not equip	Confidential
	Company	Enclustra FPGA Solution Center	Project	Mercury+ XU8	Project No	466	Designed	MHEI	Date 17 Jan 2020	Sheet/sheets 17 / 22

Dual Buck Converter

channel 1: 0.85/0.9V 6A 3% channel 2: 0.9V 6A 3%

not included in user schematics

This part is intentionally left blank.

LDO 2.5V 0.5A

not included in user schematics

This part is intentionally left blank.

Power Converter Synchronization

not included in user schematics

This part is intentionally left blank.

DDR4 Termination Voltage Regulator

not included in user schematics

This part is intentionally left blank.

DDR4 VREF Decoupling

not included in user schematics

This part is intentionally left blank.

Power Sequencing

not included in user schematics

This part is intentionally left blank.

ENCLUSTRA	Copyright	© 2019 by Enclustra GmbH	Sheet Name	18_POWER_PSINT_0.9V_2.5V_VTT	Customer No	0000	Revision	R2.1	DNE = do not equip	Confidential
	Company	Enclustra FPGA Solution Center	Project	Mercury+ XU8	Project No	466	Designed	MHEI	Date 17 Jan 2020	Sheet/sheets 18 / 22

Buck Converter 1.8V

1.8V 3A 3%
not included in user schematics

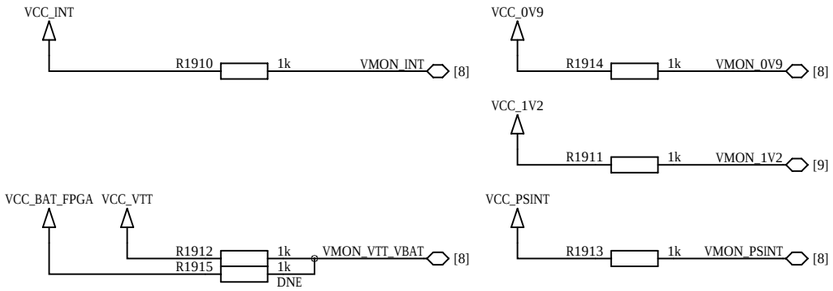
This part is intentionally left blank.

LDO 1.2V 10 mA

not included in user schematics

This part is intentionally left blank.

Voltage Monitoring



FPGA I/O Over-Voltage Protection

not included in user schematics

This part is intentionally left blank.

LDO 0.85V 0.5A

used for -1LE, -2LI, -3E speed grade SoC FPGAs
not included in user schematics

This part is intentionally left blank.

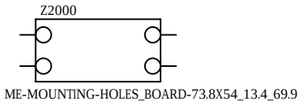
Voltage Reference

not included in user schematics

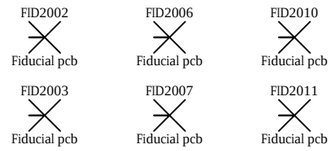
This part is intentionally left blank.

ENCLUSTRA	Copyright	© 2019 by Enclustra GmbH	Sheet Name	19_POWER_1.8V_0V85	Customer No	0000	Revision	R2.1	DNE = do not equip	Confidential
	Company	Enclustra FPGA Solution Center	Project	Mercury+ XU8	Project No	466	Designed	MHEI	Date 17 Jan 2020	Sheet/sheets 19 / 22

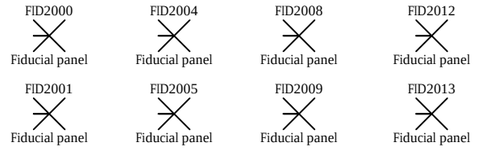
Module Mounting Holes M3



PCB Fiducials

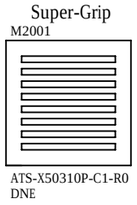


Panel Fiducials

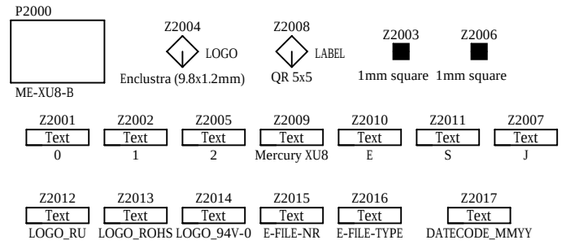


FPGA Heat Sink

optional



PCB / Logo / Pin-1 Marking / Text



ENCLUSTRA	Copyright	© 2019 by Enclustra GmbH	Sheet Name	20_MECHANICS	Customer No	0000	Revision	R2.1	DNE = do not equip	Confidential
	Company	Enclustra FPGA Solution Center	Project	Mercury+ XU8	Project No	466	Designed	MHEI	Date 17 Jan 2020	Sheet/sheets 20 / 22

Component Variants

FPGA	DDR4			eMMC	Ethernet PHY	OSC27	OSC24
Part U200A XCZU4CG-1FBVB900E EN102158	Part U1000A:1 H5AN4G6NAFR-UHC EN101655 Part U1000A:2 MT40A256M16GE-083E EN101632	Part U1000B K4A4G165WE-BIRC EN101868	Part U1000C K4A8G165WB-BIRC EN101979	Part U1601A H26M52208FPRI EN101865	Part U1300A KSZ9031RNXIA EN101934	Part Y301A ASEMPC_27.000MHZ-LR-T EN101608	Part Y1602A ASDMB-24.000MHZ-LC-T EN101221
Part U200B XCZU4CG-1FBVB900I EN102716	Part U1001A:1 H5AN4G6NAFR-UHC EN101655 Part U1001A:2 MT40A256M16GE-083E EN101632	Part U1001B K4A4G165WE-BIRC EN101868	Part U1001C K4A8G165WB-BIRC EN101979	Part U1601B EMMC16G-W525-X01U EN101932	Part U1300B KSZ9031RNXCA EN100202	Part Y301B ASEMPC-27.000MHZ-XR-T EN101609	Part Y1602B ASEMB_24.000MHZ-LC-T EN101187
Part U200C XCZU5EV-1FBVB900I EN102159	Part U1100A:1 H5AN4G6NAFR-UHC EN101655 Part U1100A:2 MT40A256M16GE-083E EN101632	Part U1100B K4A4G165WE-BIRC EN101868	Part U1100C K4A8G165WB-BIRC EN101979	Part U1601C EMMC16G-IB29-PZ90 EN102591	Part U1301A KSZ9031RNXIA EN101934		
Part U200D XCZU7EV-1FBVB900E EN102615	Part U1101A:1 H5AN4G6NAFR-UHC EN101655 Part U1101A:2 MT40A256M16GE-083E EN101632	Part U1101B K4A4G165WE-BIRC EN101868	Part U1101C K4A8G165WB-BIRC EN101979		Part U1301B KSZ9031RNXCA EN100202		
Part U200E XCZU7EV-2FBVB900I EN102160	Part U1102A:1 H5AN4G6NAFR-UHC EN101655 Part U1102A:2 MT40A256M16GE-083E EN101632	Part U1102B K4A4G165WE-BIRC EN101868	Part U1102C K4A8G165WB-BIRC EN101979				
	Part U1200A:1 H5AN4G6NAFR-UHC EN101655 Part U1200A:2 MT40A256M16GE-083E EN101632	Part U1200B K4A4G165WE-BIRC EN101868	Part U1200C K4A8G165WB-BIRC EN101979				
	Part U1201A:1 H5AN4G6NAFR-UHC EN101655 Part U1201A:2 MT40A256M16GE-083E EN101632	Part U1201B K4A4G165WE-BIRC EN101868	Part U1201C K4A8G165WB-BIRC EN101979				

Assembly Variants

Assembly Variant	FPGA	DDR4	eMMC	Ethernet PHY	OSC27	OSC24
Variant EN102673:0 ME-XU8-4CG-1E-D11E-R2.1	Option EN102673:1 FPGA EN102158	Option EN102673:2 DDR4 EN101868	Option EN102673:3 EMMC EN102591	Option EN102673:4 ETH EN101934	Option EN102673:5 OSC27 EN101608	Option EN102673:6 OSC24 EN101221
Variant EN102720:0 ME-XU8-4CG-1I-D11E-R2.1	Option EN102720:1 FPGA EN102716	Option EN102720:2 DDR4 EN101868	Option EN102720:3 EMMC EN102591	Option EN102720:4 ETH EN101934	Option EN102720:5 OSC27 EN101608	Option EN102720:6 OSC24 EN101221
Variant EN102674:0 ME-XU8-5EV-1I-D12E-R2.1	Option EN102674:1 FPGA EN102159	Option EN102674:2 DDR4 EN101979	Option EN102674:3 EMMC EN102591	Option EN102674:4 ETH EN101934	Option EN102674:5 OSC27 EN101608	Option EN102674:6 OSC24 EN101221
Variant EN102676:0 ME-XU8-7EV-1E-D11E-R2.1	Option EN102676:1 FPGA EN102615	Option EN102676:2 DDR4 EN101868	Option EN102676:3 EMMC EN102591	Option EN102676:4 ETH EN101934	Option EN102676:5 OSC27 EN101608	Option EN102676:6 OSC24 EN101221
Variant EN102675:0 ME-XU8-7EV-2I-D12E-R2.1	Option EN102675:1 FPGA EN102160	Option EN102675:2 DDR4 EN101979	Option EN102675:3 EMMC EN102591	Option EN102675:4 ETH EN101934	Option EN102675:5 OSC27 EN101608	Option EN102675:6 OSC24 EN101221

Component Variants

OSC25	OSC33	OSC100	L0U68	L1U5	L2U2	L_VCC_INT	SEC_EEPROM	VCC_INT_VCU
Part Y1601A ASDMB-25.000MHZ-LC-T EN101588	Part Y1600A ASDMB_33.333MHZ-LC-T EN100285	Part Y300A ASDMB-100.000MHZ-LY-T EN100284	Part L1701A 0.68uH EN102112	Part L1700A 1u5 EN102613	Part L1900A 2u2 EN102185	Part L1702A 0u1 EN102190	Part U1505A ATSHA204A-MAHDA-T EN100827	R604 or R607
Part Y1601B ASEMB_25.000MHZ-LC-T EN101589	Part Y1600B ASEMB_33.333MHZ-LC-T EN100914		Part L1701B 0.68uH EN102445	Part L1700B 1u5 EN102207	Part L1900B 2u2 EN102208	Part L1702B 220n EN102189	Part U1505B DS28CN01U-A00+ EN100280	C731, C736, C740, C743, C746, C749 or DNE
			Part L1800A 0.68uH EN102112		Part L1900C 2u2 EN101680			
			Part L1800B 0.68uH EN102445					
			Part L1801A 0.68uH EN102112					
			Part L1801B 0.68uH EN102445					

Assembly Variants

OSC25	OSC33	OSC100	L0U68	L1U5	L2U2	L_VCC_INT	SEC_EEPROM	VCC_INT_VCU
Option EN102673:7 OSC25 EN101588	Option EN102673:8 OSC33 EN100914	Option EN102673:9 OSC100 EN100284	Option EN102673:10 L0U68 EN102112	Option EN102673:11 L1U5 EN102207	Option EN102673:12 L2U2 EN102185	Option EN102673:13 L_VCC_INT EN102190	Option EN102673:14 SEC_EEPROM EN100827	Option EN102673:15 VCC_INT_VCU DNE
Option EN102720:7 OSC25 EN101588	Option EN102720:8 OSC33 EN100914	Option EN102720:9 OSC100 EN100284	Option EN102720:10 L0U68 EN102112	Option EN102720:11 L1U5 EN102207	Option EN102720:12 L2U2 EN102185	Option EN102720:13 L_VCC_INT EN102190	Option EN102720:14 SEC_EEPROM EN100827	Option EN102720:15 VCC_INT_VCU DNE
Option EN102674:7 OSC25 EN101588	Option EN102674:8 OSC33 EN100914	Option EN102674:9 OSC100 EN100284	Option EN102674:10 L0U68 EN102112	Option EN102674:11 L1U5 EN102207	Option EN102674:12 L2U2 EN102185	Option EN102674:13 L_VCC_INT EN102190	Option EN102674:14 SEC_EEPROM EN100827	Option EN102674:15 VCC_INT_VCU
Option EN102676:7 OSC25 EN101588	Option EN102676:8 OSC33 EN100914	Option EN102676:9 OSC100 EN100284	Option EN102676:10 L0U68 EN102112	Option EN102676:11 L1U5 EN102207	Option EN102676:12 L2U2 EN102185	Option EN102676:13 L_VCC_INT EN102190	Option EN102676:14 SEC_EEPROM EN100827	Option EN102676:15 VCC_INT_VCU
Option EN102675:7 OSC25 EN101588	Option EN102675:8 OSC33 EN100914	Option EN102675:9 OSC100 EN100284	Option EN102675:10 L0U68 EN102112	Option EN102675:11 L1U5 EN102207	Option EN102675:12 L2U2 EN102185	Option EN102675:13 L_VCC_INT EN102190	Option EN102675:14 SEC_EEPROM EN100827	Option EN102675:15 VCC_INT_VCU