The protocol is based on UART with RS-485 physical interface.
The controler board is the master and all other nodes are slaves.
Each bus transaction (read or write) constitutes three frames:

Physical device address (provided by master)
Internal register address (provided by master)
Data (provided by master in a write operation and by slave in a read operation)

8-bit Device Address							
7	6	5	4	3	2	1	0

Each physical device has one or more addresses in range 1-255.
Address 0 is reserved.

7-bit Register Address							
R/W	6	5	4	3	2	1	0

Each physical device has up to 128 registers with addresses 0-127.
The MSB of the register address represents a Read (=1) or Write (=0) operation.
After writing the register address by the master, the MSB determines if it is a read or a write operation.

Timing

Master and slaves agree on a specific baud rate (e.g., 9600bps) and 1 cycle=1/(baud rate)
Maximum bus idle time between consecutive frames of a transaction is 2*10=20 cycles
If the next frame of a bus transaction does not appear after this time => reset bus

On/Off Light

Register Address	Bits							
	7	6	5	4	3	2	1	0
0	POL7 RW	POL6 RW	POL5 RW	POL4 RW	POL3 RW	POL2 RW	POL1 RW	POL0 RW
1	POL15 RW	POL14 RW	POL13 RW	POL12 RW	POL11 RW	POL10 RW	POL9 RW	POL8 RW

Writing a '1' to POLn bit turns light switch n to turn on and vice versa.
Reading from POLn bit returns the current status of the light switch n.

Dimmer

Register Address	Bits 7	6	5	4	3	2	1	0
0	DM0_7 RW	DM0_6 RW	DM0_5 RW	DM0_4 RW	DM0_3 RW	DM0_2 RW	DM0_1 RW	DM0_0 RW
1	DM1_7 RW	DM1_6 RW	DM1_5 RW	DM1_4 RW	DM1_3 RW	DM1_2 RW	DM1_1 RW	DM1_0 RW
…					…			
15	DM15_7 RW	DM15_6 RW	DM15_5 RW	DM15_4 RW	DM15_3 RW	DM15_2 RW	DM15_1 RW	DM15_0 RW

Writing a value 0<=x<=255 into register n (bits DMn_7-DMn_0) causes the light on (x/255)*100 %
Reading from register n (bits DMn_7-DMn_0) returns the dimmer status.