



## **LAB MANUAL**

# Digital Design & Computer Architecture (23EC1202)

## **I Year B.Tech Even Semester**

(CSE, CS & IT, AI & DS, ECE, EEE & IOT)

## List of Experiments

| S. No. | Name of the Experiment  |
|--------|---|
| 1.     | Introduction and Verification of logic gates                                    |
| 2.     | Design and Realization of logic Gates using universal Gates                     |
| 3.     | Combinational Circuit Based Car Security System                                 |
| 4.     | Participant selection in Competitions Using Multiplexer                         |
| 5.     | Digital Display of the Department Name using 7-segment decoder                  |
| 6.     | Design of Computational Processing System for Arithmetic and Logical Operations |
| 7.     | Random Number Generator for Gaming Using D-Flip- flop                           |
| 8.     | Digital Unlocking System using Shift Register                                   |
| 9.     | Design of 4-bit asynchronous counter  |
| 10.    | Implementation of Information Transmission System                               |
| 11.    | Development of Instruction Processing System from Fetching to Execution         |
| 12.    | Implementation of Cache Memory  |
| 13.    | Choice Based Control of Vending Machine   |
| 14.    | Implementation of 3-Stage Pipelining  |

## Lab Evaluation components

| Evaluation Component                   | Maximum Marks | Weightage |
|--|---------------|-----------|
| Continuous evaluation-<br>Lab exercise | 50            | 9         |
| Lab In semester Exam                   | 50            | 8         |
| Lab End semester Exam                  | 50            | 16        |

## Continuous Evaluation Lab exercise:

| Exp. No. | Date | Title of the Experiment | Pre-lab (5M) | Connections & Execution (20M) | Result & Analysis (20M) | Viva (5M) | Total Marks (50M) | Signature of the Faculty with date |
|----------|------|-------------------------|--------------|-------------------------------|-------------------------|-----------|-------------------|------------------------------------|
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## **EXPERIMENT – 1**

### **Introduction and Verification of Logic Gates**

**Aim:** Introduction to digital design lab- nomenclature of digital ICs, specifications, study of the data sheet, concept of VCC and ground, verification of the truth tables of logic gates using TTL ICs.

**Apparatus:** Digital IC Trainer kit, single strand wires, breadboard

| <b>Gates</b> | <b>IC NO.</b> |
|--------------|---------------|
| AND          | 7408          |
| OR           | 7432          |
| NAND         | 7400          |
| NOR          | 7402          |
| NOT          | 7404          |
| XOR          | 74136         |

#### **Pre-lab:**

##### **1. What is a logic gate?**

**Ans:** Logic gate is a physical device implementing a Boolean function and performs Logical operation on one or more logic inputs and produces a single logic output.

##### **2. What are universal gates?**

**Ans:** NAND and NOR gates are called universal gates as any type of logic gates or logic Functions can be implemented by these gates.

##### **3. What are basic gates?**

**Ans:** AND, OR, Not are called basic gates.

##### **4. What is the primary motivation for using Boolean algebra to simplify logic expressions?**

**Ans:** (1) Boolean algebra reduces the number of inputs required. (2) It will reduce number of gates (3) It makes easier to understand the overall function of the circuit.

**Theory:**

Logic gates are idealized or physical devices implementing a Boolean function, which it performs a logical operation on one or more logical inputs and produce a single output. In digital electronics, logic gates are fundamental building blocks used to perform logical operations on binary signals (0s and 1s). Depending on the context, the term may refer to an ideal logic gate, one that has for instance zero rise time and unlimited fan out or it may refer to anon-ideal physical device.

The main hierarchy is as follows:

1. Basic Gates
2. Universal Gates

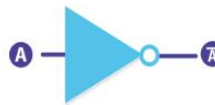
The symbols and truth tables of logic gates are shown in below figure.

**AND GATE**

| A | B | Output |
|---|---|--------|
| 0 | 0 | 0      |
| 0 | 1 | 0      |
| 1 | 0 | 0      |
| 1 | 1 | 1      |

**OR GATE**

| A | B | Output |
|---|---|--------|
| 0 | 0 | 0      |
| 0 | 1 | 1      |
| 1 | 0 | 1      |
| 1 | 1 | 1      |

**NOT GATE**

| A | $\bar{A}$ |
|---|-----------|
| 0 | 1         |
| 1 | 0         |

**BUFFER**

| Input | Output |
|-------|--------|
| 0     | 0      |
| 1     | 1      |

**NAND GATE**

| A | B | Output |
|---|---|--------|
| 0 | 0 | 1      |
| 0 | 1 | 1      |
| 1 | 0 | 1      |
| 1 | 1 | 0      |

**NOR GATE**

| A | B | Output |
|---|---|--------|
| 0 | 0 | 1      |
| 0 | 1 | 0      |
| 1 | 0 | 0      |
| 1 | 1 | 0      |

**XOR GATE**

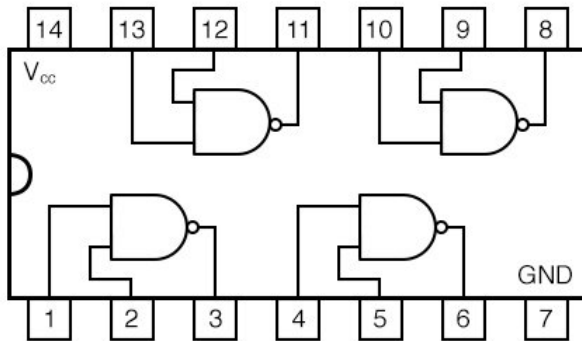
| A | B | Output |
|---|---|--------|
| 0 | 0 | 0      |
| 0 | 1 | 1      |
| 1 | 0 | 1      |
| 1 | 1 | 0      |

**XNOR GATE**

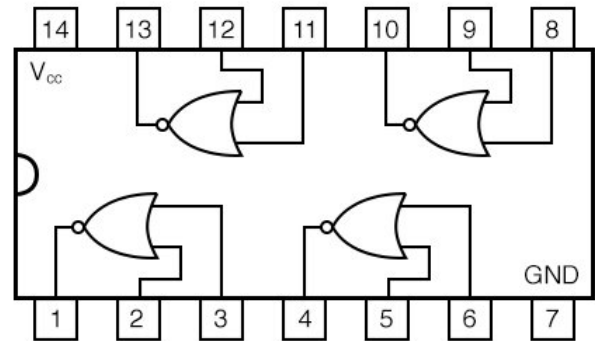
| A | B | Output |
|---|---|--------|
| 0 | 0 | 1      |
| 0 | 1 | 0      |
| 1 | 0 | 0      |
| 1 | 1 | 1      |

The IC numbers and pin diagrams of all logic gates are as shown below.

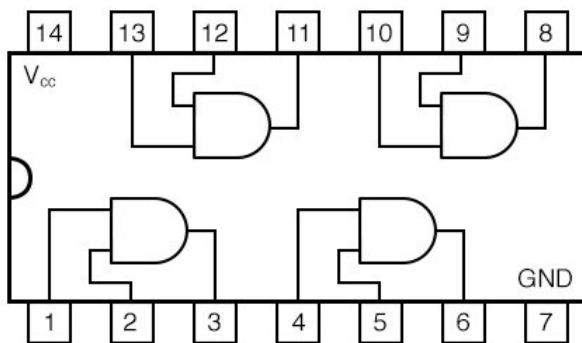
5400/7400  
Quad NAND Gate



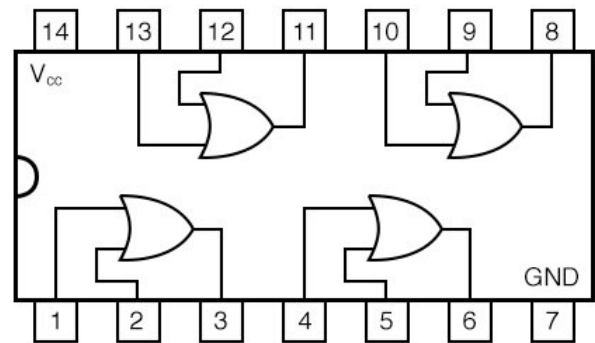
5402/7402  
Quad NOR Gate



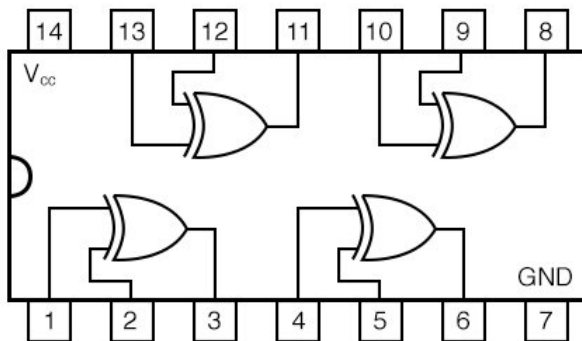
5408/7408  
Quad AND Gate



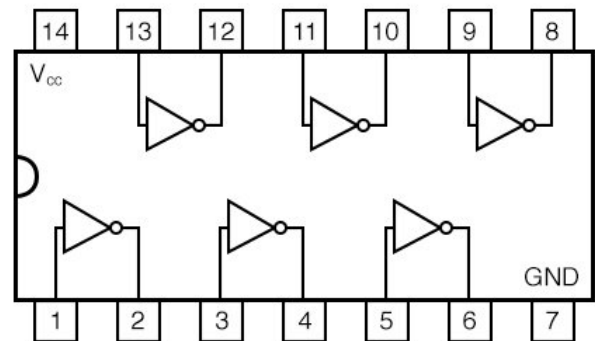
5432/7432  
Quad OR Gate



5486/7486  
Quad XOR Gate



5404/7404  
Hex Inverter



**Procedure:**

1. Place the breadboard gently on the observation table.
2. Fix the IC which is under observation between the half shadow line of breadboard, so there is no shortage of voltage.
3. Connect the wire to the main voltage source ( $V_{cc}$ ) whose other end is connected to last pin of the IC (14 place from the notch).
4. Connect the ground of IC (7th place from the notch) to the ground terminal provided on the digital lab kit.
5. Give the input at any one of the gates of the ICs i.e. 1st, 2nd, 3rd, 4th gate by using connecting wires. (In accordance to IC provided).
6. Connect output pins to the led on digital lab kit.
7. Switch on the power supply.
8. If led glows red then output is true, if it glows green output is false, which is numerically denoted as 1 and 0 respectively. The Color can change based on the IC manufacturer it's just verification of the Truth Table not the color change.

**Precautions:**

1. Connections must be tight on the bread board.
2. Identify the pins of the IC properly.
3. Take care while removing and inserting the IC on bread board.

**Viva Questions and answers:**

**Question 1:** Which of the logical operations is represented by the + sign in Boolean algebra?

**Answer:** OR gate.

**Question 2:** Which of the two input logic gate can be used to implement an inverter circuit?

**Answer:** Ex-NOR gate

**Question 3:** Which are the logic gates whose all output entries are logic 1 except for one entry there

is logic 0?

**Answer:** NAND and NOR gate

**Question 4:** Explain the concept of universal gates. Why are NAND and NOR gates considered universal?

**Answer:** Universal gates are logic gates that can be used to construct any other type of gate. NAND and NOR gates are considered universal because combinations of these gates can be used to implement AND, OR, and NOT gates, making them versatile in digital circuit design.

**Question 5:** How can the experiment results be applied in digital circuit design?

**Answer:** The experiment results demonstrate the practical application of universal gates in controlling outputs based on logical conditions. This understanding is fundamental in designing digital circuits and systems, where logical operations play a crucial role.

**Result:**

The experiment demonstrated the successful verification of all logic gates. The LEDs illuminated based on the logical conditions imposed by these logic gates.