EXPERIMENT – 14

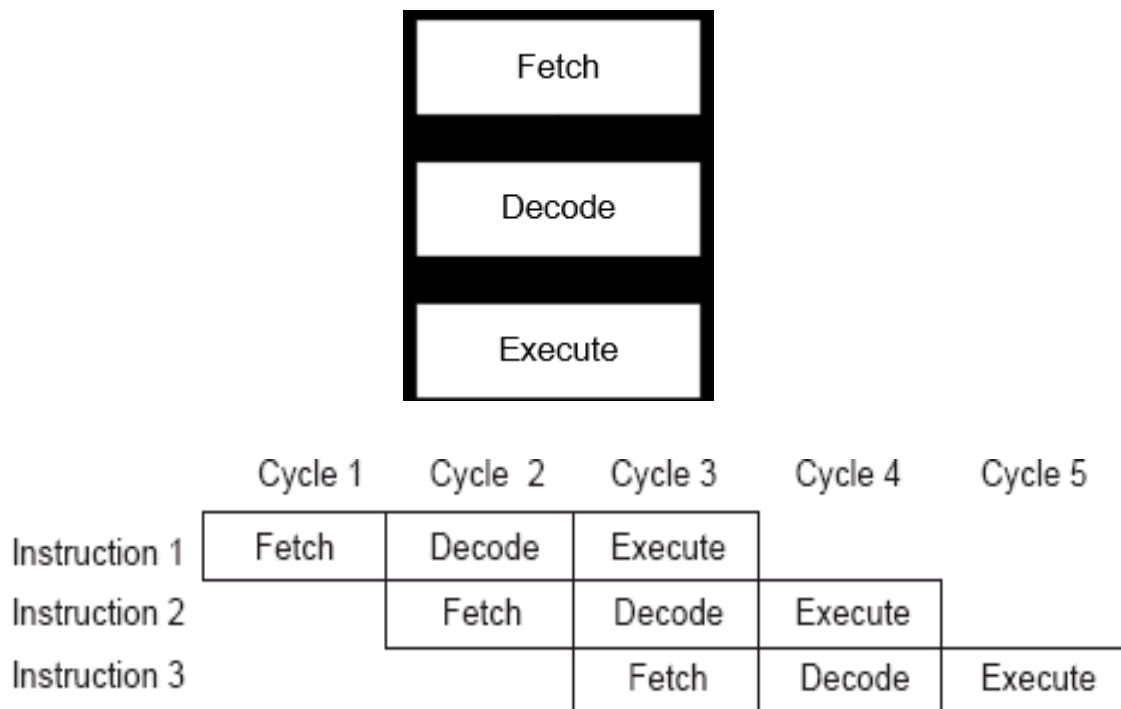## IMPLEMENTATION OF 3-STAGE PIPELINING

Aim: To implement 3-stage pipelining using Logisim.

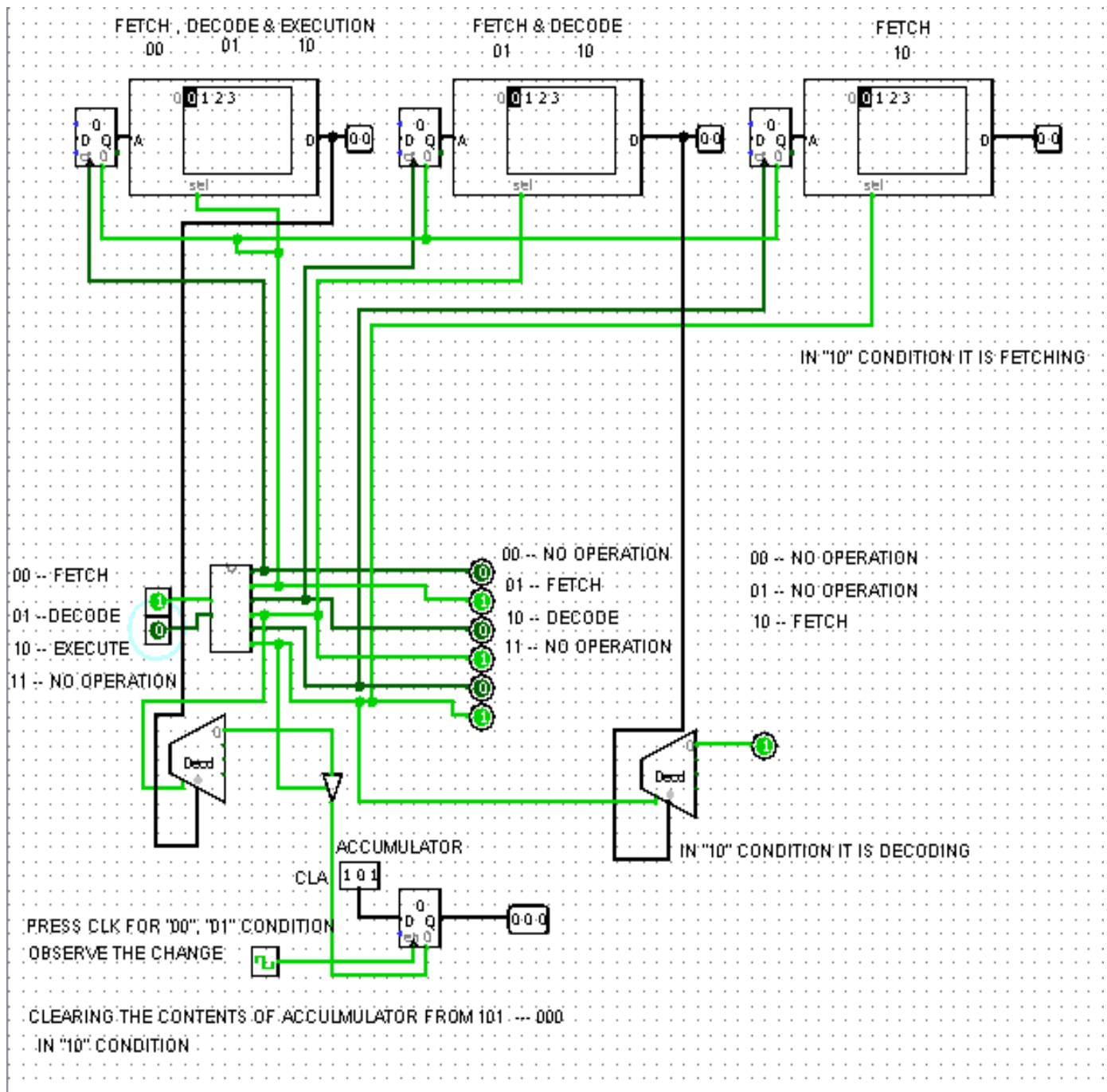**Tools Required:** Logisim

Components/devices can be used: Memories, decoders

Need and purpose:

Instruction pipelining is a technique for implementing instruction-level parallelism within a single processor. Pipelining attempts to keep every part of the processor busy with some instruction by dividing incoming instructions into a series of sequential steps performed by different processor units with different parts of instructions processed in parallel. It allows faster CPU throughput than would otherwise be possible at a given clock rate, but may increase latency due to the added overhead of the pipelining process itself.

Model Diagram / Table:

Circuit Diagram:

FETCH , DECODE & EXECUTION   FETCH & DECODE   FETCH
00   01   10   01   10   10

IN "10" CONDITION IT IS FETCHING

00 -- FETCH

01 --DECODE

10 -- EXECUTE

11 -- NO OPERATION

00 -- NO OPERATION   00 -- NO OPERATION

01 -- FETCH   01 -- NO OPERATION

10 -- DECODE   10 -- FETCH

11 -- NO OPERATION

IN "10" CONDITION IT IS DECODING

ACCUMULATOR

CLA 1 0 1

PRESS CLK FOR "00", "01" CONDITION

OBSERVE THE CHANGE

CLEARING THE CONTENTS OF ACCULMULATOR FROM 101 --- 000

IN "10" CONDITION

Procedure:

1. Analyse the given model diagram and select the required modules in Logisim.
2. Implement 3-stages fetch, decode and execute in pipelining.
3. Verify the operation of 3-stage pipelining using Logisim.

Result: The experiment successfully demonstrated the implementation of 3-stage pipelining using Logisim.