5.JFET CHARACTERISTICS

AIM

To study the **drain and transfer characteristics** of an n-channel Junction Field Effect Transistor (JFET) and to calculate its parameters such as **drain resistance (rd)**, **transconductance (gm)**, and **amplification factor (μ)**.

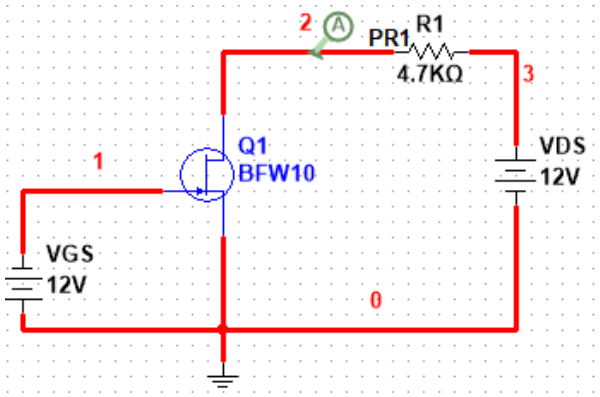
APPARATUS REQUIRED

S.No	Apparatus	Specification	Quantity
1	n-channel JFET (e.g., BF245 / 2N5457)	–	1
2	Regulated DC Power Supply (RPS)	0–30V, dual output	1
3	Digital/Analog Voltmeter	0–30V	2
4	Digital/Analog Ammeter	0–50 mA	1
5	Resistors	100 Ω, 1 kΩ (as per circuit)	2–3
6	Breadboard / Trainer Kit	–	1
7	Connecting Wires / Patch Cords	–	Required

PRE-LAB QUESTIONS

1. What is the basic construction and working principle of a JFET?
2. Define **pinch-off voltage (Vp)** and explain its significance.
3. What are the differences between **JFET and BJT**?
4. Explain the terms **IDSS** (Drain saturation current) and **VGS(off)** (Gate-source cut-off voltage).
5. Write the equation of the **transfer characteristic** of a JFET.
6. Why is the gate terminal of a JFET reverse biased?

Circuit Diagram:



PROCEDURE

A) Drain Characteristics (ID vs VDS at different VGS)

1. Keep VGS source as the secondary DC source (negative steps).
2. Go to Simulate → Analyses → DC Sweep.
3. Primary Source: Select VDS.

   Sweep from 0 V to 12 V (or higher up to 20 V).
4. Secondary Source (Nested): Select VGS.

   Sweep from 0 V to −5 V in steps (e.g., −1 V each).
5. In Grapher, plot -I(VDS source) vs VDS.

   This gives a family of drain curves for different gate voltages.

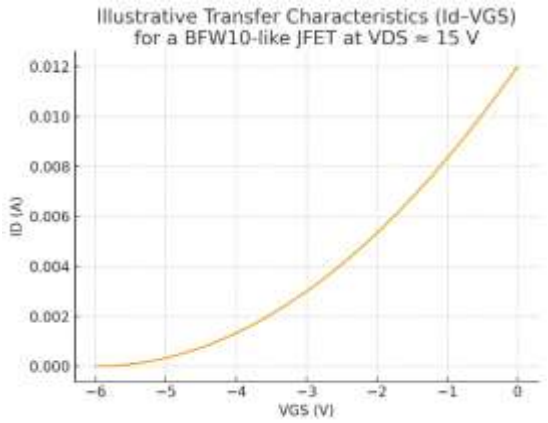
B) Transfer Characteristics (ID vs VGS at fixed VDS)

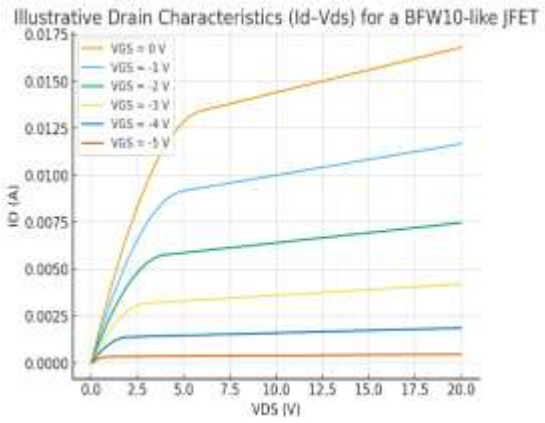
1. Fix VDS = 12 V (constant DC supply).
2. Go to Simulate → Analyses → DC Sweep.
3. Primary Source: Select VGS.

   Sweep from 0 V to −6 V (or until cutoff).
4. Plot -I(VDS source) vs VGS.

   This gives the transfer curve (parabolic Shockley type).

Expected Graphs:





POST-LAB TASKS

1. Plot the graphs neatly with proper scales and legends.
2. Calculate the values of **rd, gm, and μ** from the graphs.
3. Compare experimental values with theoretical expectations.
4. Discuss possible reasons for any deviations observed.

VIVA QUESTIONS

1. What are the advantages of JFET over BJT?
2. Why is the input impedance of JFET high?
3. Define **pinch-off region** and **saturation region** in a JFET.
4. What is the role of reverse-biased gate in JFET operation?
5. Explain the significance of **IDSS** and **VGS(off)** in determining JFET characteristics.
6. What happens to the drain current when **VGS** becomes more negative than **VGS(off)**?
7. Why is JFET considered a voltage-controlled device?

Evaluator Remark (if Any):	**Marks Secured: _____out of 50**
	Signature of the Evaluator with Date