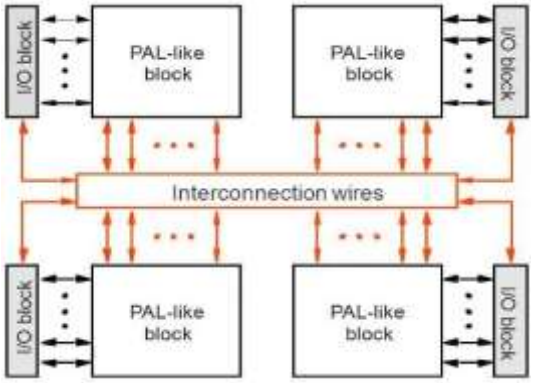
Simplify the expression F = A B D + A B' using Boolean identities.

F = A B D + A B'
= A (BD+B')
= A (B'+B)(B'+D)
= A (B'+D)

Represent the given expression in canonical POS form Y = (A + B)(B + C)(A + C)

Y = (A + B)(B + C)(A + C)
= (A+B+CC')(B+C+AA')(A+C+BB')
= (A+B+C)(A+B+C')(A+B+C)(A'+B+C)(A+B+C)(A+B'+C)
= $M_0.M_1.M_0.M_4.M_0.M_2$
= ΠM(0, 1, 2, 4)

Draw the architecture of a Complex Programmable Logic Device (CPLD) and its key components.



Reduce A (A + B) to the least number of terms.

= A (A + B) = AA + AB = A + AB = A (1+B) = A

Represent the given expression in canonical SOP form Y = AC + AB + BC.

= AC(B+B') + AB(C+C') + BC(A+A') [Since, C + C = 1]

= ABC + AB'C + ABC + ABC' + ABC + A'BC
= $m_7 + m_5 + m_7 + m_6 + m_7 + m_3$
= ∑m (3, 5, 6, 7)

Discuss the role of macro cells in CPLD architecture.

- The main building block of the CPLD is a macro cell. Macro cells are defined as functional blocks responsible for performing sequential or combinational logic.
- The macro cell consists of AND/OR array, Flip-flop, Multiplexer, XOR gate.

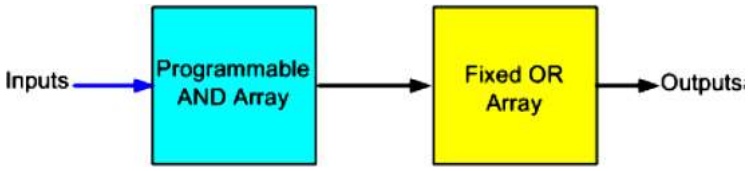
Apply De Morgan's theorems to simplify the expression: F = [(A+B)(C+D)]'

F = [(A+B)(C+D)]'
= (A+B)' + (C+D)'
= A'.B' + C'.D'

Develop a truth table that represents the Boolean equation. F = A'B'C + AB'C' + ABC' + ABC = ∑ m (1,4,6,7).

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Sketch a basic block diagram for a Programmable Array Logic (PAL) device.



Describe the concept of clocking in a flip-flop.
Clocking the flip-flop either to change or to retain its output signal based upon the values of the input signals at the transition.

Discuss the applications of shift registers in real- world scenarios.

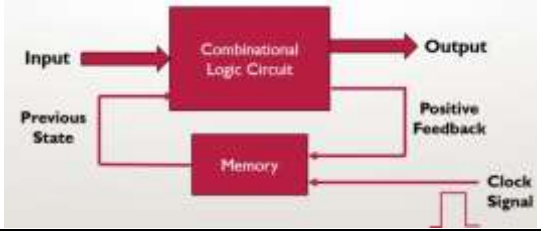
- Temporary data storage
- Data transfer
- Data manipulation
- As counters

Illustrate the purpose of a clear and reset pin on a shift register.

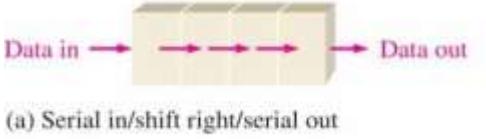
- The clear pin sets all bits in the shift register to a known state, often all zeros.
- The reset pin restores the shift register to its initial condition, clearing any stored data and preparing it for new input.

Outline the drawback of a JK flip-flop.
A race-around condition in a JK flip-flop occurs when both J and K inputs are set to 1 simultaneously, causing the flip-flop to oscillate rapidly between its states, leading to unpredictable behavior and potential damage to the circuit.

Draw the block diagram of a sequential circuit highlighting the feedback.



Describe the operation of a serial-in/serial-out shift register.



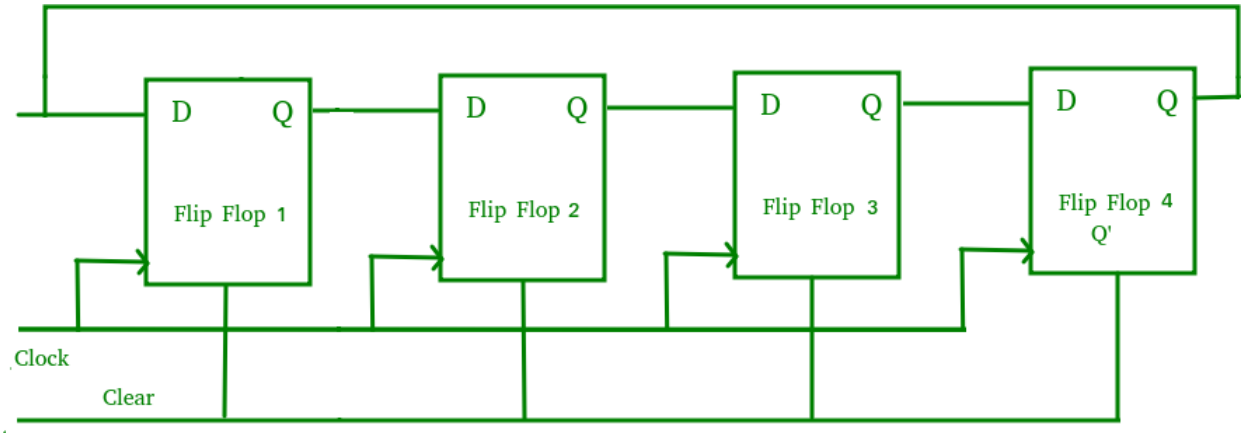
(a) Serial in/shift right/serial out

A serial-in/serial-out shift register is a type of shift register that allows data to be inputted serially (one bit at a time) and shifted out serially whenever a clock signal is applied.

Compare and contrast a Latch and Flipflop in controlling the logic of the system.

Latches	**Flip-flops**
Continuously checks its inputs and changes output accordingly.	Continuously checks its inputs and changes output at times determined by the clock signal.
Level Triggered	Edge Triggered
Requires Enable signal to function	Requires clock to function
Made up of Logic gate blocks	Made up of Latches and Logic gates

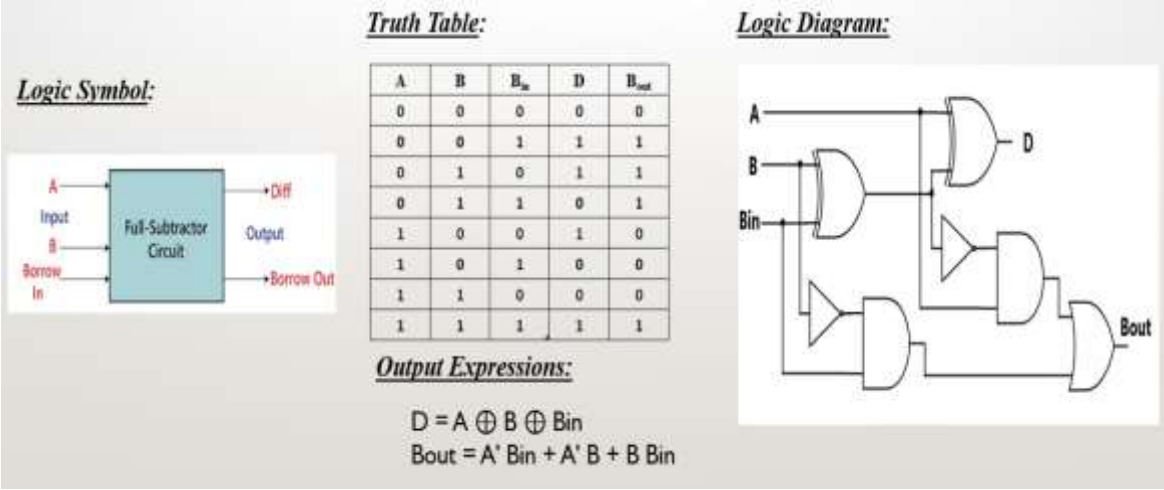
Illustrate the modelling diagram of a register using flip-flops.



List the different types of shift registers.

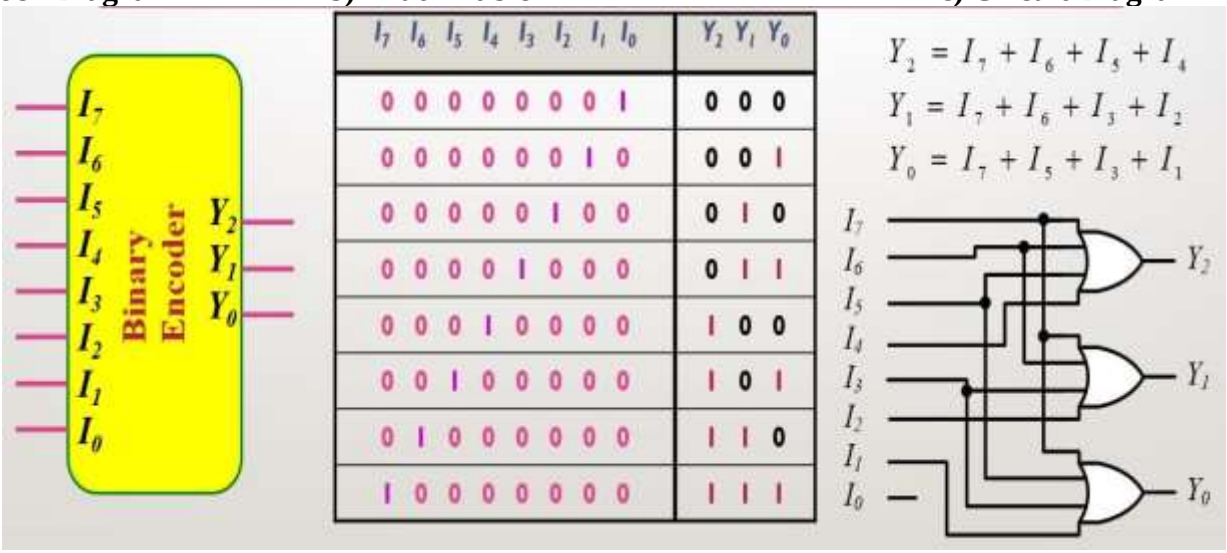
1. Serial In Serial Out (SISO)
2. Serial In Parallel Out (SIPO)
3. Parallel In Serial Out (PISO)
4. Parallel In Parallel Out (PIPO)

Describe the full subtractor using a block diagram, list its truth table and output equations.

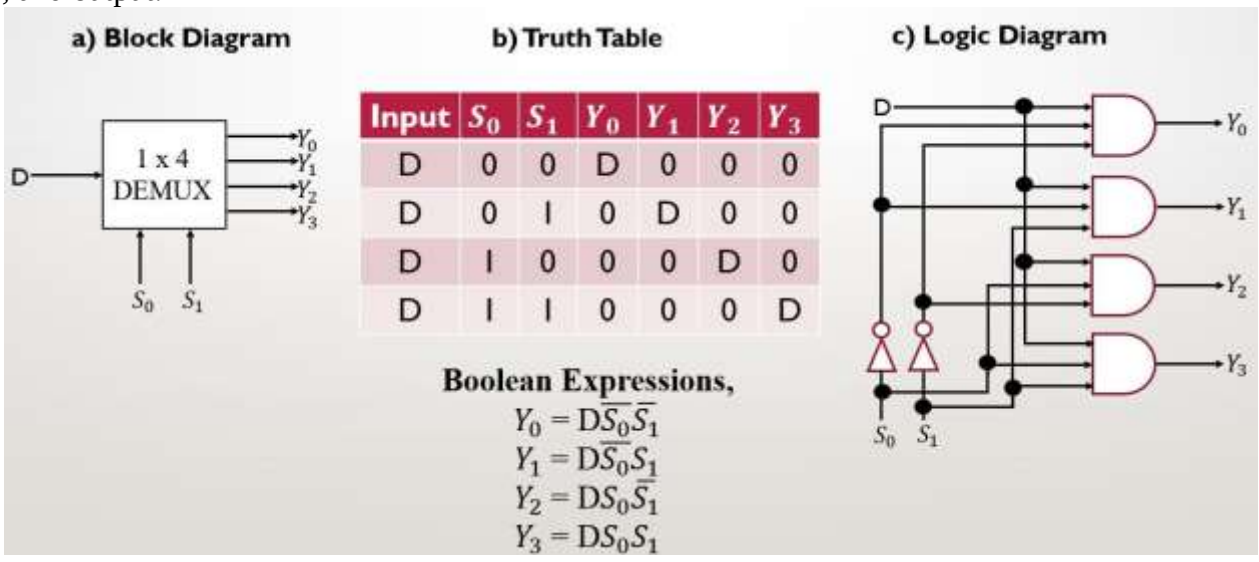


Design a circuit diagram for a 8-to-3 line encoder. Include input and output labels in your diagram.

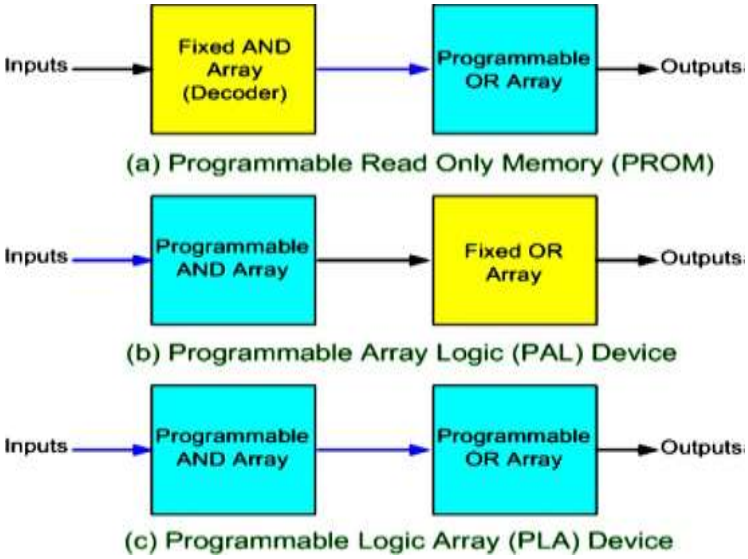
a) Block Diagram **b) Truth Table** **c) Circuit Diagram**



Provide a thorough description of the architecture of a 1:4 de-multiplexer, including its input lines, control lines, and output.



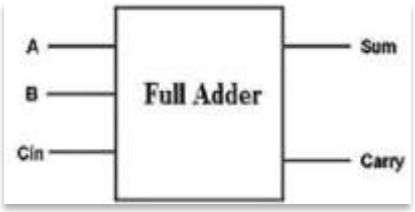
Compare and contrast PROM, PAL & PLA using schematic diagrams.



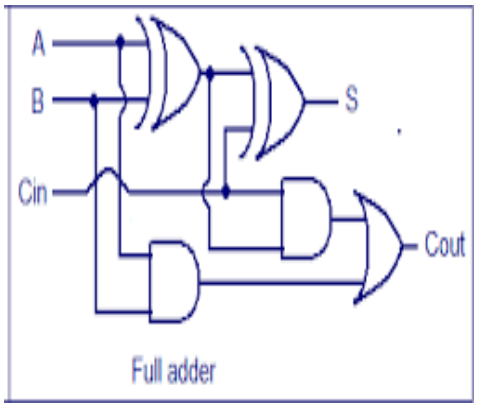
- The PROM (Programmable Read Only Memory) has a fixed AND array (constructed as a decoder) and programmable connections for the output OR gates array. The PROM implements Boolean functions in sum-of-min terms form.
- The PAL (Programmable Array Logic) device has a programmable AND array and fixed connections for the OR array.
- The PLA (Programmable Logic Array) has programmable connections for both AND and OR arrays. So it is the most flexible type of PLD.

Describe the full adder using a block diagram, list its truth table and output equations.

Block Diagram: **Truth Table:** **Circuit Diagram:**



A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

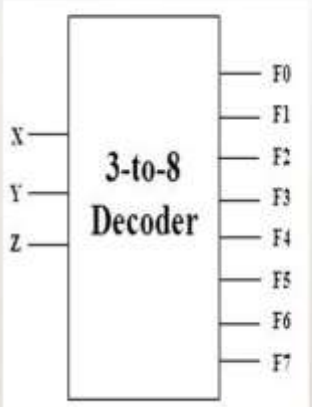


Output Expressions: **S**UM = ∑m(1,2,4,7) = A'.B'.C+A'.B.C'+A.B'.C'+A.B.C

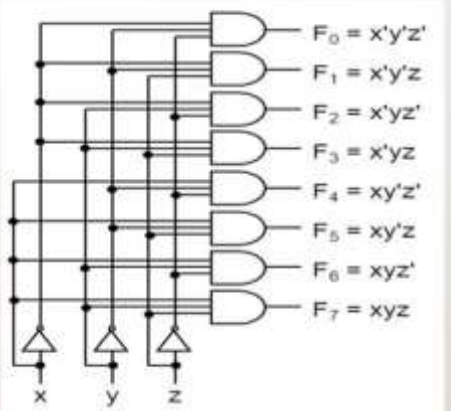
CARRY= ∑m(3,5,6,7) = A'.B.C+A.B'.C+A.B.C'+A.B.C

Design a circuit diagram for a 3-to-8 line decoder. Include input and output labels in your diagram.

Block Diagram **Truth Table** **Logic Diagram**



X	Y	Z	F7	F6	F5	F4	F3	F2	F1	F0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0



Differentiate the design aspects of combinational circuits compared to sequential circuits.

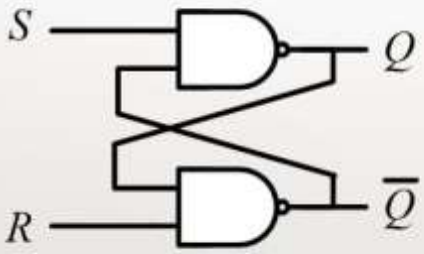
Feature	Combinational Circuits	Sequential Circuits
Dependency on Inputs	Output depends only on current inputs.	Output depends on both current inputs and past states.
Memory Elements	No memory elements.	Contains memory elements (e.g., flip-flops).
Output Determination	Determined instantly based on current inputs.	Determined by both current inputs and past states.
Feedback	No feedback from output to input.	May have feedback from output to input, allowing the circuit to store information.
Timing	No clock signal required.	Synchronized by a clock signal, operates in discrete clock cycles.
Examples	Logic gates, adders, multiplexers.	Flip-flops, registers, counters.
Speed	Typically faster as there is no reliance on clock cycles.	Speed can be limited by clock frequency and cycle time.

Illustrate the difference between a latch and a flip- flop.

Latches	Flip-flops
Continuously checks its inputs and changes output accordingly.	Continuously checks its inputs and changes output at times determined by the clock signal.
Level Triggered	Edge Triggered
Requires Enable signal to function	Requires clock to function
Made up of Logic gate blocks	Made up of Latches and Logic gates

Create the logic diagram for an SR latch and provide its truth table.

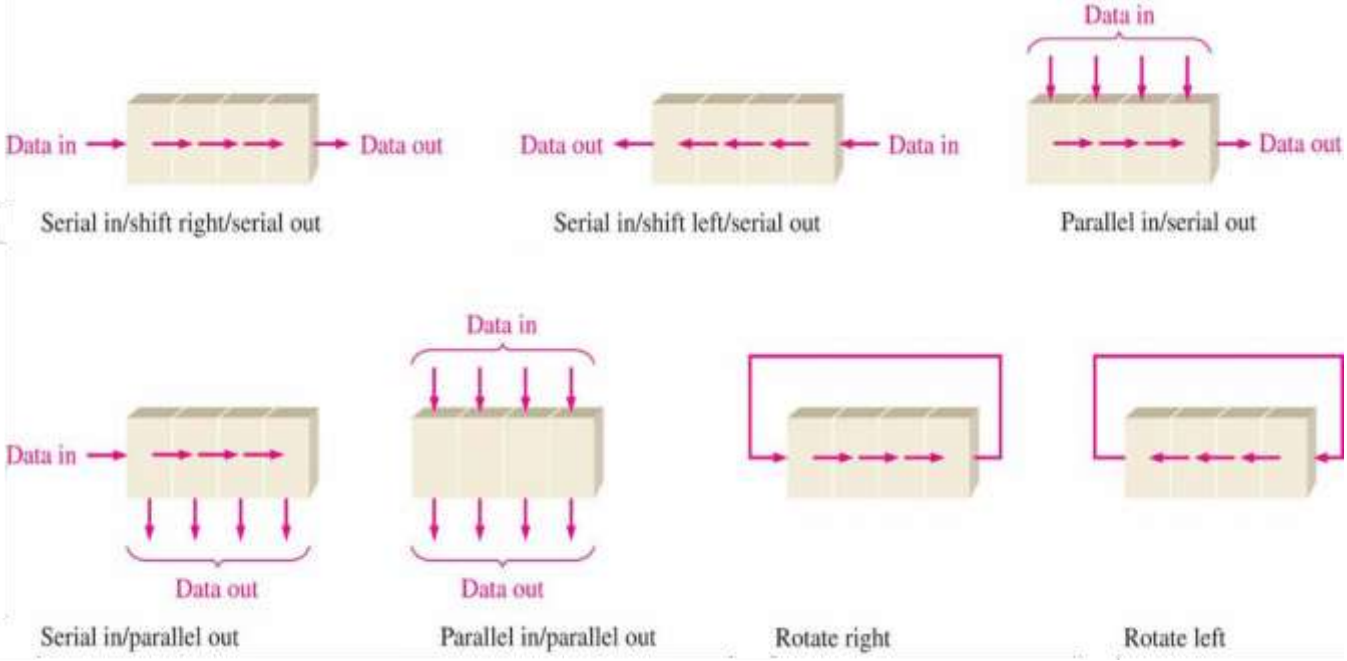
Logic diagram:



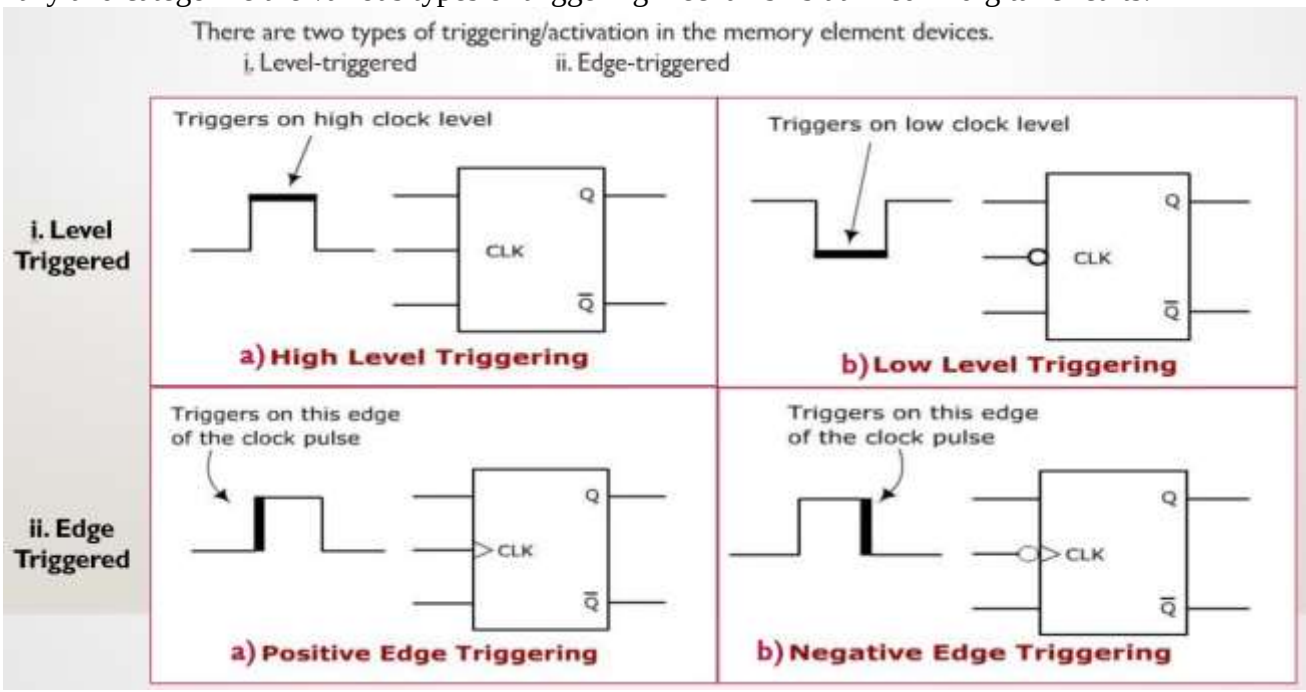
Truth Table:

S R	Q	
0 0	$Q=Q'=1$	Invalid
0 1	1	Set
1 0	0	Reset
1 1	Q_0	No change

Describe the different types of shifting operations that can be performed using shift registers.



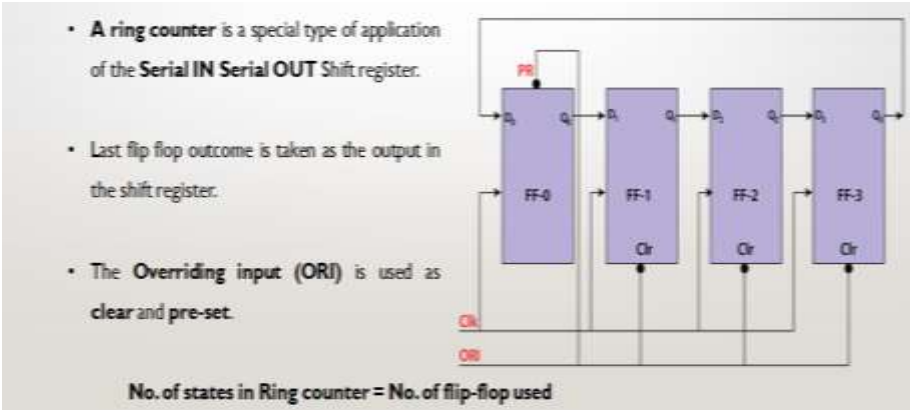
Identify and categorize the various types of triggering mechanisms utilized in digital circuits.



Compare and contrast the design considerations for synchronous and asynchronous sequential circuits.

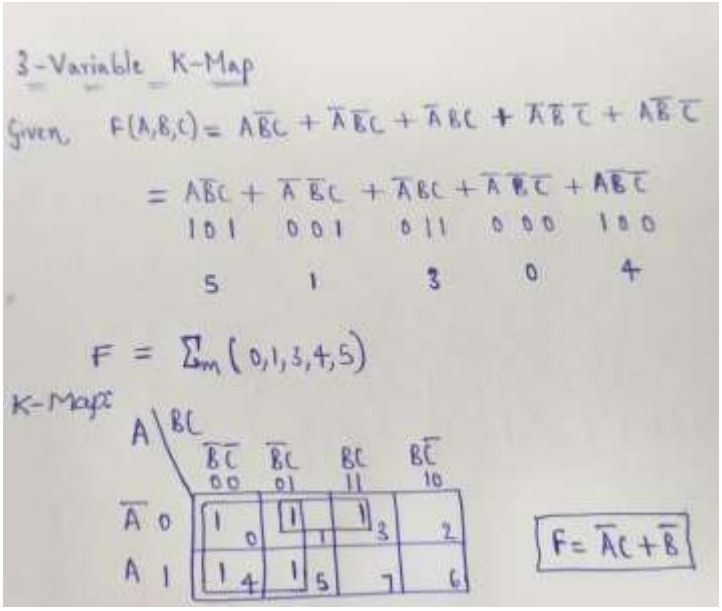
Synchronous sequential circuits	Asynchronous sequential circuits
Change their state only at specific intervals, dictated by a clock signal.	Do not rely on a clock signal for their operation, they change states immediately in response to changes in input.
Memory elements are clocked flip-flops	Memory elements are unclocked flip-flops or time delay elements.
Easier to design and Clock-Dependent Delay	More difficult to design & responds immediately to changes in input

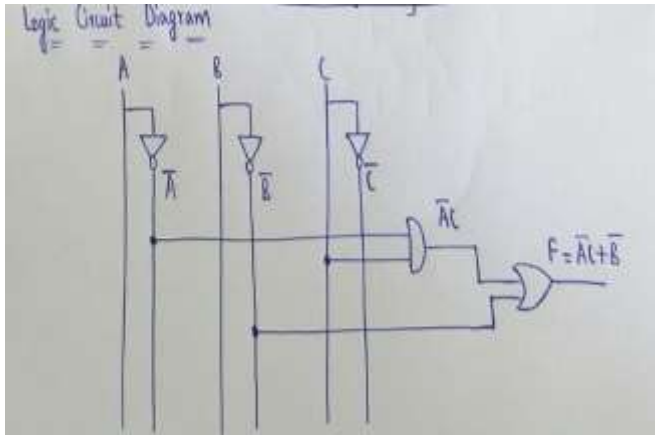
Design a 4-bit Ring Counter using D-flipflops and describe it's working.



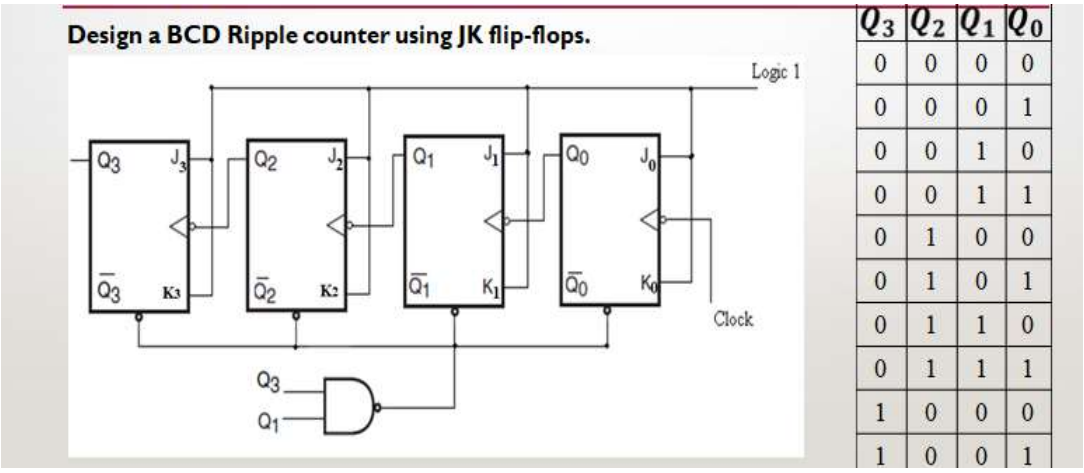
ORI	Clk	Q_0	Q_1	Q_2	Q_3
low	X	1	0	0	0
high	high	0	1	0	0
high	high	0	0	1	0
high	high	0	0	0	1
high	high	1	0	0	0

Optimize the equation F (A, B, C) = AB'C + A'B'C + A'BC + A'B'C' + AB'C' using K-Maps and realize the resultant expression using logic gates.



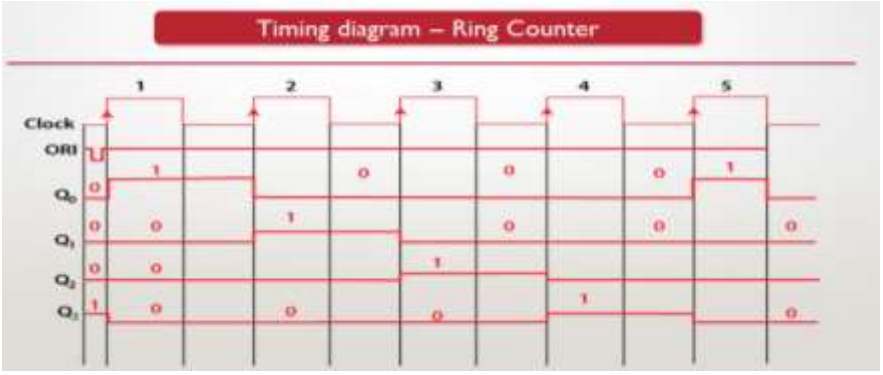


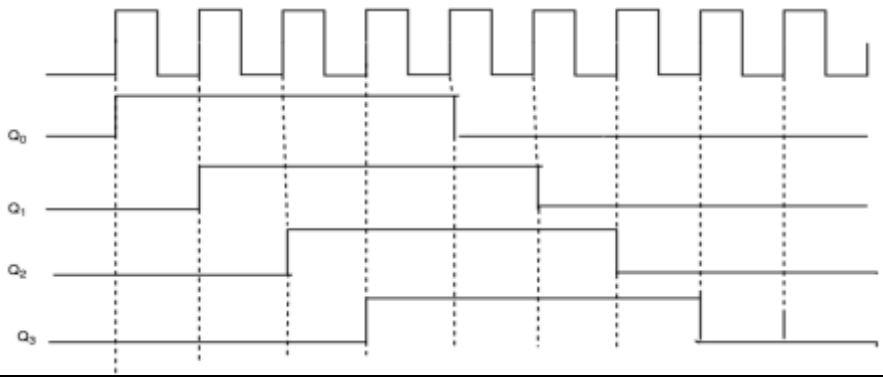
Develop the functioning of a BCD ripple counter using JK Flip-flops including truth table.



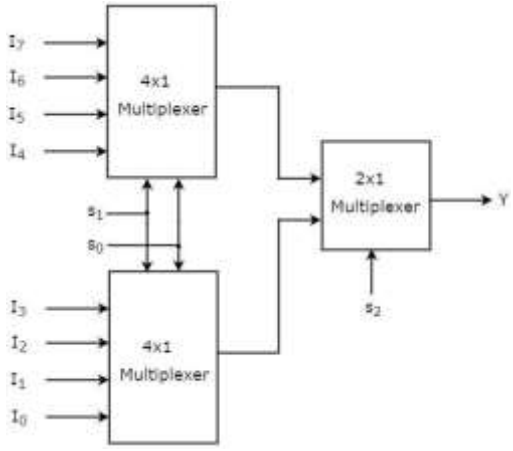
Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1

Draw the timing wave forms of Ring & Johnson counters for 4-bit in each case.



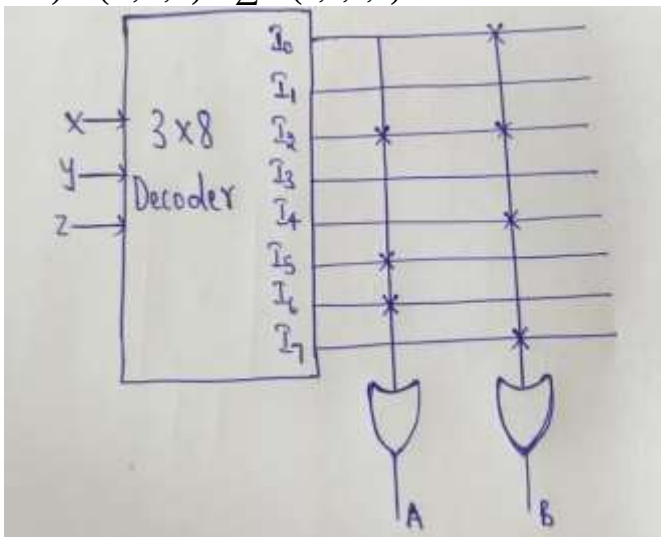


Design a 8:1 multiplexer using two 4:1 mux and one 2:1 mux.

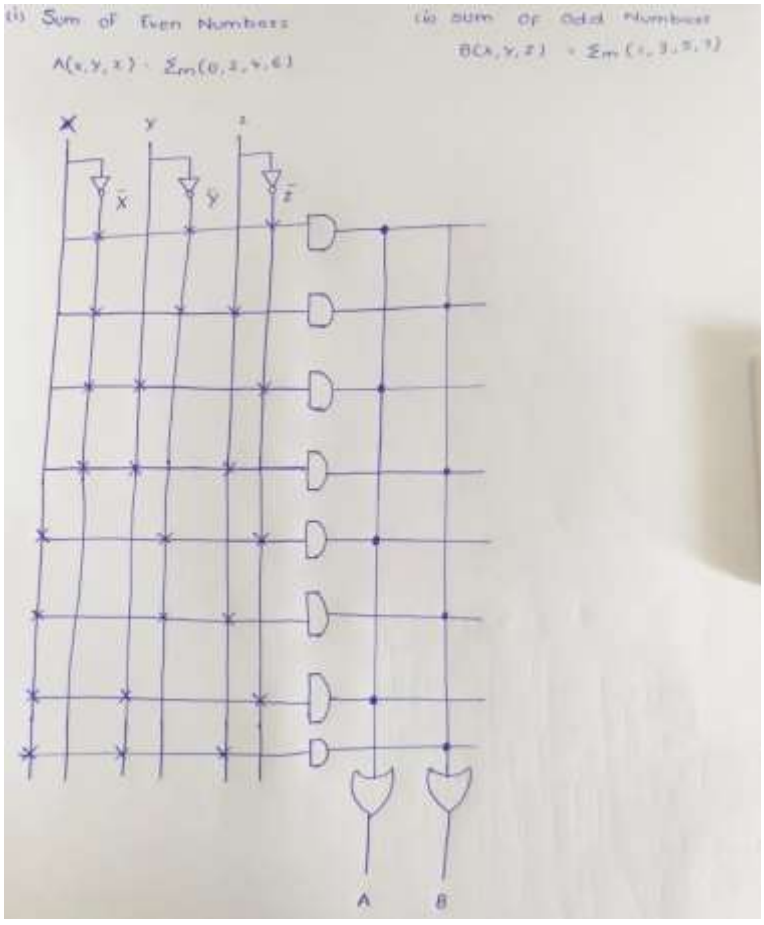


Design the following Boolean functions using PROM.

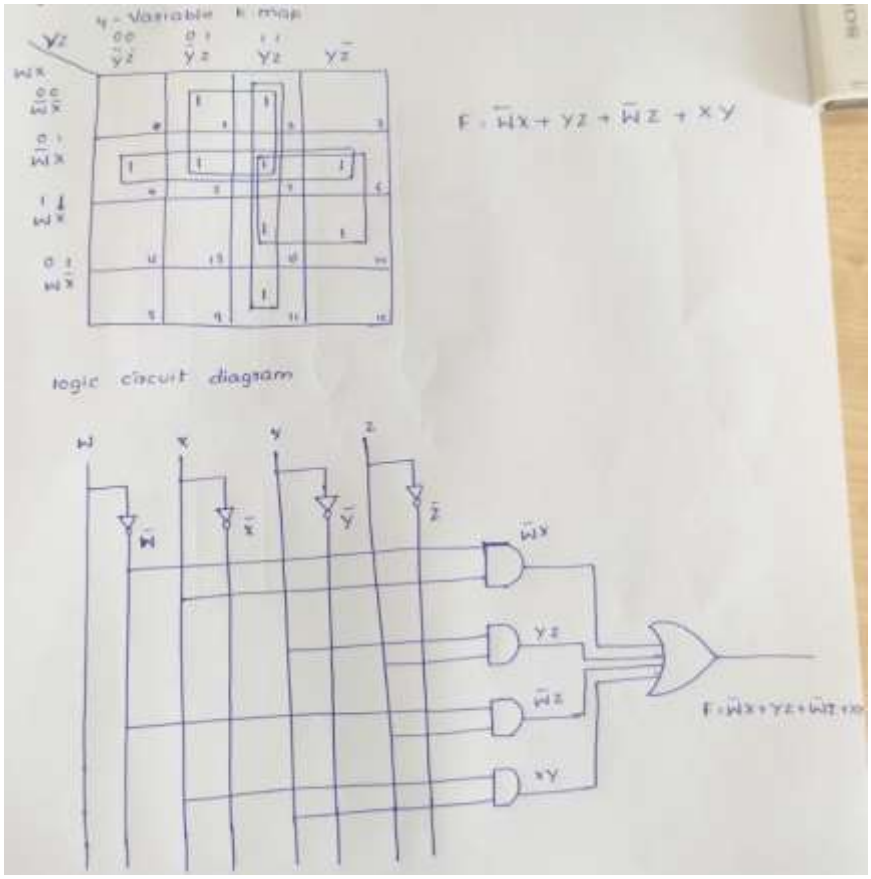
i) A (X,Y,Z) = ∑m (2,5,6) ii) B (X,Y,Z) = ∑m (0,2,4,7)



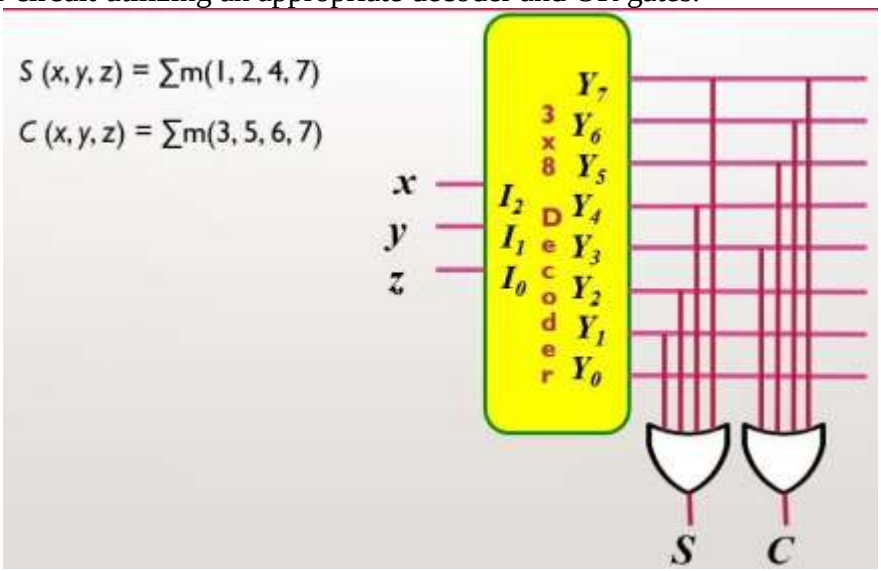
Design the following Boolean functions using PAL. A (X,Y,Z) = Sum of Even Numbers (include Zero also) and B (X,Y,Z) = Sum of Odd Numbers.



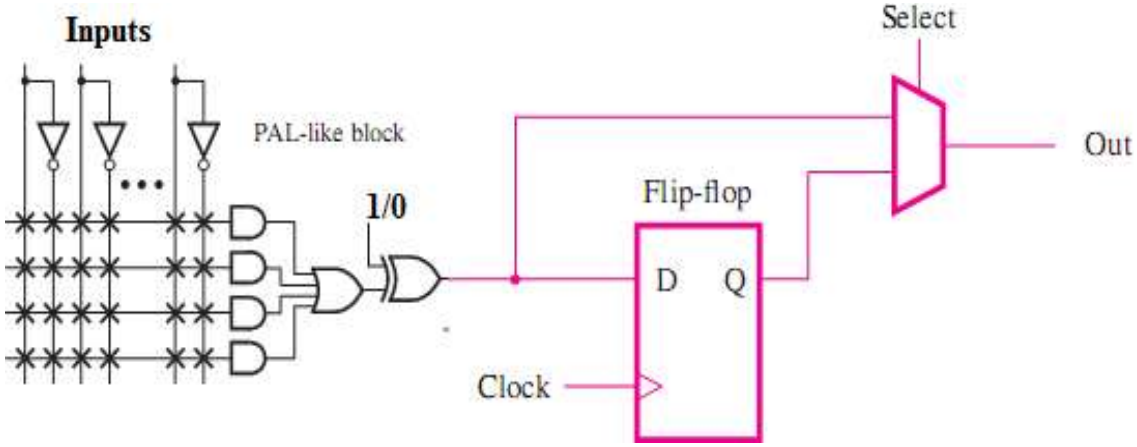
Optimize the given function using K-map F (W, X, Y, Z) = ∑m (1, 3, 4, 5, 6, 7, 11, 14, 15) and implement using logic gates.



Design a Full Adder circuit utilizing an appropriate decoder and OR gates.

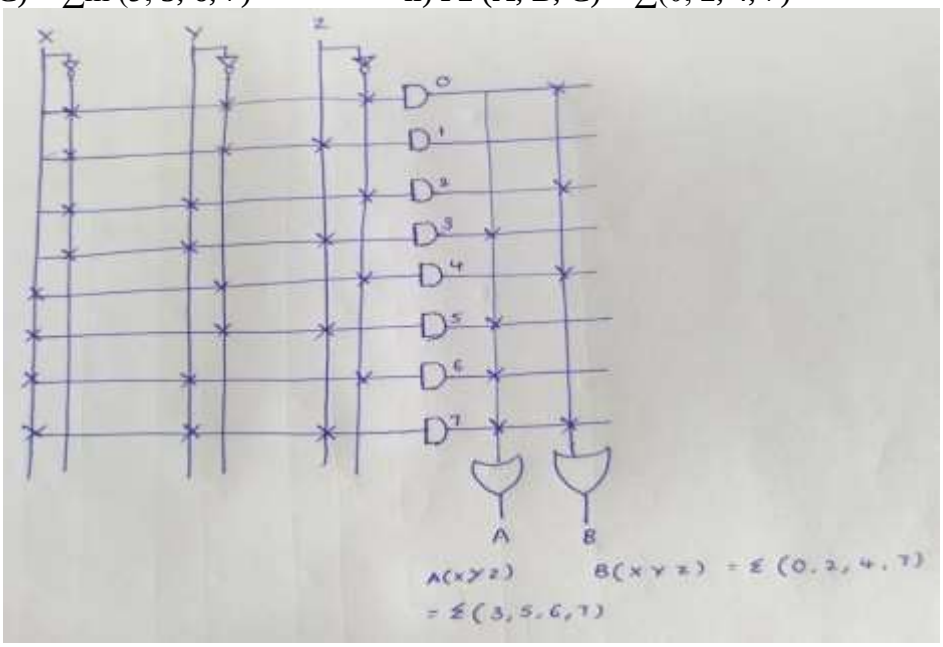


Illustrate the internal structure of Macro cell in CPLD using D Flip-flop and give the insights.

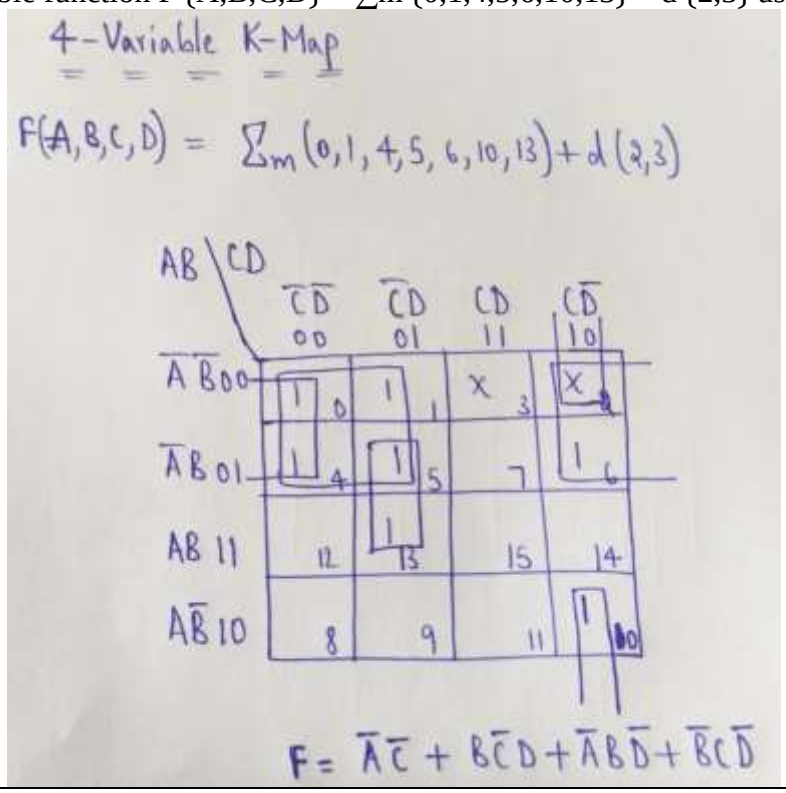


Design the circuit with a PLA having three inputs and two outputs.

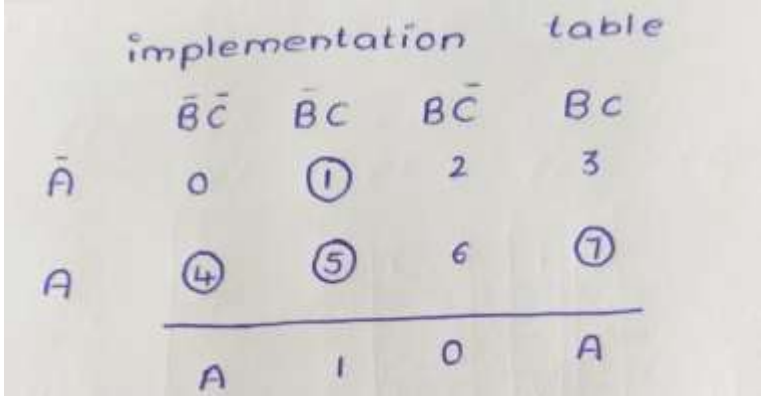
i) F1 (A, B, C) = ∑m (3, 5, 6, 7) ii) F2 (A, B, C) = ∑(0, 2, 4, 7)

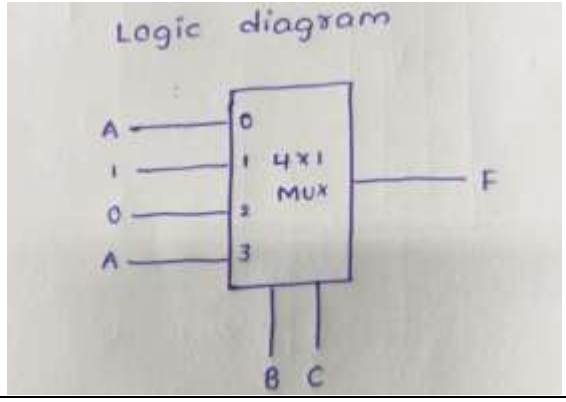


Optimize the four variable function F {A,B,C,D} = ∑m {0,1,4,5,6,10,13} + d {2,3} using K-Maps.



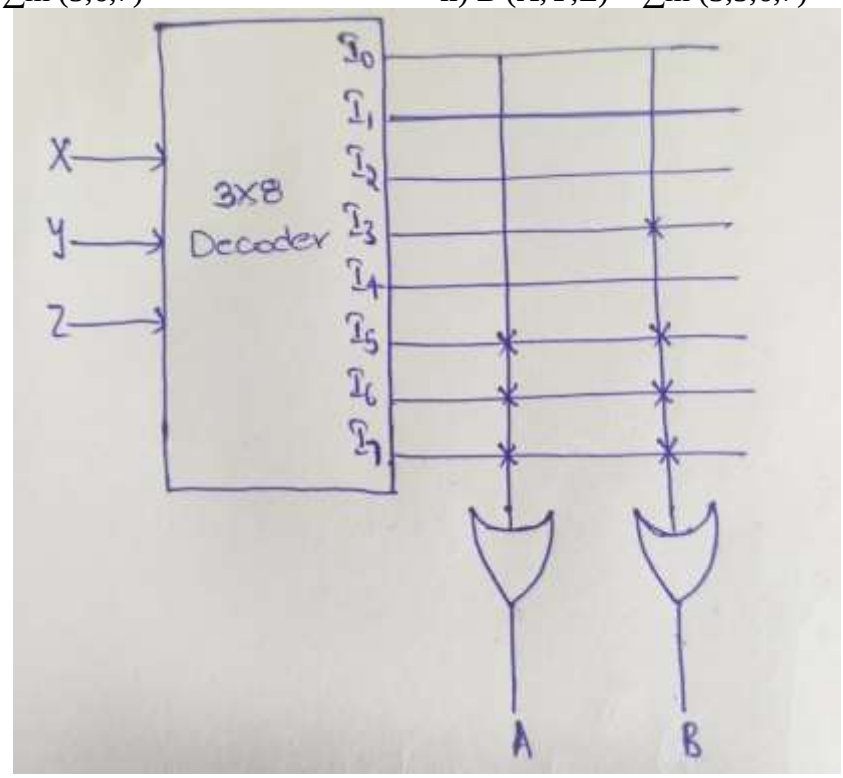
Design the function F(A,B,C) = ∑ m (1,4,5,7) using 4X1 MUX considering A as Input line and B, C as selection lines.





Design the following Boolean functions using PROM.

i) A (X,Y,Z) = ∑m (5,6,7) ii) B (X,Y,Z) = ∑m (3,5,6,7)

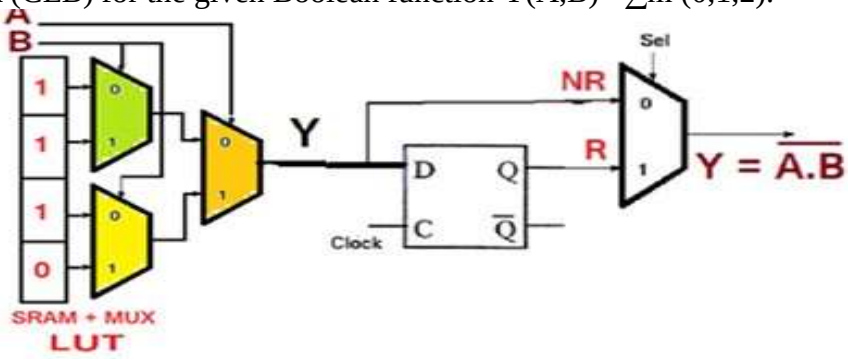


Design a Configurable Logic Block (CLB) for the given Boolean function Y(A,B)= ∑m (0,1,2).

FPGA: CLB

A	B	Σm	Y
0	0	0	1
0	1	1	1
1	0	2	1
1	1	3	0

NAND Gate



A	B	CLK	NR	R	SEL	Y
0	0	0	1	Z	0	1
0	1	0	1	Z	0	1
1	0	0	1	Z	0	1
1	1	0	0	Z	0	0
1	0	0	1	Z	1	Z

A	B	CLK	NR	R	SEL	Y
0	0	1	1	1	1	1
0	1	1	1	1	1	1
1	0	1	1	1	1	1
1	1	1	0	0	1	0
1	0	0	1	Z	0	1

Develop the T flip-flop, D flip-flop characteristics table and excitation table.

D Flip-flop

Characteristic Table:

D	Q(t)	Q(t+1)
0	0	0
0	1	0
1	0	1
1	1	1

Characteristic Equation:
Q(t+1) = D

Excitation Table:

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

T Flip-flop

Characteristic Table:

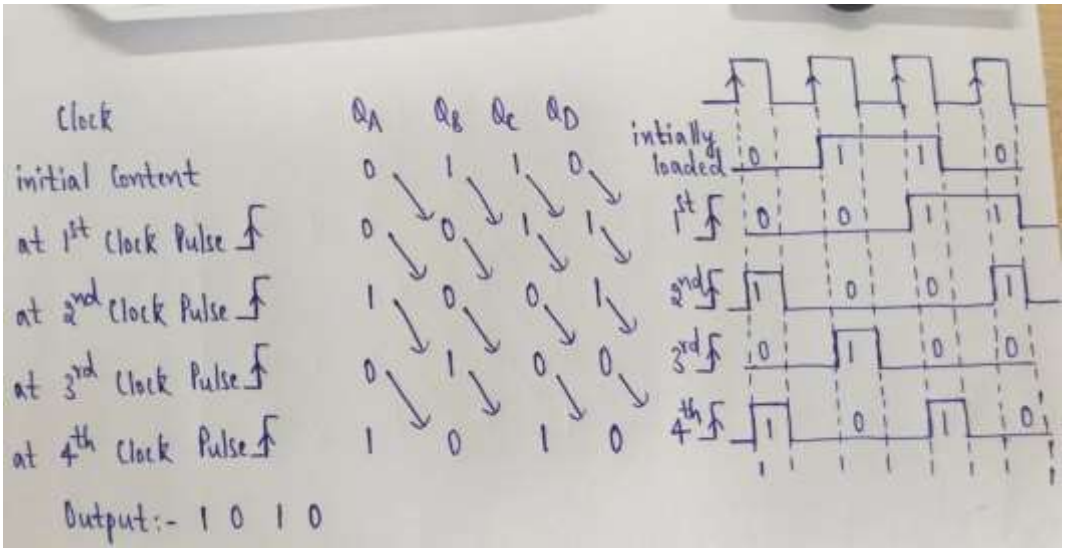
T	Q(t)	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Characteristic Equation:
Q(t+1) = T ⊕ Q

Excitation Table:

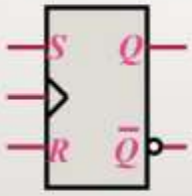
Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

Construct a 4-bit shift register that detects a specific bit pattern of "1010" in a serial input stream. Initially it starts with "0110".

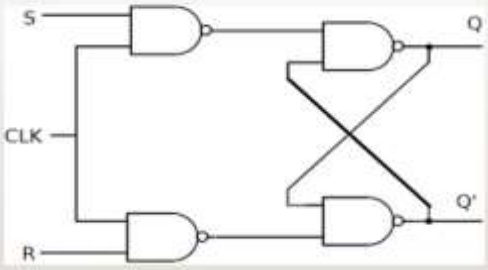


Describe the working principle of an SR Flip-Flop using a truth table and logic diagram.

Block diagram:



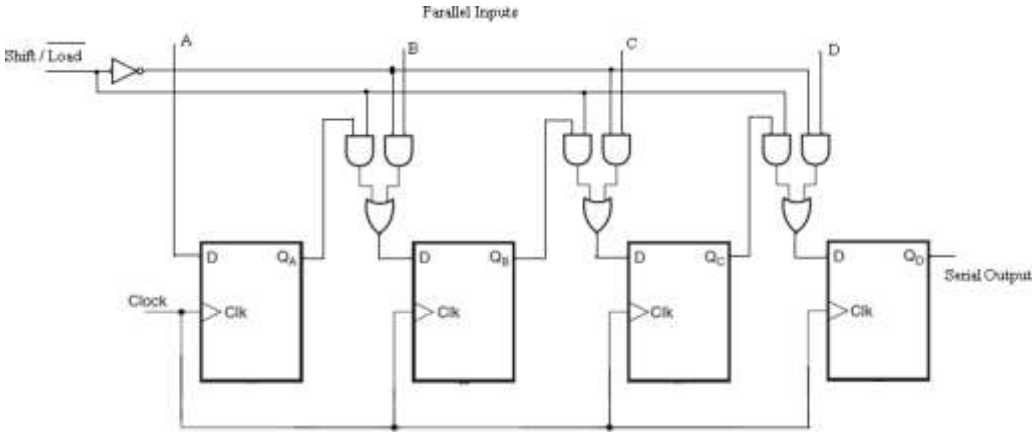
Logic diagram:



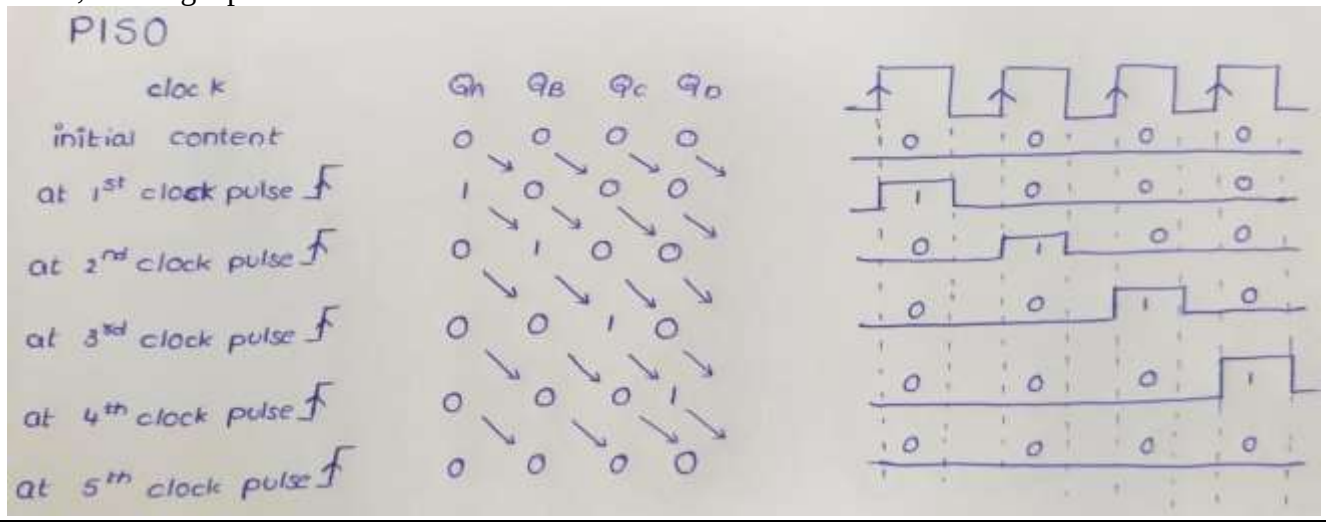
Truth Table:

S	R	Q (t+1)
0	0	Q (t)
0	1	0
1	0	1
1	1	Invalid

Design a 4-bit parallel-to-serial data converter using a PISO shift register.



S/L' = 0, Loading Operations,
S/L' = 1, Shifting Operations.



Develop the JK flip-flop characteristics table and excitation table.

Characteristic Table:

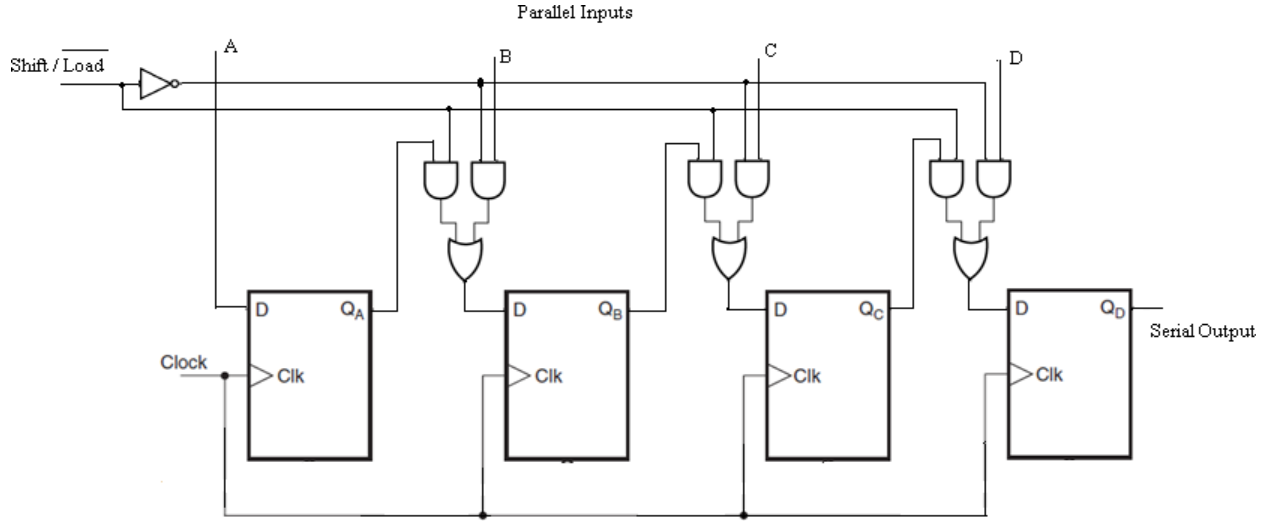
J	K	Q(t)	Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Characteristic Equation:
$Q(t+1) = JQ' + K'Q$

Excitation Table:

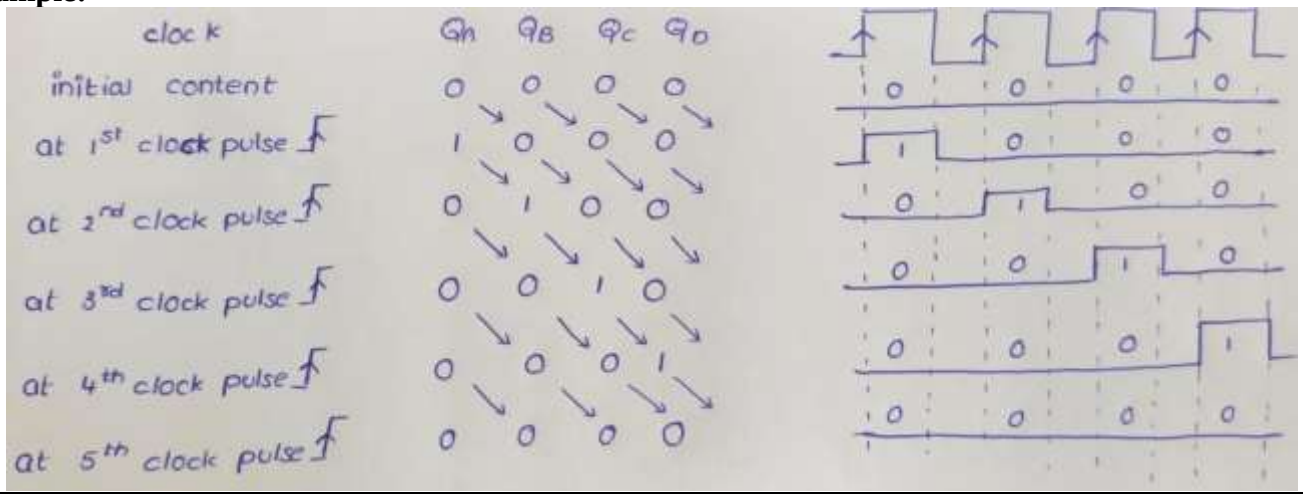
Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Design a 4-bit shift register setup that converts parallel input into serial output, specifically outputting the binary data pattern "1000".

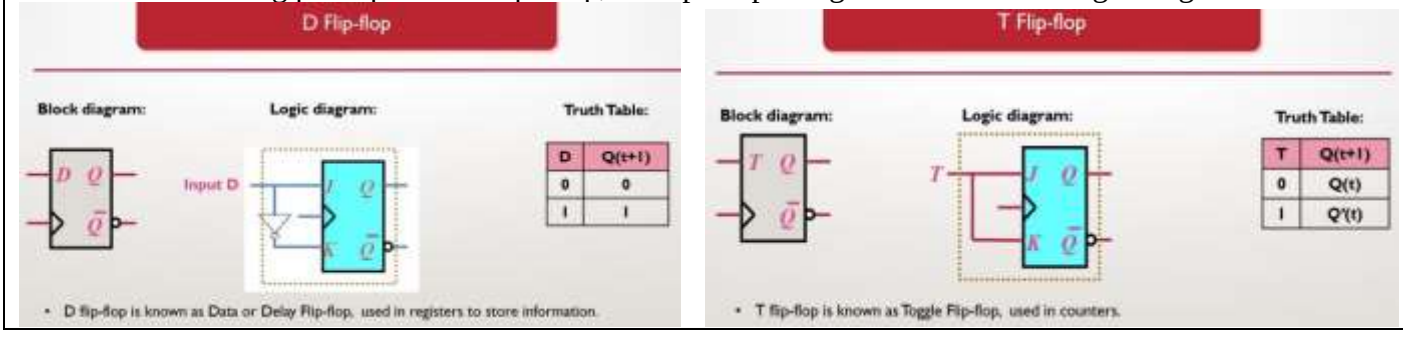


S/L' = 0, Loading Operations,
S/L' = 1, Shifting Operations.

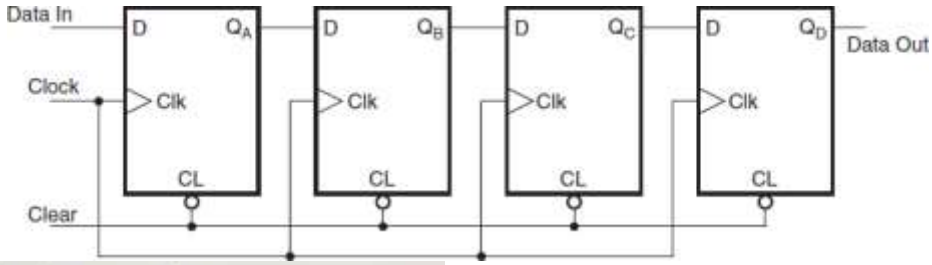
Example:

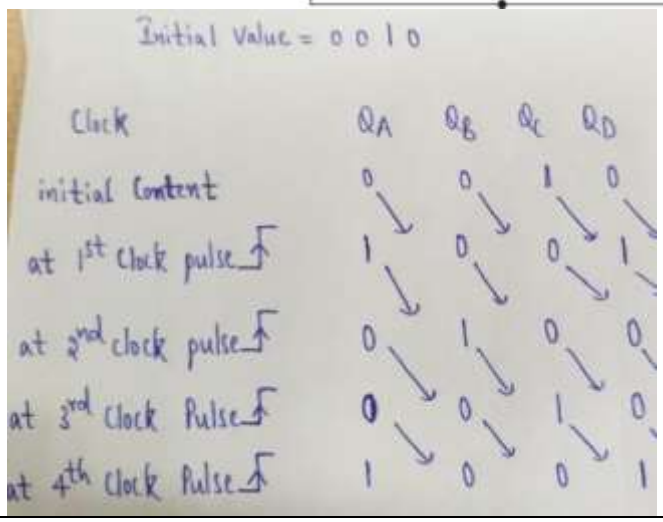


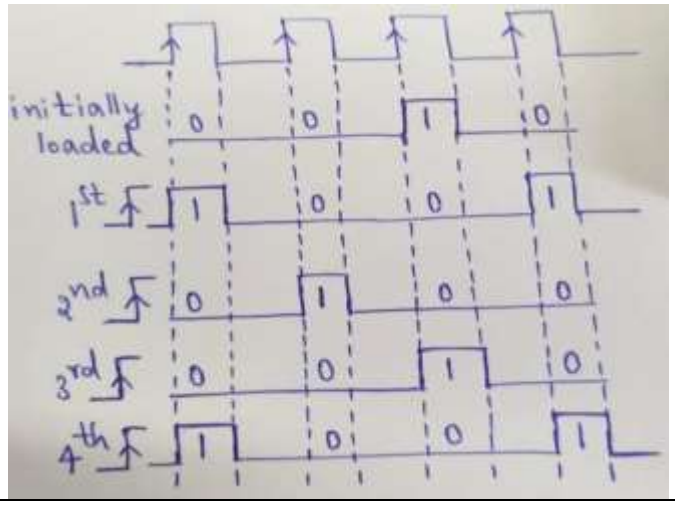
Describe the working principle of T Flip-Flop, D Flip-Flop using a truth table and logic diagram.



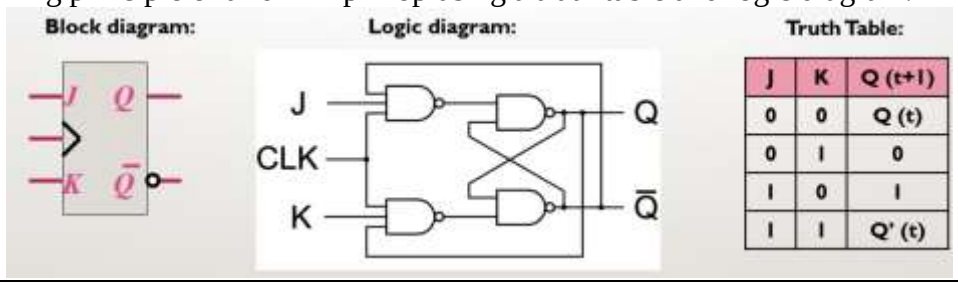
Design a 4-bit shift register capable of detecting the specific bit pattern "1001" within a serial input stream. The register should begin with the initial data "0010".







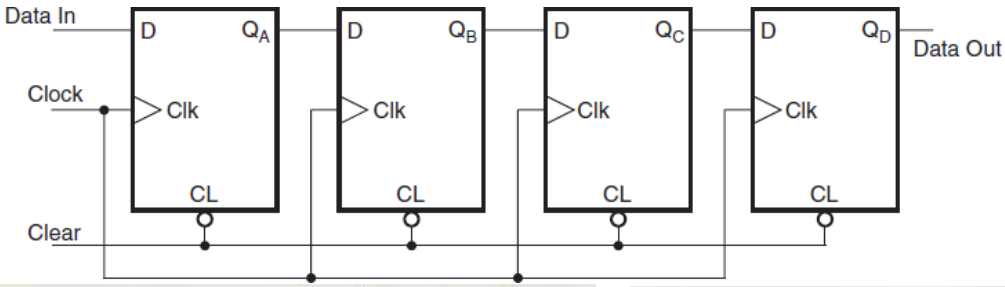
Describe the working principle of an JK Flip-Flop using a truth table and logic diagram.

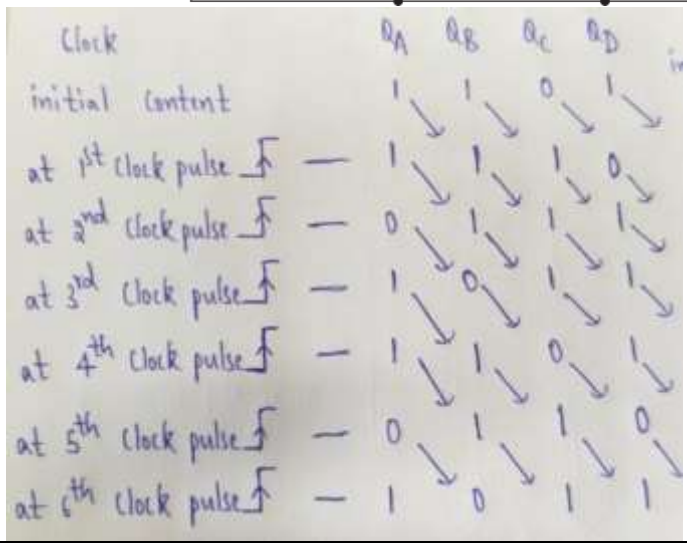


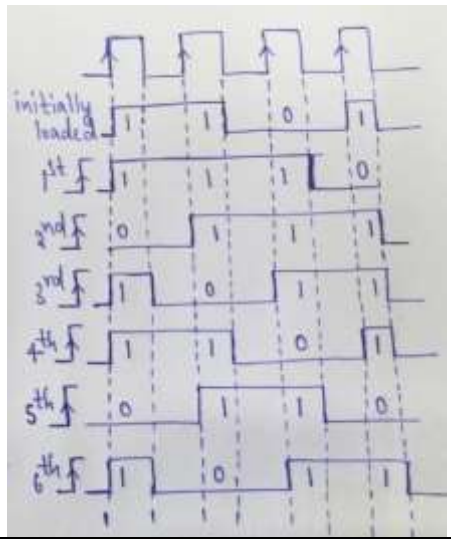
Truth Table:

J	K	Q (t+1)
0	0	Q (t)
0	1	0
1	0	1
1	1	Q' (t)

A 4-bit register is initially filled with the data "1101". The register is shifted six times to the right with the serial input being 101101. What is the content of the register after each shift?







Develop the SR flip-flop characteristics table and excitation table.

Characteristic Table:

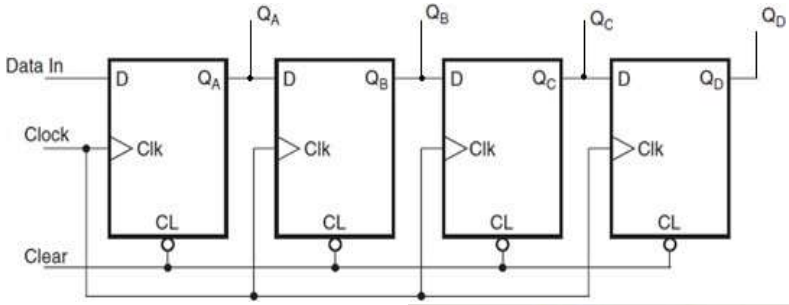
S	R	Q(t)	Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	Invalid
1	1	1	Invalid

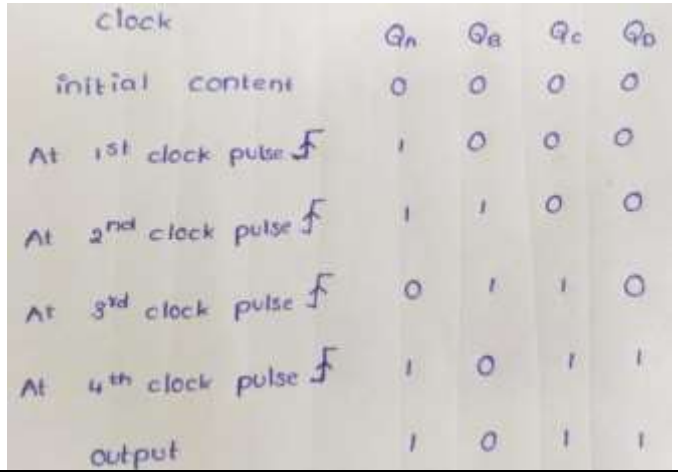
Characteristic Equation:
$Q(t+1) = S + R'Q$

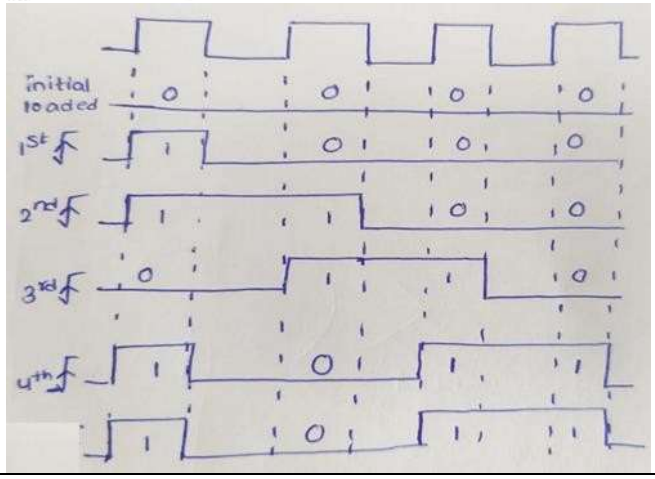
Excitation Table:

Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Construct a 4-bit shift register configuration that outputs the binary data pattern "1011" in parallel format after receiving it serially.







Design a MOD-8 ripple counter using JK Flip-flops and describe its functionality.

Since the modulus or mod

Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1