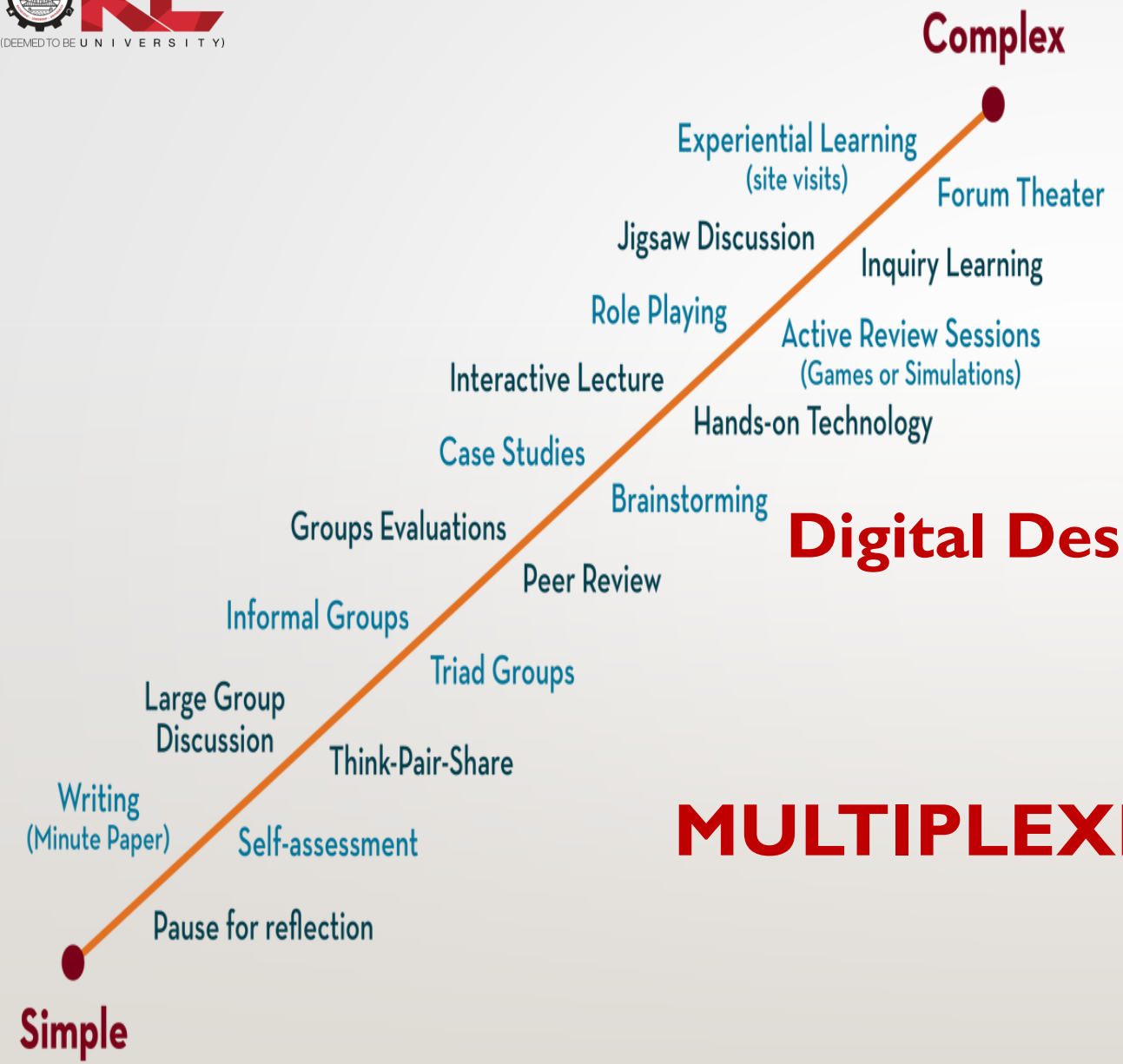


Department of BES-II

Digital Design and Computer Architecture
23EC1202

Topic:

MULTIPLEXERS AND DE-MULTIPLEXERS

Session No: 05

AIM OF THE SESSION

To familiarize students with the basic concept of multiplexers and demultiplexers.

INSTRUCTIONAL OBJECTIVES

This Session is designed to:

1. Demonstrate multiplexers, truth tables and its application.
2. Describe the demultiplexers, truth tables and its application.
3. Analyze how demultiplexers are used for data distribution.

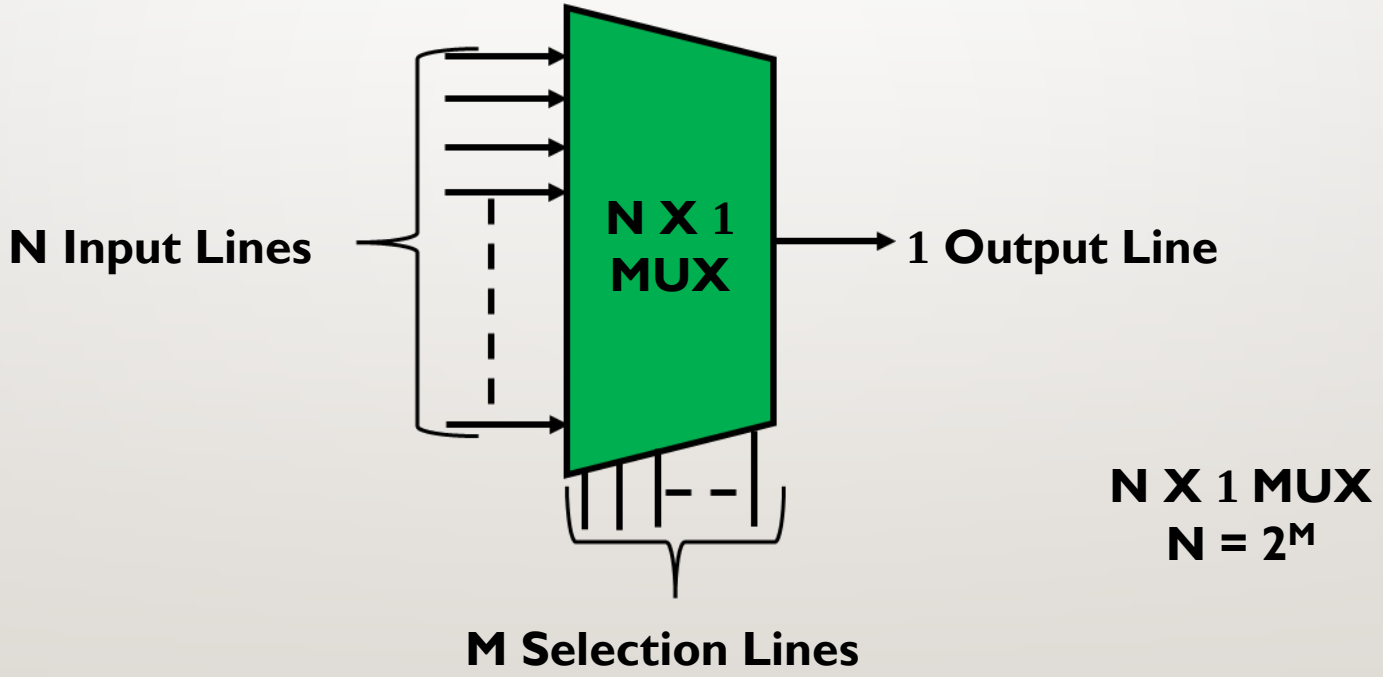
LEARNING OUTCOMES

At the end of this session, you should be able to:

1. Interpret and create truth tables for different multiplexer, demultiplexer configurations, demonstrating an understanding of how input lines are selected based on control inputs.
2. Apply the concepts of multiplexer and demultiplexer for data selection and distribution.

SESSION INTRODUCTION : MULTIPLEXER

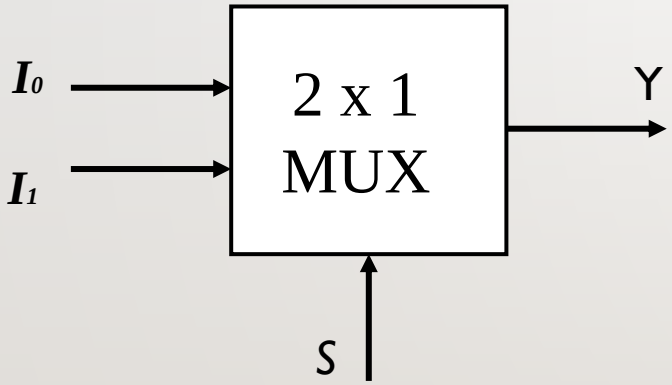
- A multiplexer is a combinational circuit that has M selection lines, 2^M input lines and a single output line.
- It is also called a data selector and control inputs are termed select inputs.



N X 1 MUX
$N = 2^M$

2X1 MULTIPLEXER

a) Block Diagram



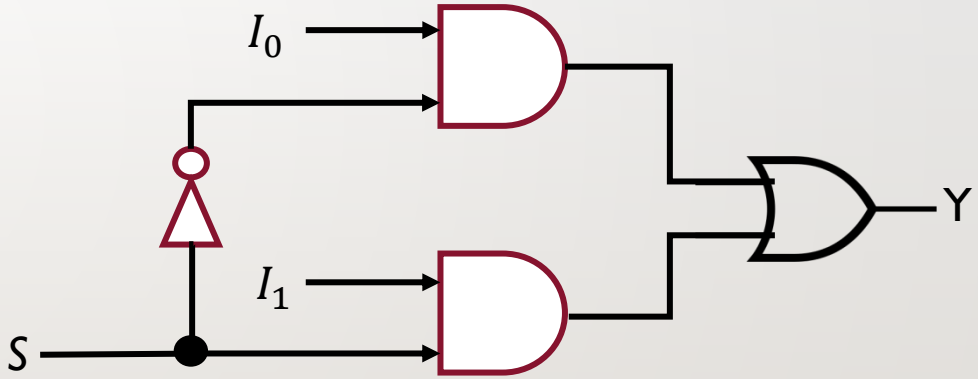
b) Truth Table

S	Y
0	I_0
1	I_1

Boolean Expression,

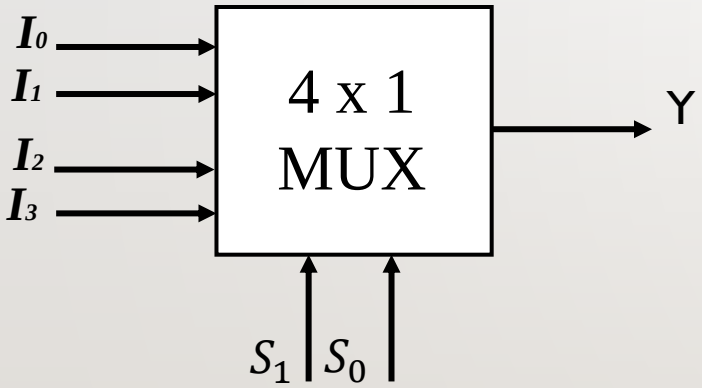
$$Y = I_0\overline{S} + I_1S$$

c) Logic Diagram



4X1 MULTIPLEXER

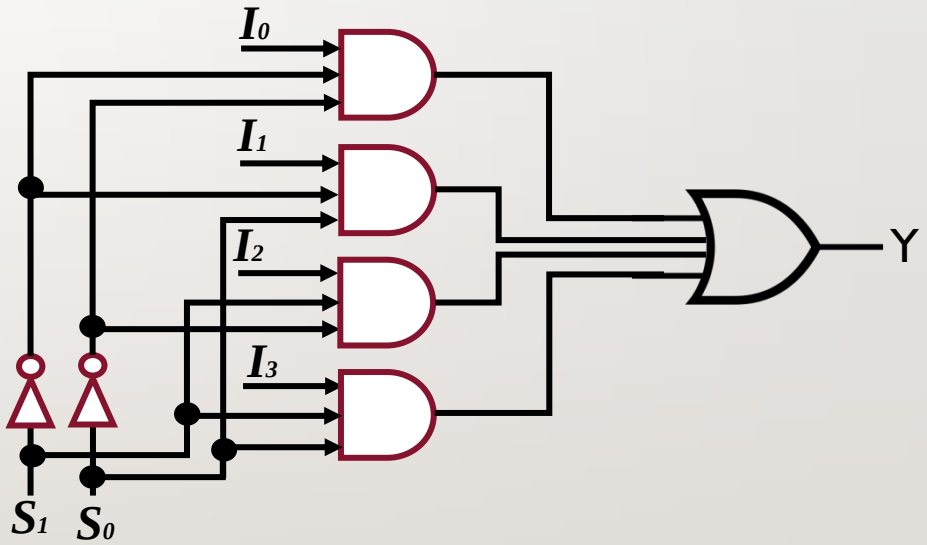
a) Block Diagram



b) Truth Table

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

c) Logic Diagram



Boolean Expression,

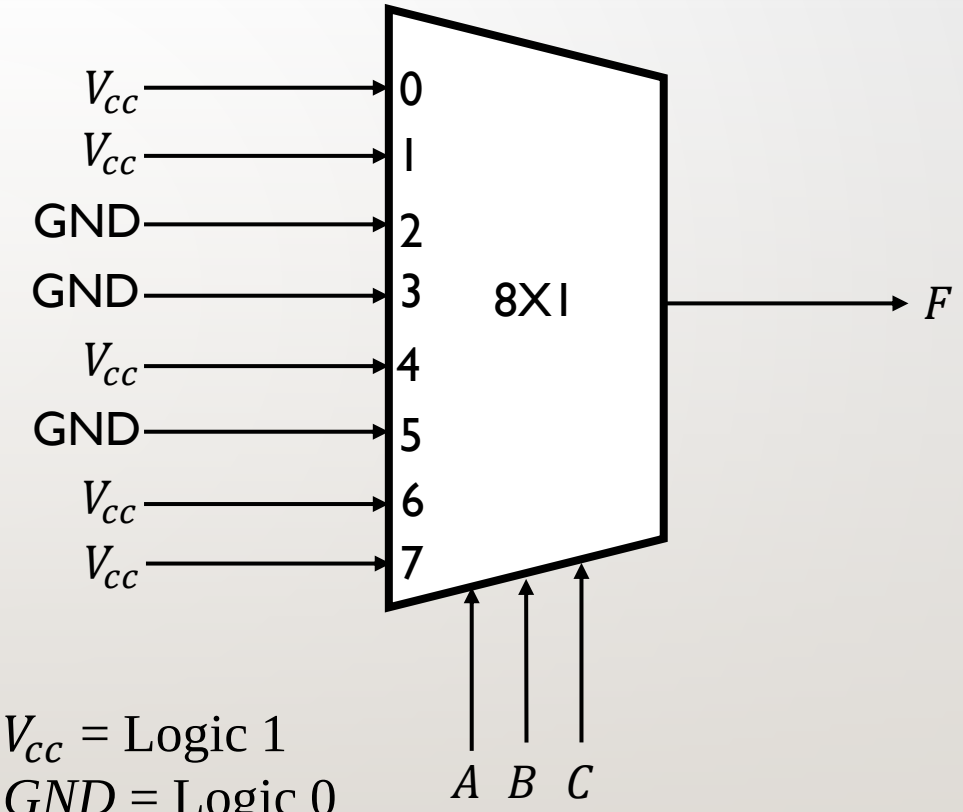
$$Y = \overline{S_1}\,\overline{S_0} I_0 + \overline{S_1} S_0 I_1 + S_1 \overline{S_0} I_2 + S_1 S_0 I_3$$

Implementation of Boolean Function using Multiplexers

Ex.1) Implement the function $F(A, B, C) = \sum m(0,1,4,6,7)$ using suitable MUX

Solution:

A	B	C	F (A,B,C)
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1



V_{cc} = Logic 1
GND = Logic 0

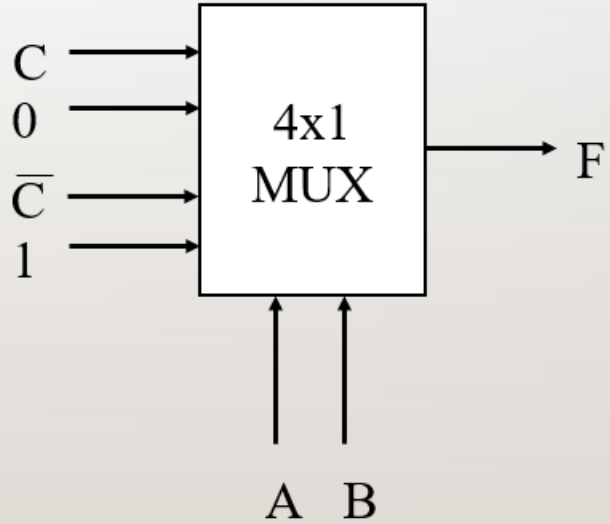
Ex.2) Implement the function $F(A,B,C) = \sum m(1,4,6,7)$ using 4X**1** MUX considering C as Input line and A, B as selection lines.

Solution:

a) Implementation Table

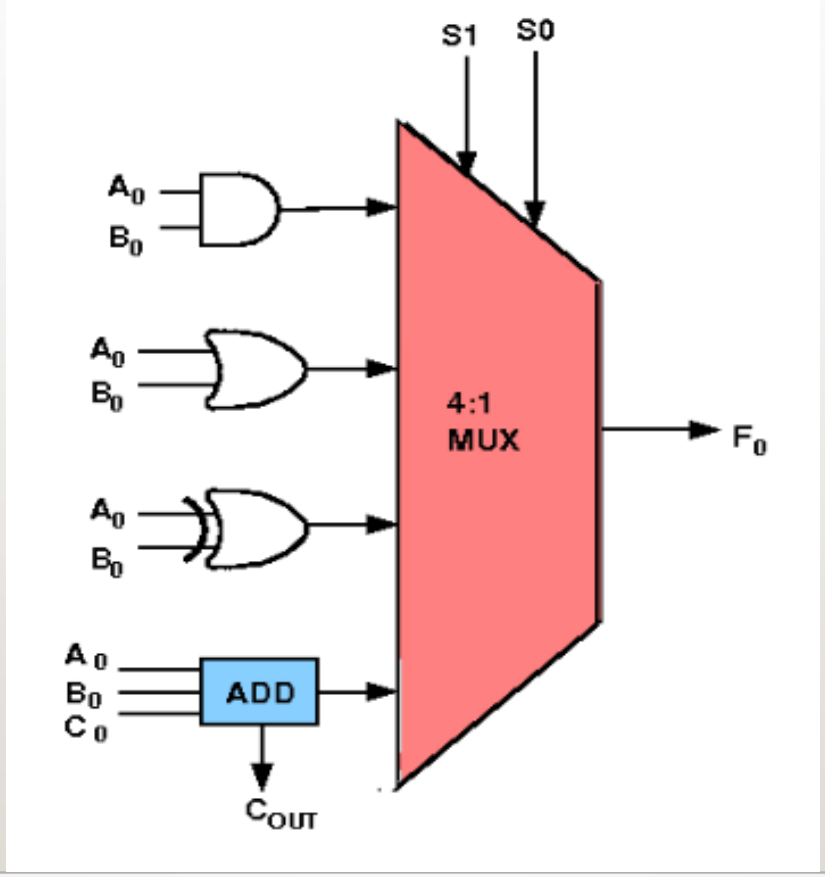
	I_0	I_1	I_2	I_3
	$\bar{A}\bar{B}$	$\bar{A}$B	A$\bar{B}$	AB
$\bar{C}$	0	2	(4)	(6)
C	(1)	3	5	(7)
	c	0	c'	1

b) Logic Diagram



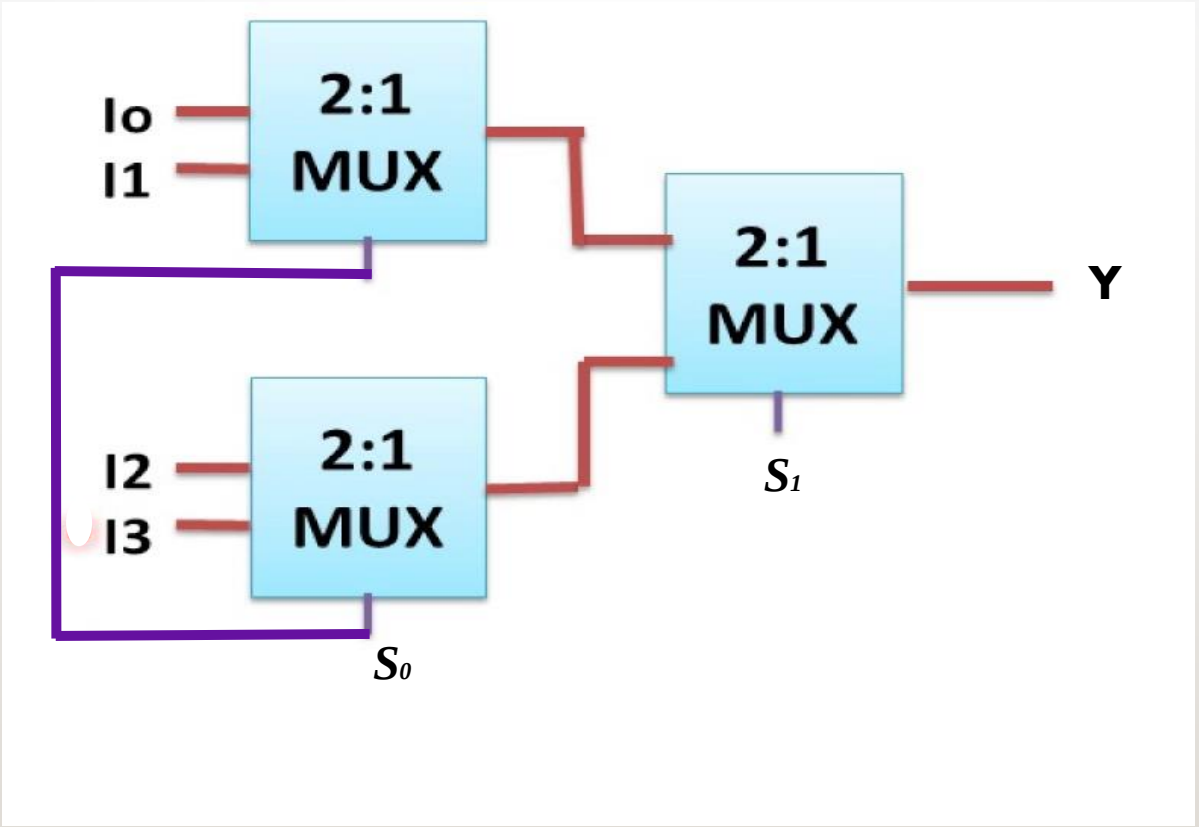
Ex.3) Develop an Arithmetic Logic Unit (ALU) by using a 4-to-1 Multiplexer.

Solution:



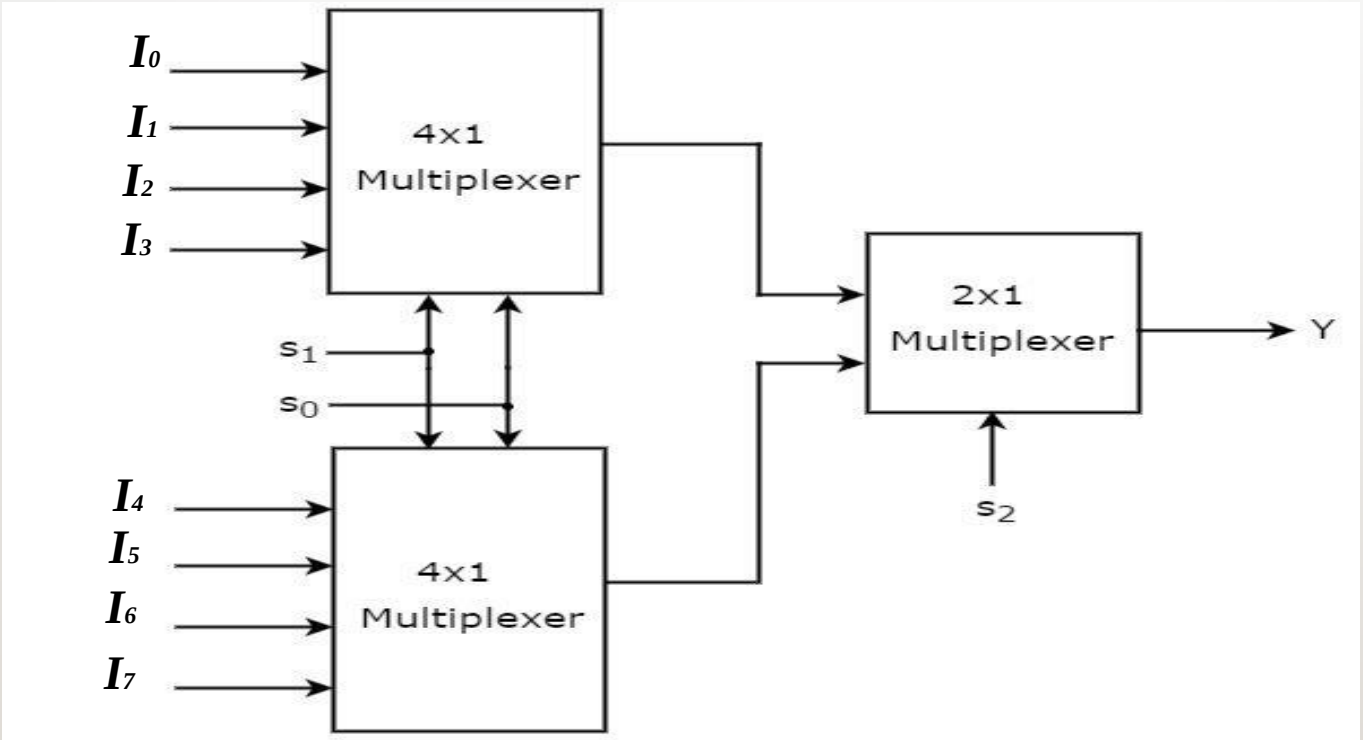
Ex.4) Design a 4x1 multiplexer using 2X1 multiplexers

Solution:



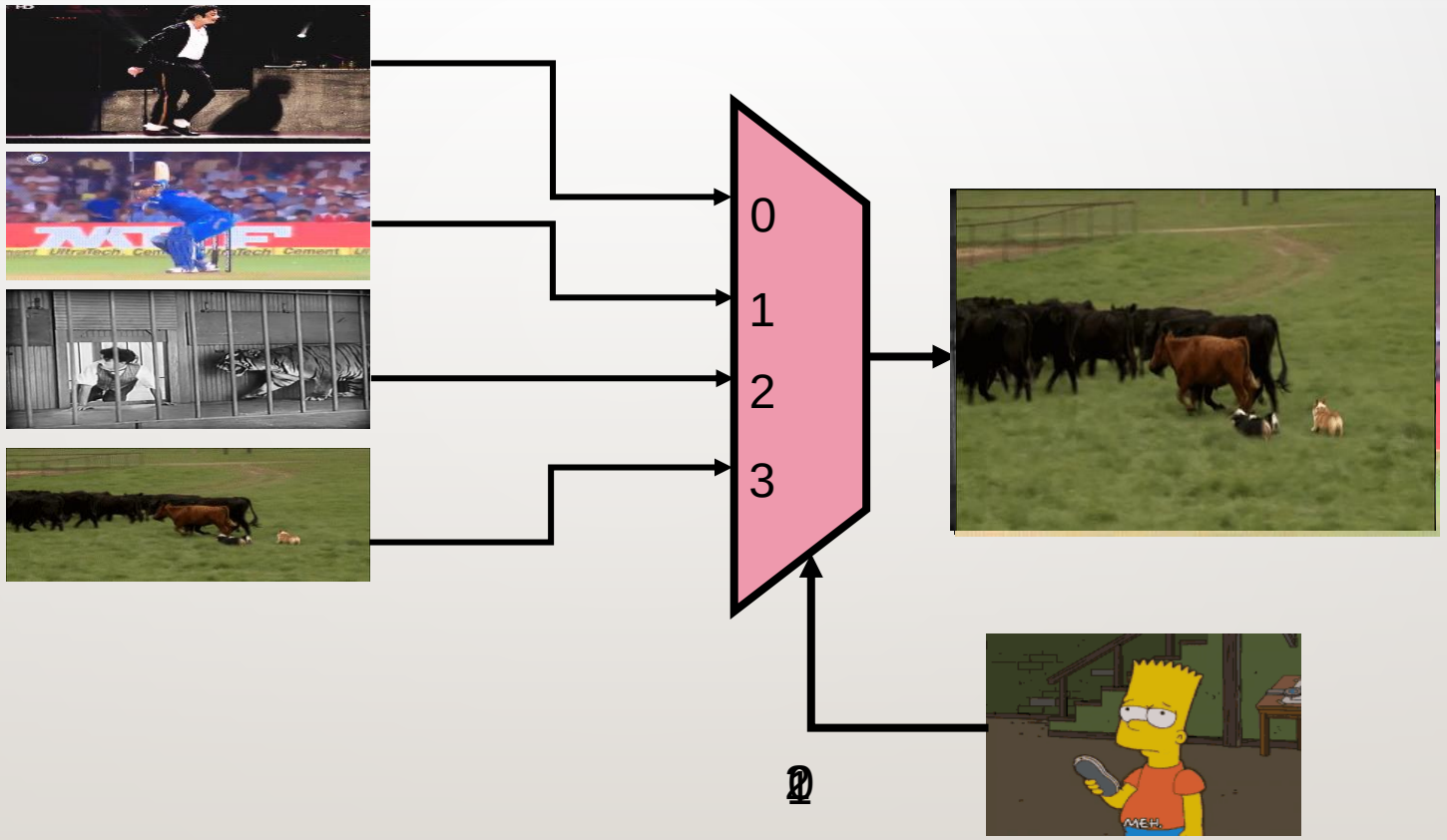
Ex.5) Design a 8x1 multiplexer using two 4*1 multiplexer and one 2x1 multiplexer.

Solution:



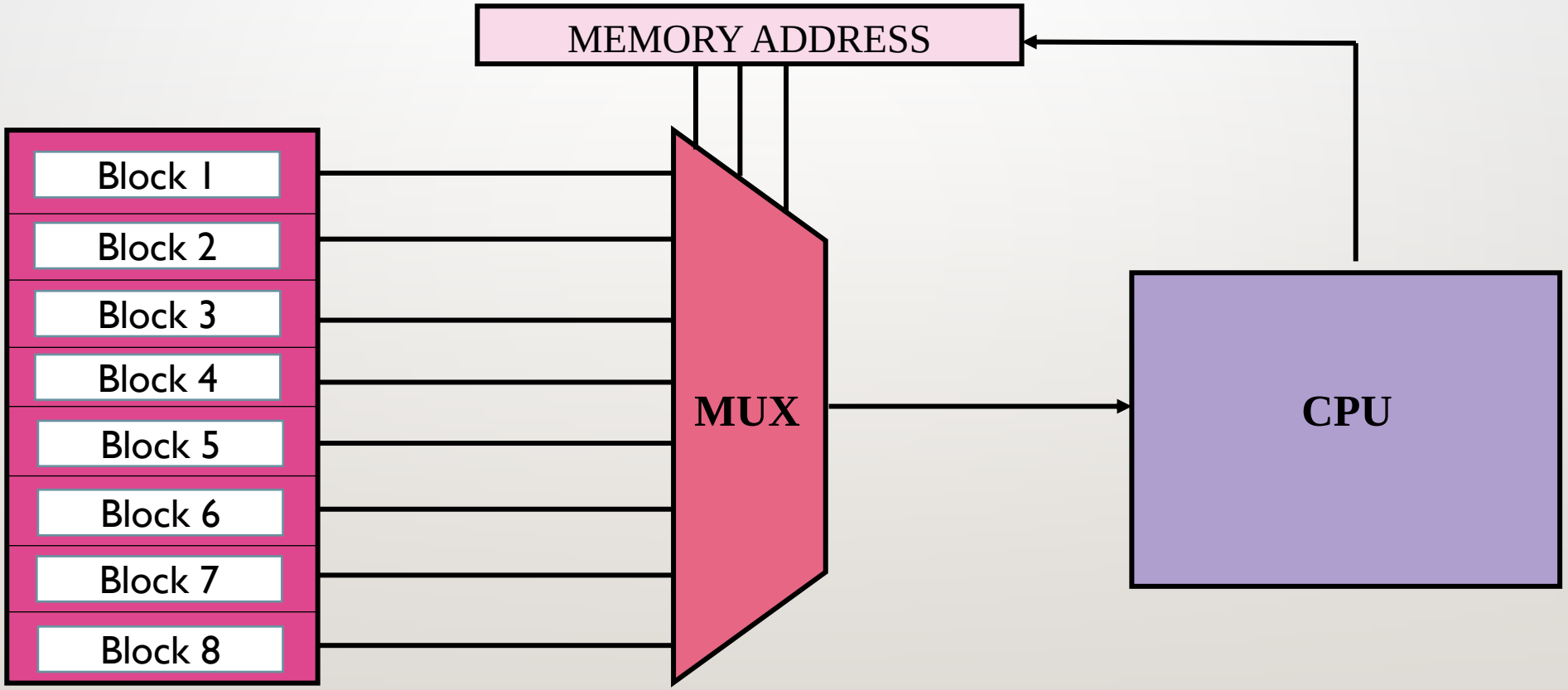
S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

APPLICATIONS OF A MULTIPLEXER



APPLICATIONS OF A MULTIPLEXER

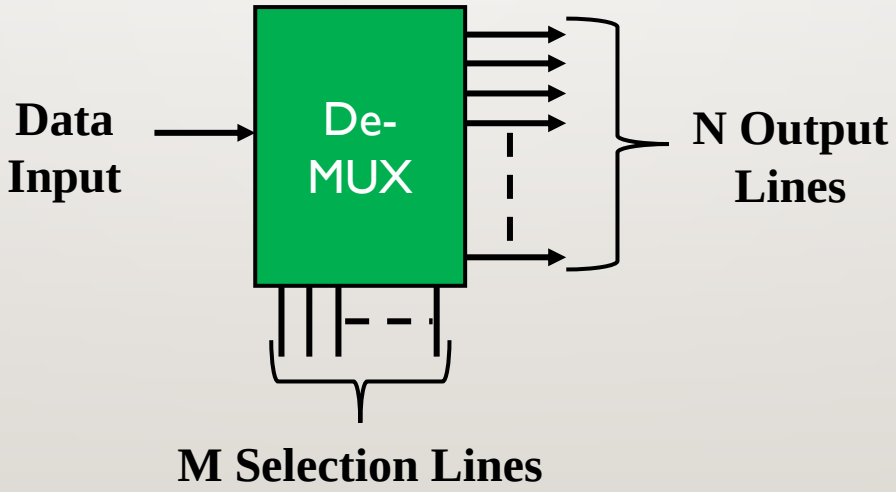
MEMORY UNIT



De-multiplexer

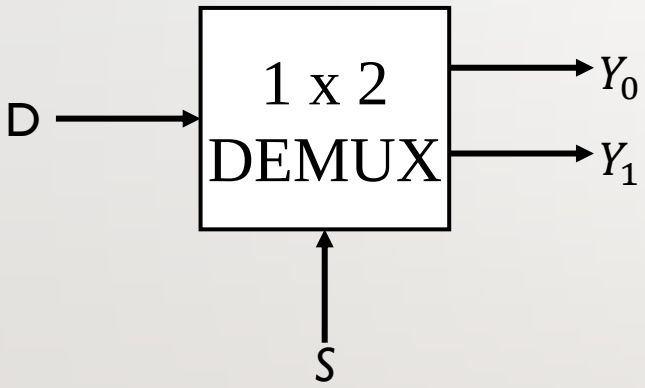
- A De-multiplexer is a combinational circuit that has only 1 input line and 2^M = N output lines and M selection lines.

- Demultiplex means one into many. By applying control signals, we can steer the input signal to one of the output lines.



1 x 2 DEMULTIPLEXER

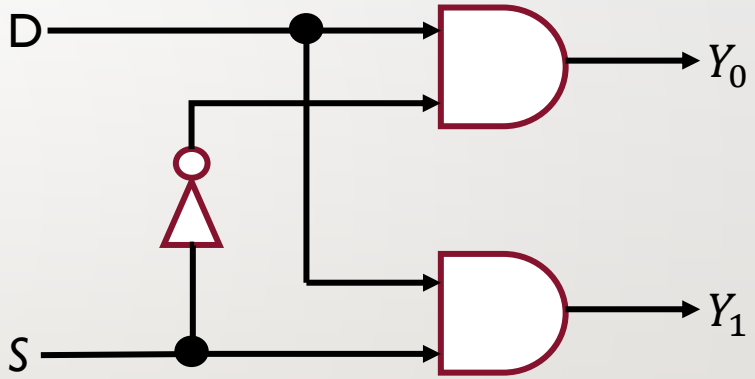
a) Block Diagram



b) Truth Table

Input	S	Y_0	Y_1
D	0	D	0
D	1	0	D

c) Logic Diagram



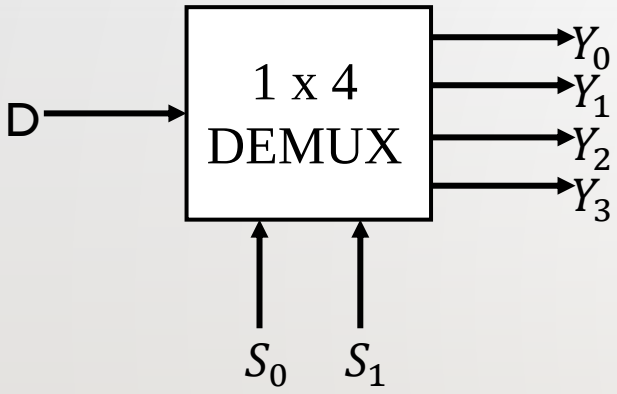
Boolean Expression,

$$Y_0 = D\overline{S}$$

$$Y_1 = DS$$

DEMULTIPLEXER : 1X4

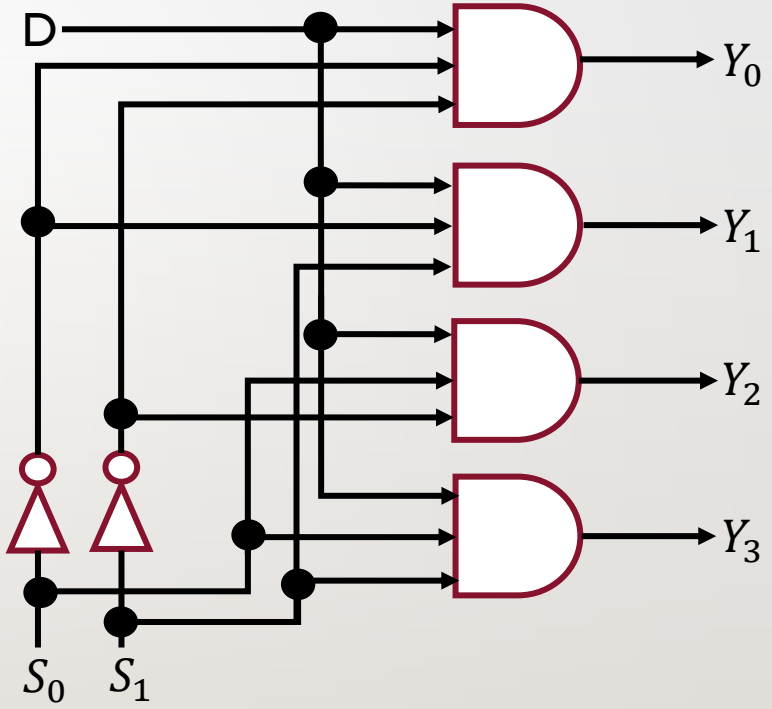
a) Block Diagram



b) Truth Table

Input	S_0	S_1	Y_0	Y_1	Y_2	Y_3
D	0	0	D	0	0	0
D	0	I	0	D	0	0
D	I	0	0	0	D	0
D	I	I	0	0	0	D

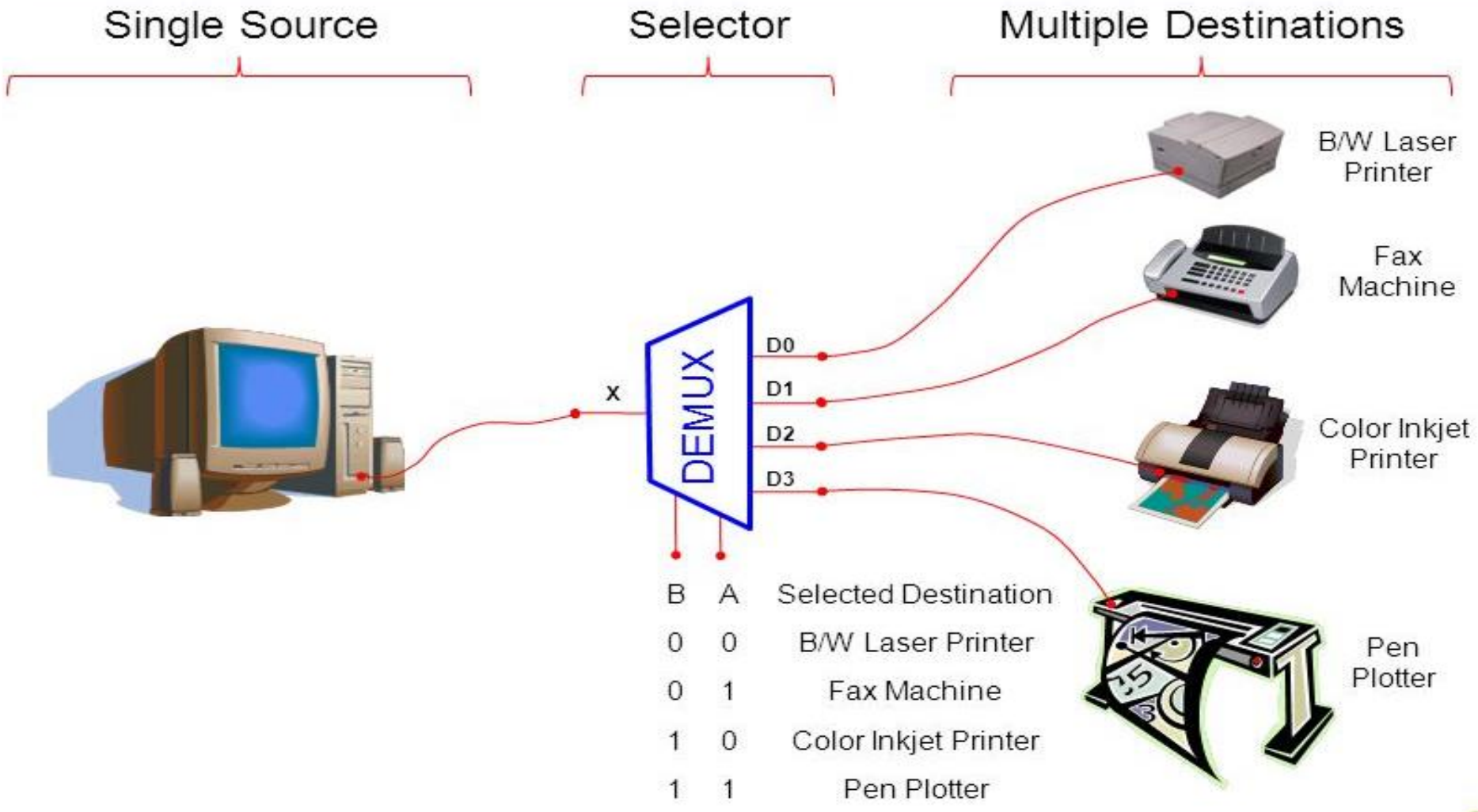
c) Logic Diagram



Boolean Expressions,

$$Y_0 = D\overline{S_0}\,\overline{S_1}$$
$$Y_1 = D\overline{S_0}S_1$$
$$Y_2 = DS_0\overline{S_1}$$
$$Y_3 = DS_0S_1$$

APPLICATIONS OF DEMUX



B	A	Selected Destination
0	0	B/W Laser Printer
0	1	Fax Machine
1	0	Color Inkjet Printer
1	1	Pen Plotter

SELF-ASSESSMENT QUESTIONS

1. What is a multiplexer?

A. It is a type of decoder which decodes several inputs and gives one output

B. A multiplexer is a device which converts many signals into one

C. It takes one input and results into many output

D. It is a type of encoder which decodes several inputs and gives one output

2. A 4-to-1 MUX has _____ input lines and _____ select lines.

A. 2, 1

B. 4, 2

C. 8, 2

D. 1, 4

SELF-ASSESSMENT QUESTIONS

3. What is the output configuration of a Demultiplexer (DEMUX)?

A. One input, multiple outputs
B. Multiple inputs, one output
C. Multiple inputs, multiple outputs
D. One input, one output

4. In a 4-to-1 MUX, if the select lines are 01, which input line will be selected?

A. Input 0
B. Input 1
C. Input 2
D. Input 3

TERMINAL QUESTIONS

Short answer questions:

1. Provide the symbol and truth table for a 4-to-1 multiplexer.

Long answer questions:

1. Design the function F(A,B,C)=∑m(1,4,5,7) using 4X1 MUX considering "A" as Input line and B, C as selection lines.
2. Design a 8:1 multiplexer using two 4:1 mux and one 2:1 mux.
3. Design an Arithmetic Logic Unit (ALU) by using a 4-to-1 Multiplexer.
4. Provide a thorough description of the architecture of a 1:4 de-multiplexer, including its input lines, control lines, and output.

REFERENCES FOR FURTHER LEARNING OF THE SESSION

Reference Books:

1. Computer System Architecture by M. Moris Mano

2. Fundamentals of Digital Logic with Verilog HDL by Stephen Brown and ZvonkoVranesic

Sites and Web links:

1. https://unacademy.com/content/jee/difference-between/multiplexer-and-demultiplexer/
2. https://www.electronicshub.org/multiplexer-and-demultiplexer/

THANK YOU

(DEEMED TO BE UNIVERSITY)

Team – Digital Design & Computer Architecture