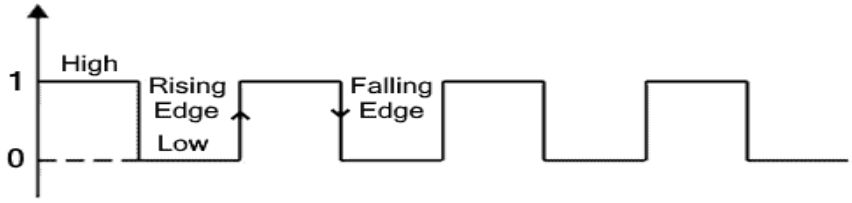
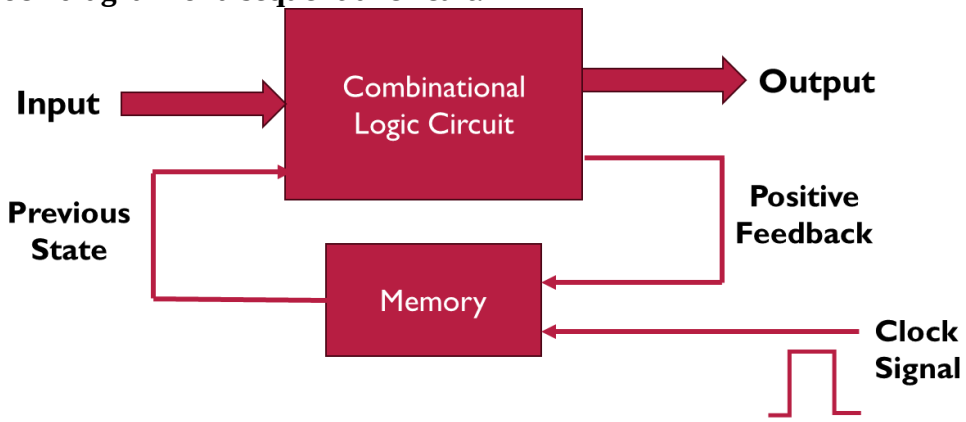
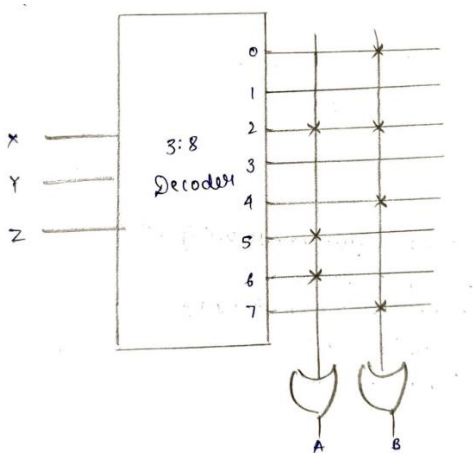
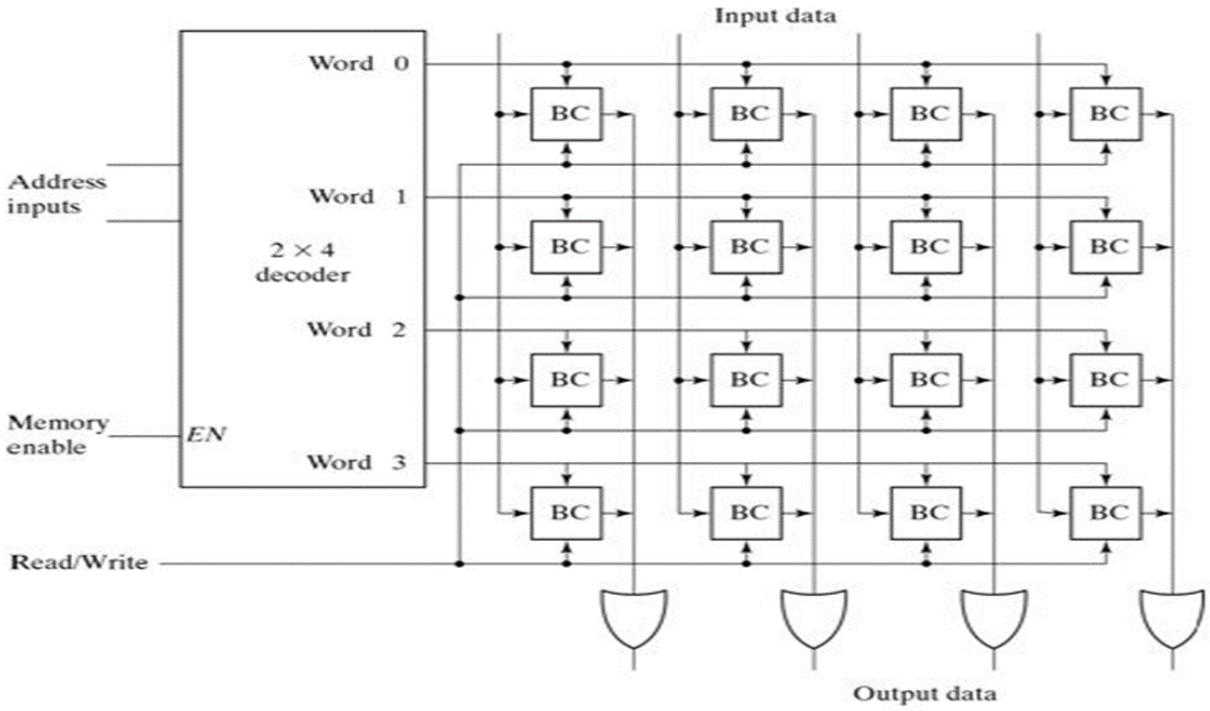
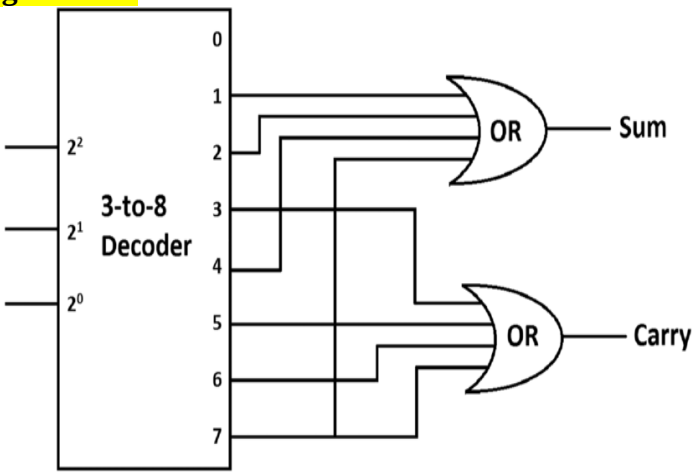
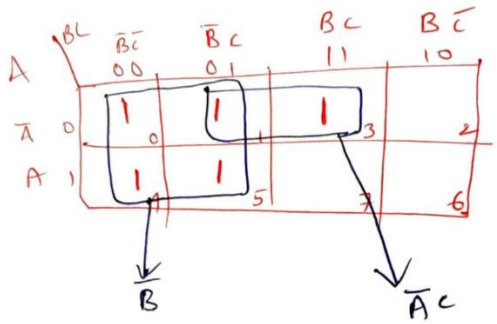
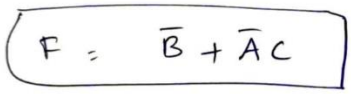
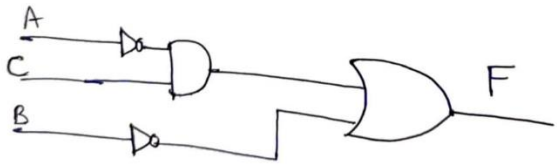
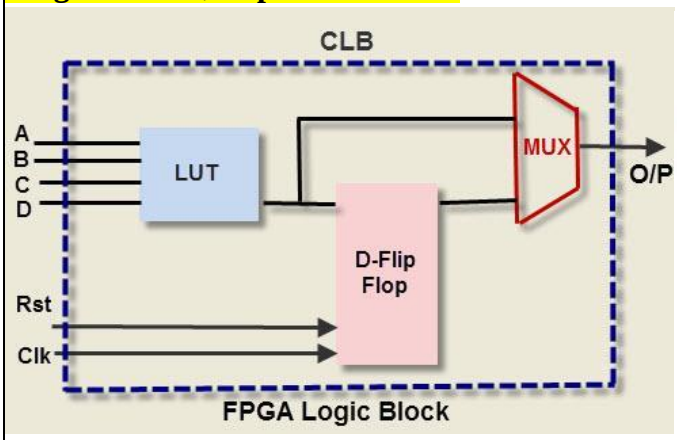
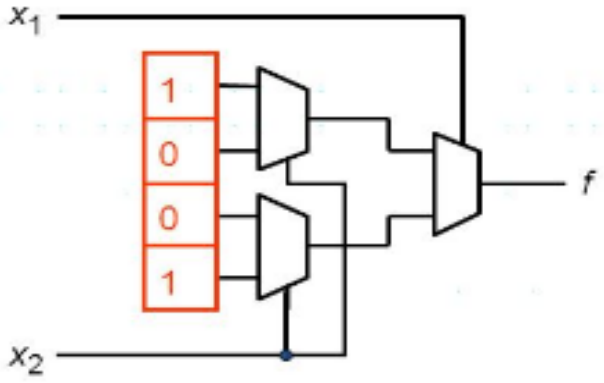
KONERU LAKSHMAIAH EDUCATION FOUNDATION
(Deemed to be University, Estd. u/s. 3 of UGC Act 1956)

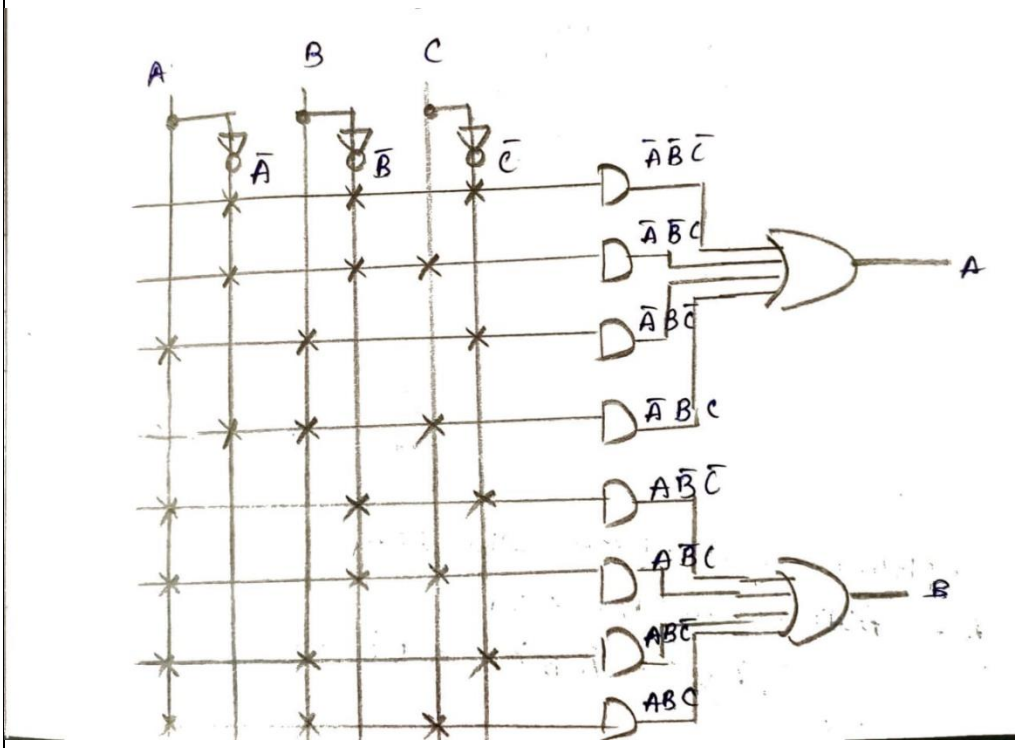
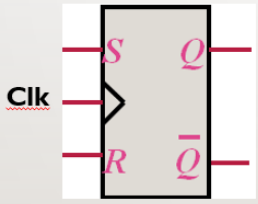
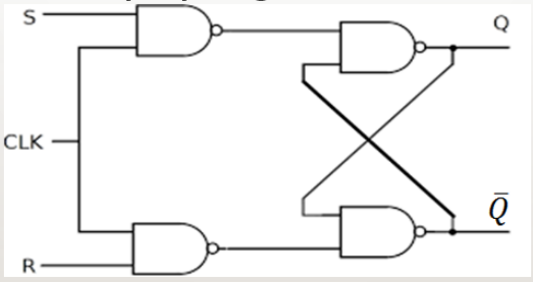
I- B. Tech- Even Sem: In Semester Exam-1
Academic Year:2024-2025
23EC1202 – DIGITAL DESIGN & COMPUTER ARCHITECTURE
Scheme of Evaluation - Set No: 1

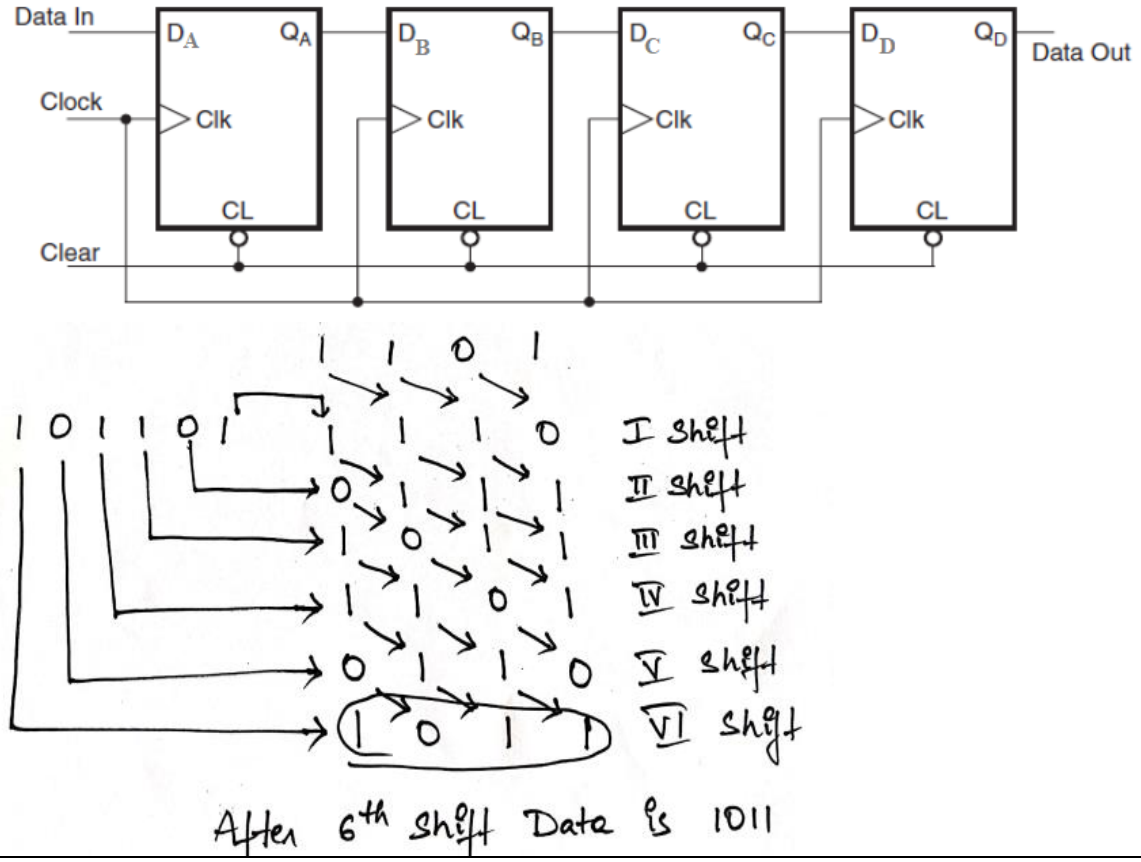
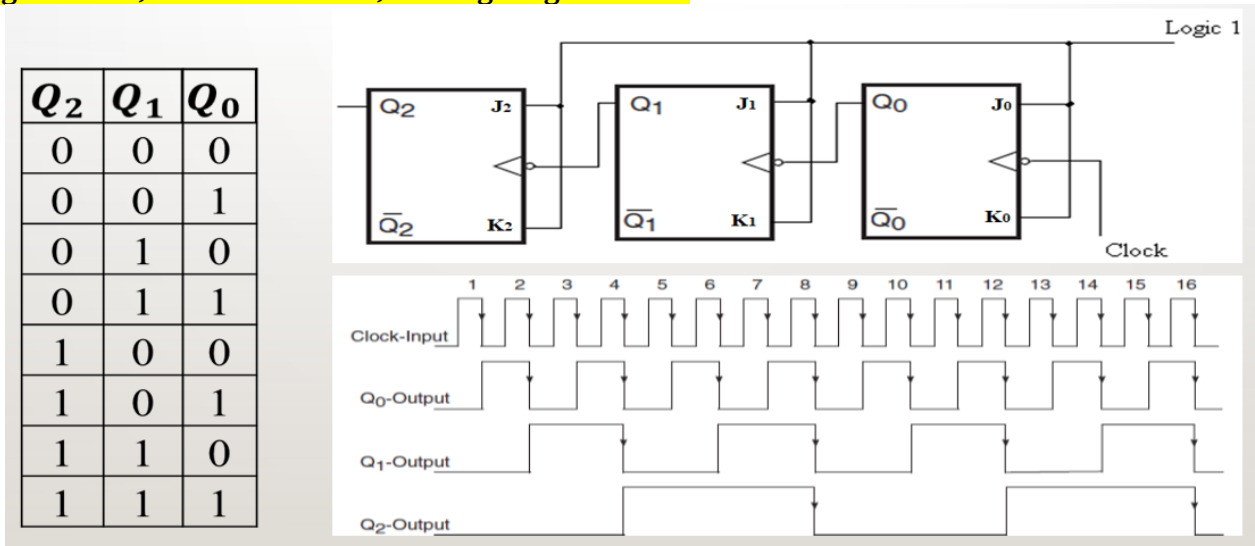
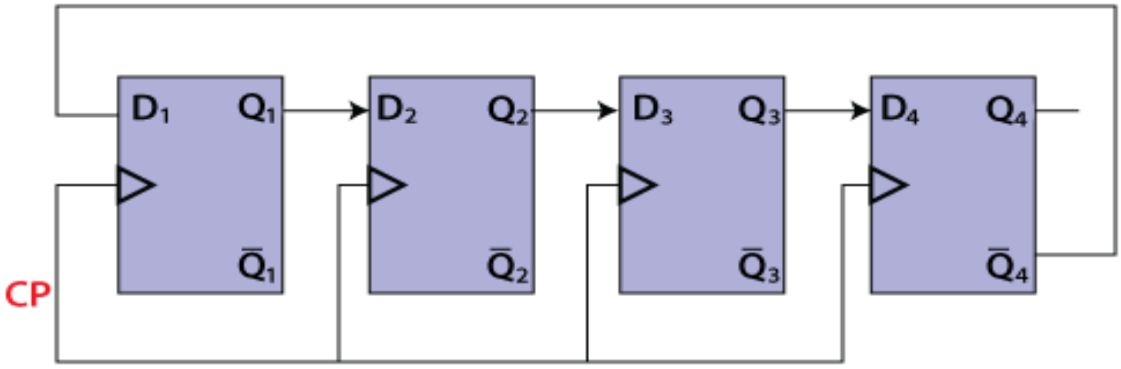
1.A.	**Simplify the expression F = AB+ A(B+C) + B(B+C) using Boolean identities.** $Y = AB + A(B + C) + B(B + C)$ $= AB + AB + AC + BB + BC$ *distributive law* $= AB + AB + AC + B + BC$ *idempotency theorem* $= AB + AC + B + BC$ $B + BC = B$ $= AB + AC + B$ $AB + B = B$ $= B + AC$	2M	CO1
1.B.	**Develop a truth table for the function F = ∑ m (1,4,6,7).** A B C F = ∑ m (1,4,6,7). 0 0 0 0 0 0 1 1 0 1 0 0 0 1 1 0 1 0 0 1 1 0 1 0 1 1 0 1 1 1 1 1	2M	CO1
1.C.	**Discuss the role of macrocells in CPLD architecture.** In a CPLD (Complex Programmable Logic Device) architecture, macrocells serve as the fundamental building blocks, essentially acting as programmable logic units that can perform both combinational and sequential logic functions by combining various logic gates like AND and OR within a single cell, allowing designers to implement complex logic circuits by connecting and configuring these macrocells together.	2M	CO1
1.D.	**Describe the need of clocking in flip-flops.** A clock pulse activates the sequential cicuit and then it changes its state based on the input and previous output. Triggering ensures precise timing and synchronization of state changes, which is crucial for reliable circuit operation.  Clock Pulse	2M	CO2

1.E.	**Draw the block diagram of a sequential circuit.** 	2M	CO2
1.F.	**Analyze the differences between synchronous and asynchronous counters.** **Synchronous sequential circuits** / **Asynchronous sequential circuits** Change their state only at specific intervals, dictated by a clock signal. / Do not rely on a clock signal for their operation, they change states immediately in response to changes in input. Memory elements are clocked flip-flops / Memory elements are un-clocked flip-flops or time delay elements. Easier to design and Clock-Dependent Delay / More difficult to design & responds immediately to changes in input	2M	CO2
2.A.	**Represent the given expression in canonical POS form Y = (A + B)(B + C)(A + C).** $Y = (A+B)(B+C)(A+C)$ $= (A+B+(C\cdot\bar{C}))(B+C+(A\cdot\bar{A}))(A+(B\cdot\bar{B})+C)$ $= (A+B+C)(A+B+\bar{C})(A+B+C)(\bar{A}+B+C)(A+B+C)(A+\bar{B}+C)$ $= (A+B+C)(A+B+\bar{C})(\bar{A}+B+C)(A+\bar{B}+C)$	4M	CO1
2.B.	Design the following Boolean functions using PROM. i) A (X,Y,Z) = ∑m (2,5,6) ii) B (X,Y,Z) = ∑m (0,2,4,7) 	4M	CO1

2.C.	**Illustrate the differences between Latch and Flip-Flops.** **Latches** / **Flip-flops** Continuously checks its inputs and changes output accordingly. / Continuously checks its inputs and changes output at times determined by the clock signal. Level Triggered / Edge Triggered Requires Enable signal to function / Requires clock to function Made up of Logic gate blocks / Made up of Latches and Logic gates	4M	CO2
2.D.	**Construct a memory decoding unit, using a 2:4 decoder.** 	4M	CO2
3.A.	**Design a Full Adder circuit utilizing an appropriate decoder and OR gates.** **Truth table (or) expressions: 2M, Diagram: 3M** A B C SUM CARRY 0 0 0 0 0 0 0 1 1 0 0 1 0 1 0 0 1 1 0 1 1 0 0 1 0 1 0 1 0 1 1 1 0 0 1 1 1 1 1 1  Sum = ∑m(1, 2, 4, 7) Carry = ∑m(3, 5, 6, 7)	5M	CO1

3.B	**Optimize the equation F (A, B, C) = AB'C + A'B'C + A'BC + A'B'C' + AB'C' using K-Maps and realize the resultant expression using logic gates.**   	6M	CO1
4.A.	**Illustrate the flexibility and programmability enabled by configuring Look-Up Tables (LUTs) in FPGAs.** **Diagrams: 3M, Explanation: 2M.**  	5M	CO1

4.B.	**Design the following Boolean functions using PAL. A (X,Y,Z) = Sum of Even Numbers (include Zero also) and B (X,Y,Z) = Sum of Odd Numbers.** 	6M	CO1
5.A.	**Develop the SR flip-flop characteristics table and excitation table.** **Logic Symbol:**  **SR Flip-flop using NAND Gates:**  **Truth Table:** S R Q (t+1) 0 0 Q (t) 0 1 0 1 0 1 1 1 Invalid **Characteristic Table:** S R Q(t) Q(t+1) 0 0 0 0 0 0 1 1 0 1 0 0 0 1 1 0 1 0 0 1 1 0 1 1 1 1 0 Invalid 1 1 1 Invalid **Characteristic Equation:** $Q(t+1) = S + \bar{R}\,Q(t)$ **Excitation Table:** Q(t) Q(t+1) S R 0 0 0 X 0 1 1 0 1 0 0 1 1 1 X 0	5M	CO2

5.B.	**A 4-bit register is initially filled with the data "1101". The register is shifted six times to the right with the serial input being 101101. What is the content of the register after each shift?** 	6M	CO2
6.A	**Design a MOD-8 ripple counter using JK Flip-flops and describe its functionality.** **Diagram: 2M, Truth table: 1M, Timing diagram: 2M.** 	5M	CO2
6.B	**Design 4-bit Johnson counter using D-flip-flops and describe it's working.** **Diagram: 2M, Truth table: 2M, Explanation: 2M.** 	6M	CO2

CP	Q1	Q2	Q3	Q4
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0