Experiment 5:Design and analyze the frequency response of FET Amplifier

AIM: To Design and study the frequency response of a common source amplifier using a given transistor.

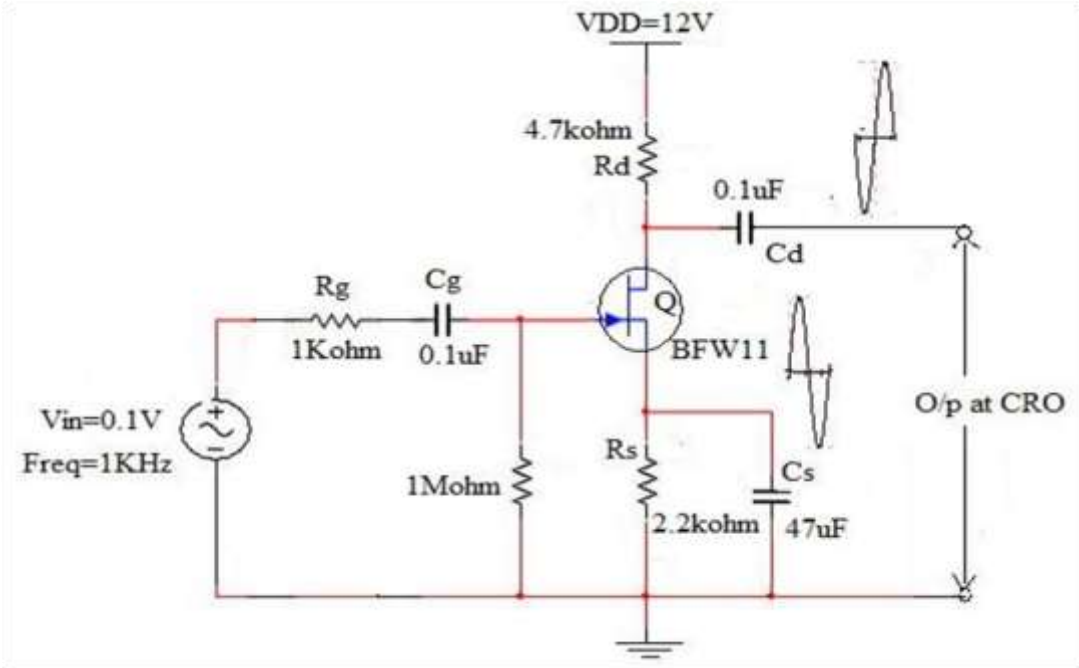
i) To measure the Maximum voltage gain of the amplifier.

ii) To obtain the frequency response characteristics and the band width of the amplifier.

THEORY:

The common source amplifier configuration is widely used amongst other JFET configurations and can provide both high voltages gain and large input impedance. In this configuration, the input signal is applied to the gate and the output signal is taken from the drain, while the source terminal being the reference or common. In order to work as an amplifier, the JFET should be properly biased by setting the gate-source voltage which results in the required drain current. The N-channel JFET requires that the gate-source voltage always be less negative than the pinch-off voltage, but less than zero. Since virtually no gate current flows due to the JFET's high input impedance, the gate voltage is essentially at ground level. Consequently, using only a drain-supply voltage, the required negative quiescent gate-source voltage is developed by the voltage drop across the source resistor of the self-bias circuit shown in Fig. This circuit is one of the simplest and practical bias circuits for JFET amplifiers in which a single power supply is used.

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connect circuit as per circuit diagram.
2. Set the Input(Vi) = 100 mv (sinewave), using the Function generator and then connect at the input terminals.
3. Connect the C.R.O at output terminals i.e. Output (Vo).
4. Keep the input voltage constant,Vary the frequency from 50 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
5. Calculate the gain & magnitude of the amplifier using the given formula.

   Max volage Gain = V_o/V_i

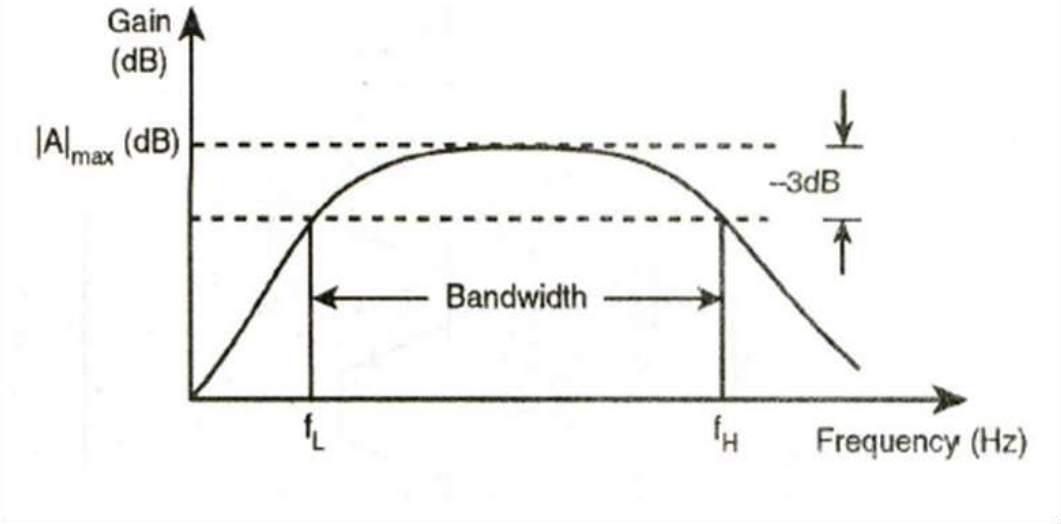
   Gain in dB= 20 log (V_o / V_i)
6. Plot the graph on semi-log sheet taking frequency(Hz) along X-axis and gain in (dB) along y-axis. Frequency response graph is as shown in fig. Below
7. Indicate the lower 3dB frequency (f_L) and upper 3dB the bandwidth (f_H) the graph.
8. Calculate the bandwidth from the graph, BW= f_H-f_L(Hz)

TABULAR COLUMN:

Vin=100mv (or) 0.1V

Sl No.	Frequency	V_O (volts)	Gain = V_O/V_i	Gain (dB) =20log V_O/V_i

Model Graph: (Frequency Response)



RESULT:

1) **Maximum voltage gain =**

2) **Lower cut-off frequency (f_L) =**

3) **Upper cut-off frequency (f_H) =**

4) **Band width (f_H- $f_{L)}$ =**

Evaluator Remark (if Any):	**Marks Secured: _____out of 50**
	Signature of the Evaluator with Date