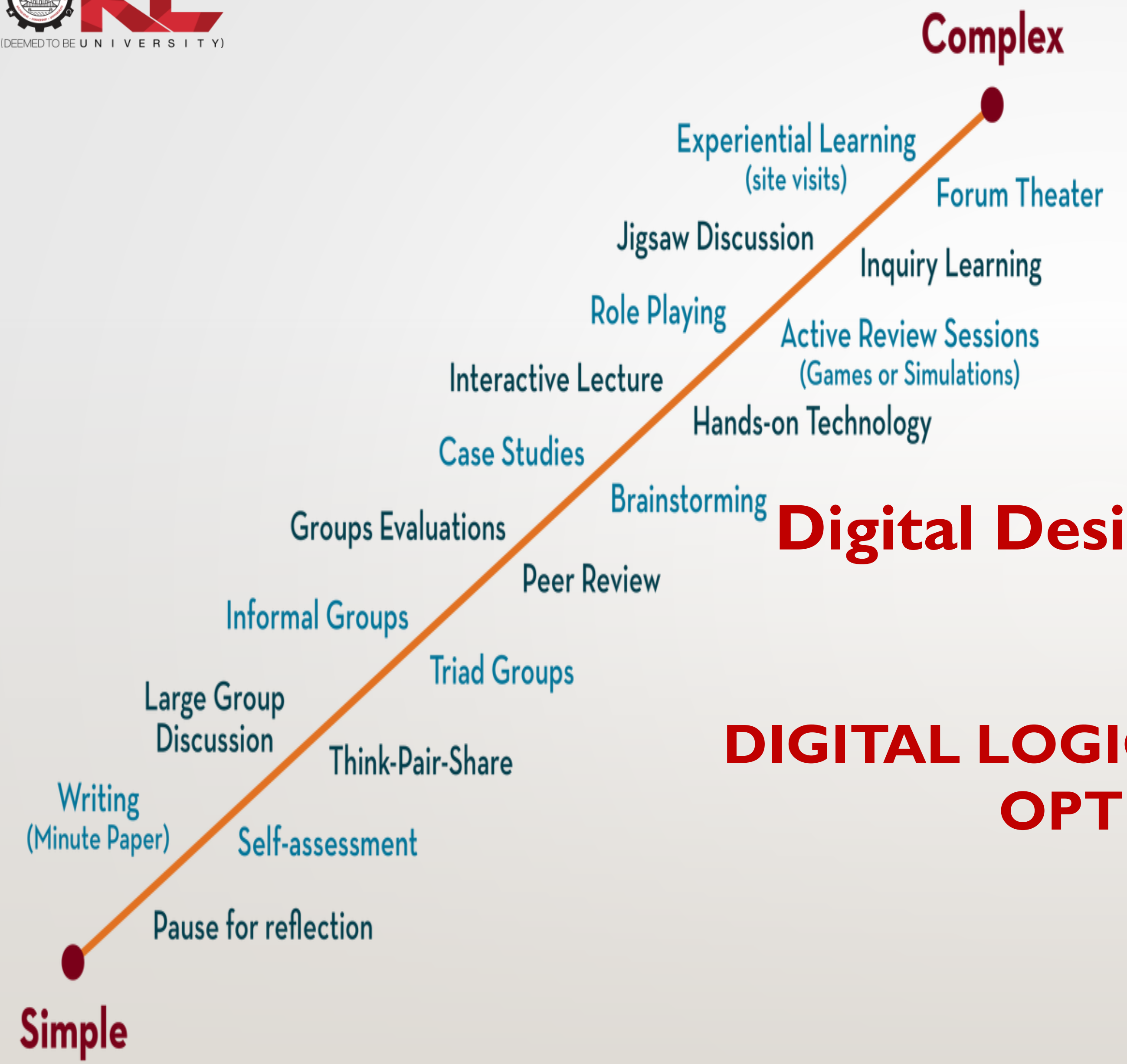


Department of BES-II

Digital Design and Computer Architecture

23EC1202

Topic:

DIGITAL LOGIC SOP/POS REPRESENTATION AND OPTIMIZATION TECHNIQUES

Session No: 03

AIM OF THE SESSION

The primary aim of this session is to provide students with a comprehensive understanding of the representation and optimization techniques associated with Sum-of-Products (SOP) and Product-of-Sums (POS) forms in digital logic.

INSTRUCTIONAL OBJECTIVES

This Session is designed to:

1. Illustrate the process of representing Boolean functions in Sum-of-Products (SOP) and Product-of-Sums (POS) forms.
2. Highlight the significance of terms, minterms in SOP, and maxterms in POS & Enumerate techniques to optimize SOP and POS expressions for better circuit efficiency.

LEARNING OUTCOMES

At the end of this session, you should be able to:

1. Understand SOP and POS Representations.
2. Interpret SOP and POS Notations.

Session Introduction: Boolean Function or Expression

- A **Boolean expression** or a function is an expression which consists of binary variables joined by the Boolean connectives AND and OR along with NOT operation.

- **Minterm:** A minterm is a standard product which consists of all variables in either complemented or un-complemented form for which the output is 1. **Example: A'B'C**

- **Maxterm:** A maxterm is a standard sum which consists of all variables in either complemented or un-complemented form for which the output is 0. **Example: A+B+C**

Minterms and Maxterms (with three variables)

Row number	x_1	x_2	x_3	Minterm	Maxterm
0	0	0	0	$m_0 = \bar{x}_1\bar{x}_2\bar{x}_3$	$M_0 = x_1 + x_2 + x_3$
1	0	0	1	$m_1 = \bar{x}_1\bar{x}_2x_3$	$M_1 = x_1 + x_2 + \bar{x}_3$
2	0	1	0	$m_2 = \bar{x}_1x_2\bar{x}_3$	$M_2 = x_1 + \bar{x}_2 + x_3$
3	0	1	1	$m_3 = \bar{x}_1x_2x_3$	$M_3 = x_1 + \bar{x}_2 + \bar{x}_3$
4	1	0	0	$m_4 = x_1\bar{x}_2\bar{x}_3$	$M_4 = \bar{x}_1 + x_2 + x_3$
5	1	0	1	$m_5 = x_1\bar{x}_2x_3$	$M_5 = \bar{x}_1 + x_2 + \bar{x}_3$
6	1	1	0	$m_6 = x_1x_2\bar{x}_3$	$M_6 = \bar{x}_1 + \bar{x}_2 + x_3$
7	1	1	1	$m_7 = x_1x_2x_3$	$M_7 = \bar{x}_1 + \bar{x}_2 + \bar{x}_3$

Representation of SOP & POS using Min & Max terms

Sum of minterms

$$F = A'B'C + AB'C' + ABC' + ABC = \sum m\,(1,4,6,7)$$

Product of Maxterms

$$F = (A+B+C)\,(A+B'+C)\,(A+B'+C')\,(A'+B+C') = \pi\,M\,(0,2,3,5)$$

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Standard form and Canonical form

Standard Form:

Standard form means Standard Sum of Products form. In this form, each product term need not contain all literals.

Canonical SOP form:

Canonical SOP form means Canonical Sum of Products form. In this form, each product term contains all literals.

Canonical POS form:

Canonical POS form means Canonical Product of Sums form. In this form, each sum term contains all literals.

Examples on Canonical form

Represent the given expression in canonical SOP form Y = AC + AB + BC.

$$AC+AB+BC= AC.(B+B')+ AB.(C+C')+BC.(A+A')$$

$$= ABC+AB'C+ABC+ABC'+ABC+A'BC$$

Hence Y= ABC+AB'C+ABC'+A'BC

Karnaugh Maps (K-Maps)

Introduction:

- Karnaugh Maps (K-Maps) are graphical representations used in digital logic design to simplify Boolean expressions and optimize logical circuits.
- It takes two forms: Sum of product (SOP) & Product of Sum (POS)

Advantages of K-Maps:

- Visualization: Provides a visual representation of the Boolean function, aiding in understanding.
- Systematic Approach: Systematic grouping helps ensure that all possible combinations are considered.
- Error Reduction: Reduces the likelihood of errors compared to manual manipulation of Boolean expressions.

2-VARIABLE K-MAPS STRUCTURE

A. SOP: -

A \ B	$\overline{B}$ 0	B 1
$\overline{A}$ 0	$\overline{A}.\overline{B}$	$\overline{A}.B$
A 1	$A.\overline{B}$	$A.B$

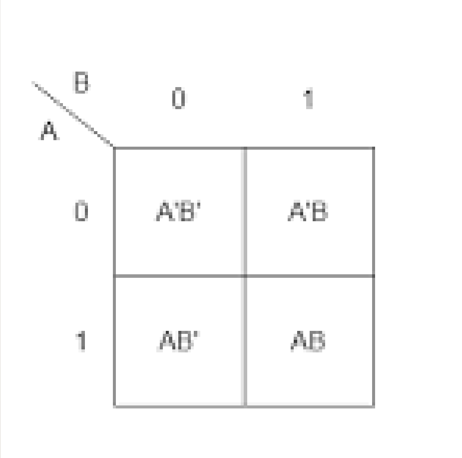
B. POS: -

A \ B	B 0	$\overline{B}$ 1
A 0	$A+B$	$A+\overline{B}$
$\overline{A}$ 1	$\overline{A}+B$	$\overline{A}+\overline{B}$

Example

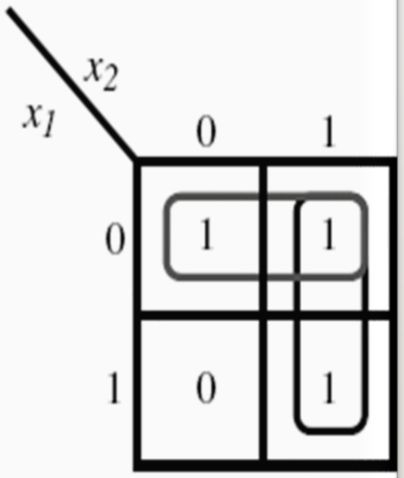
- **Map structure, rows & columns, cell numbering**

- **Grouping : Pair / Quad**



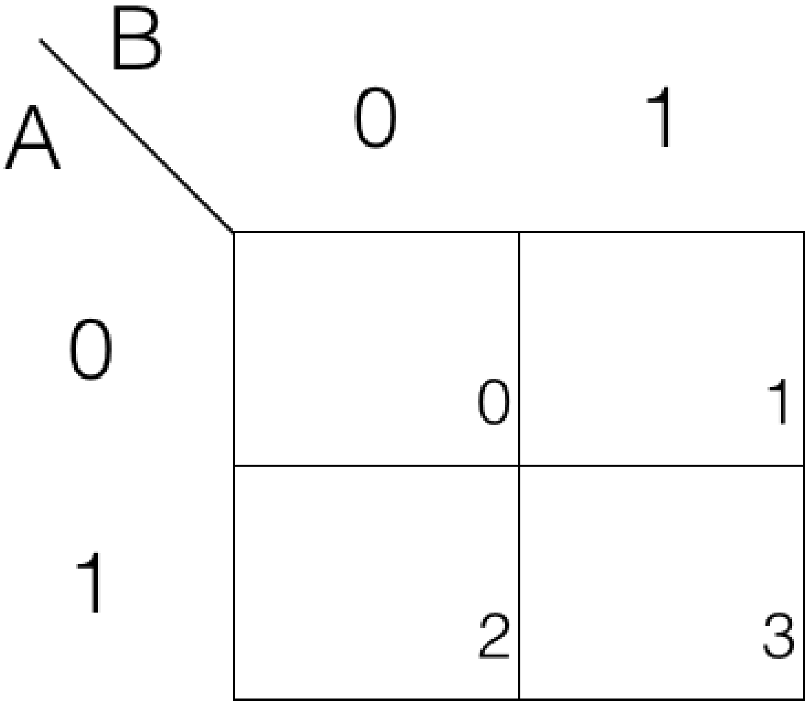
Example: $f\,(A,B) = A'\,.\,B' + A'\,.\,B + A\,.\,B$

x_1	x_2	f
0	0	1
0	1	1
1	0	0
1	1	1



$$f = \overline{x}_1 + x_2$$

EXERCISE



3-Variable K-Maps Structure

A \ BC	00	01	11	10
0	A'B'C' (0)	A'B'C (1)	A'BC (3)	A'BC' (2)
1	AB'C' (4)	AB'C (5)	ABC (7)	ABC' (6)

Grouping :

- **Oct - 8 cells**
- **Quad – 4 cells (1*4 or 2*2)**
- **Pair (2*1 or 1*2)**

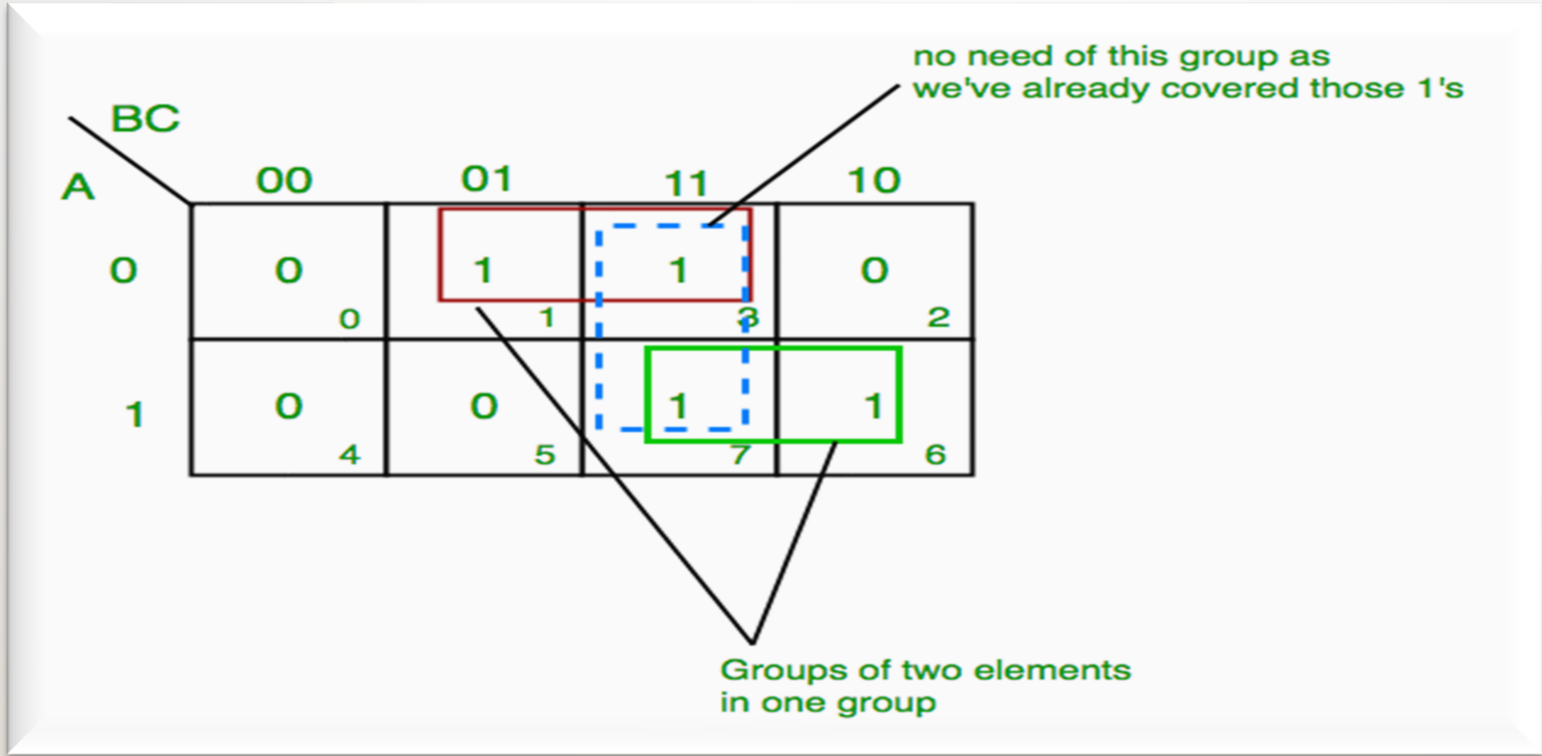
3-VARIABLE K-MAPS STRUCTURE

AB \ C	0	1
00	m_0	m_1
01	m_2	m_3
11	m_6	m_7
10	m_4	m_5

A \ BC	00	01	11	10
0	m_0	m_1	m_3	m_2
1	m_4	m_5	m_7	m_6

Example of 3-Variable K-Maps

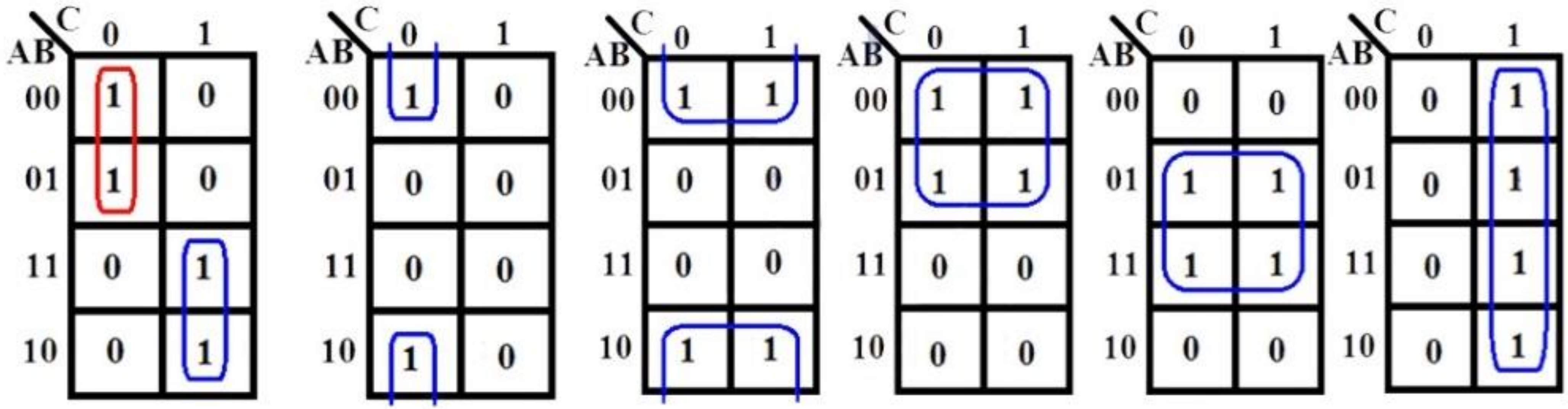
Given Z = ∑ m (1,3,6,7) → Minimize using 3 variable K-Maps



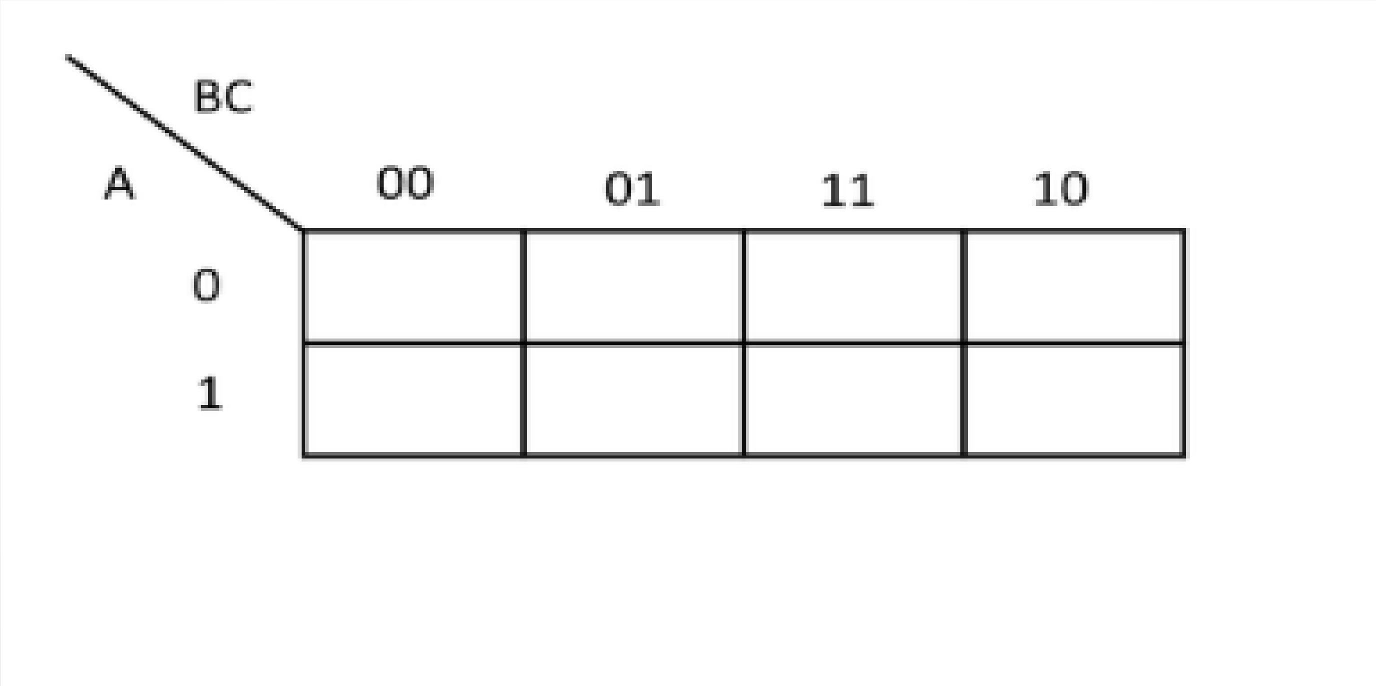
Minimized expression

Z = A'C+AB

Types of Grouping in K-Map:



Groups of 2 Groups of 4


BC
A
00
01
11
10
0
1

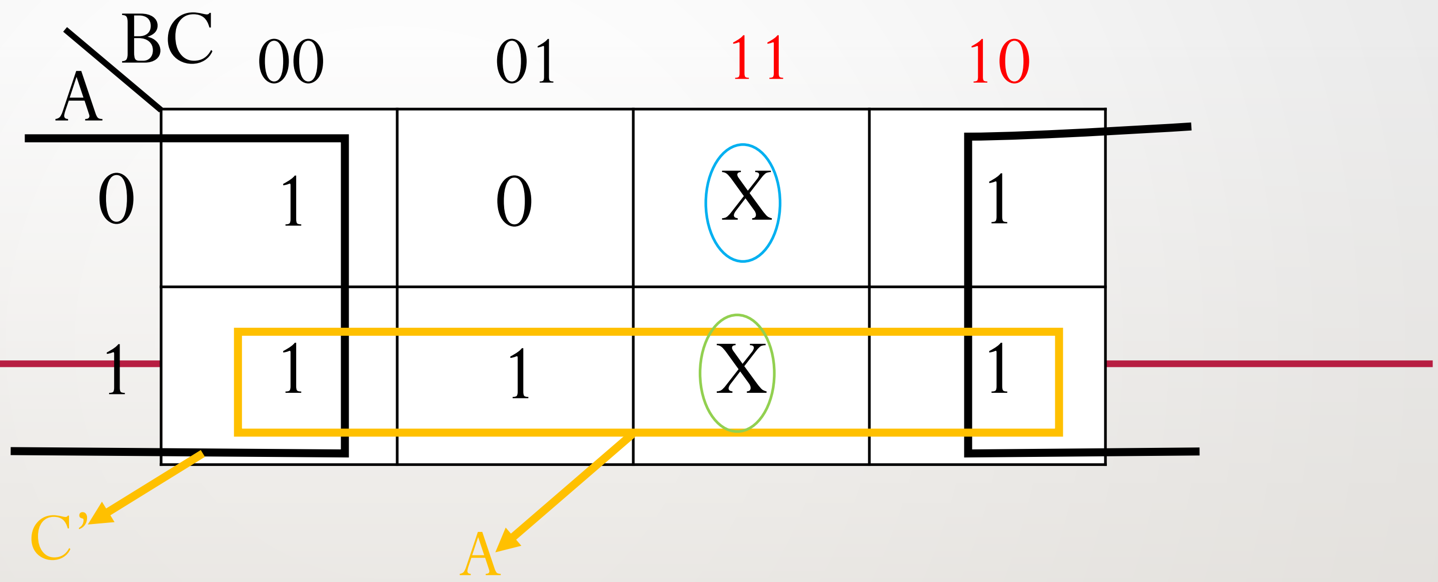
Don’t care Conditions in Karnaugh Maps (K-Maps)

- In some applications the output is not specified for certain combinations of inputs.
- **Don’t Care conditions :** we simply don’t care what output is generated for unspecified input cases.
- Don’t care conditions can be used for further simplification.

Example of 3-Variable K-Maps with Don't Care conditions

Given F (A,B,C) = ∑ (0,2,4,5,6) + d (3,7)

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	X

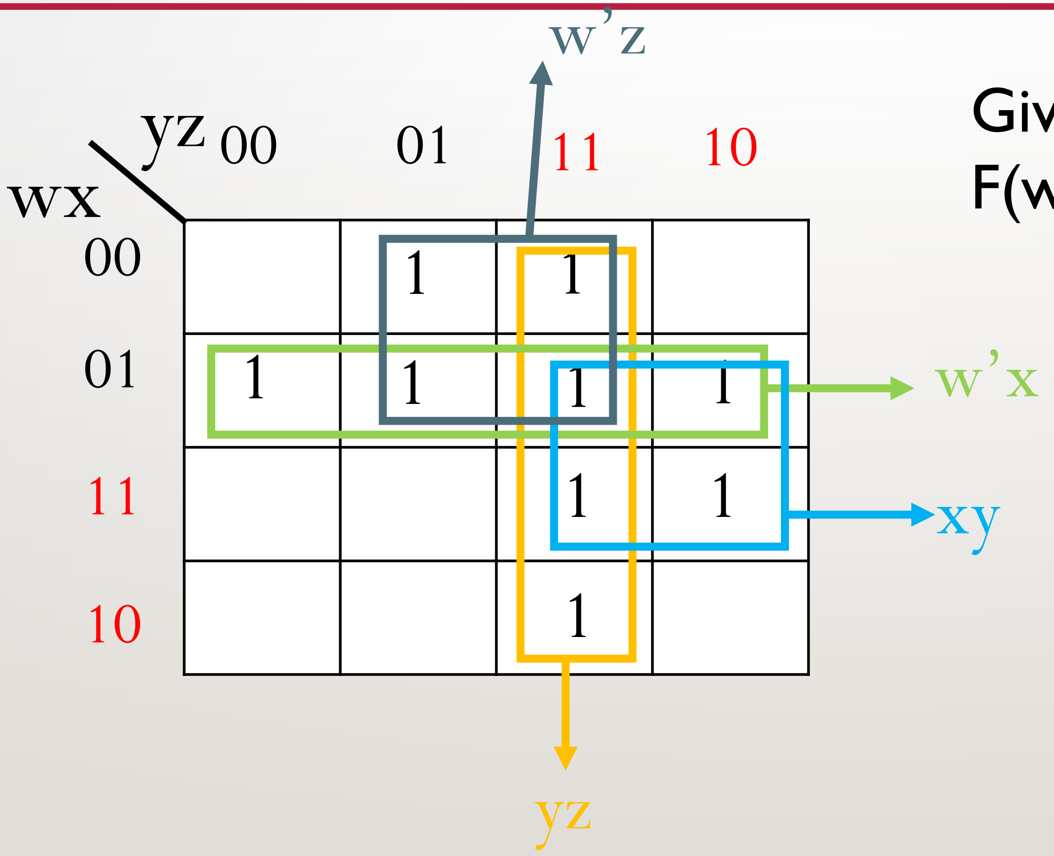


X Considered as 1 if it helps in reducing the terms or literals

X taken as 0 and neglected if it does not reduce terms or literals

Minimized expression F = C'+ A

Example of 4-Variable Karnaugh Maps (K-Maps)



Given

$F(w,x,y,z) = \sum(1,3,4,5,6,7,11,14,15)$

Simplified expression is

F = w'x + yz + xy + w'z

Example of 4-Variable K-Maps with Don't Care conditions

F (w, x, y, z) = ∑(1, 3, 7, 11, 15) which has the don't-care conditions: *d (w, x, y, z)* = (0, 2, 5)

WX \ YZ	00	01	11	10
00	X	1	1	X
01	0	X	1	0
11	0	0	1	0
10	0	0	1	0

W'X'

YZ

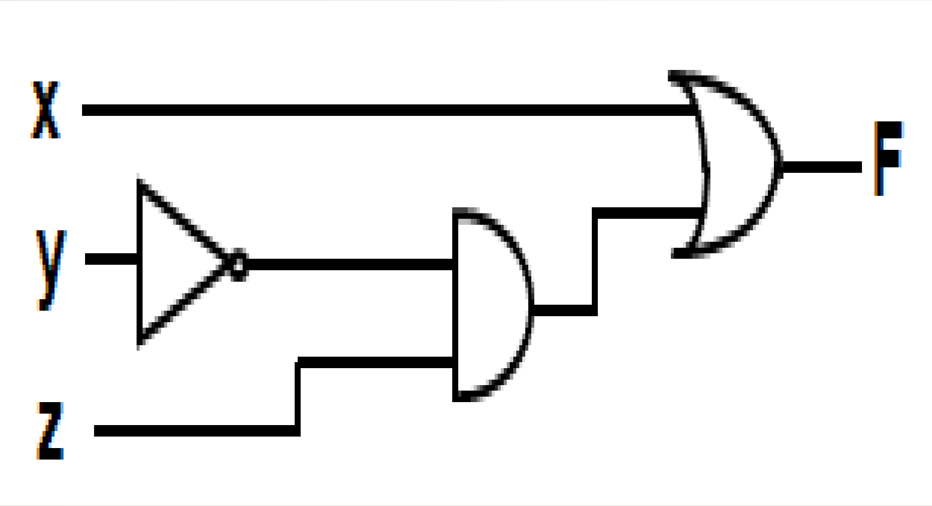
F= W'X' + YZ

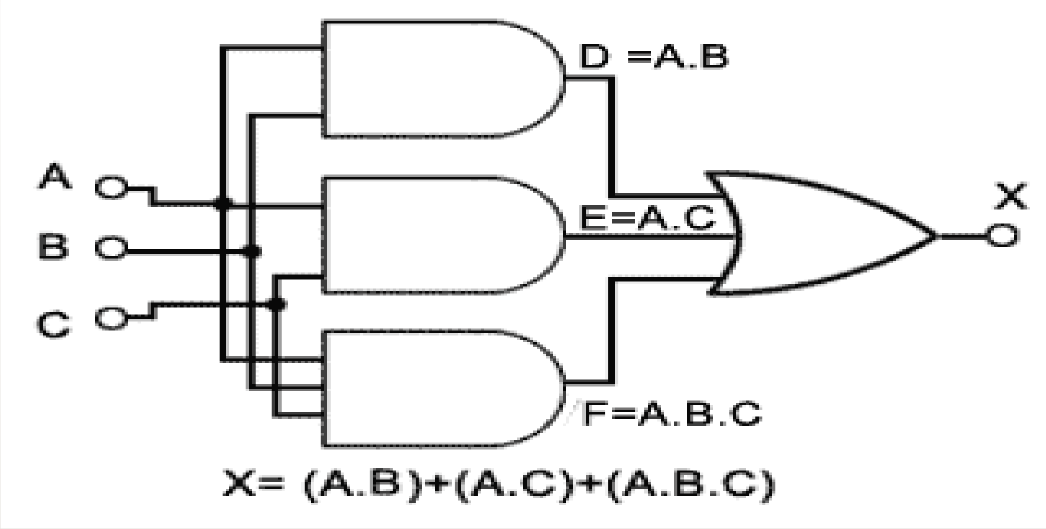
AB \ CD	00	01	11	10
00				
01				
11				
10				

Realization of Logic Diagram from Boolean function

1. Given F = x + y ' . z

2. Given X = (A.B) + (A.C) + (A.B.C)





SELF-ASSESSMENT QUESTIONS

1. What does SOP stand for in Digital Logic?

(a) Sum-of-Products
(b) Systematic Output Procedure
(c) Simplified Output Protocol
(d) Sum-of-Processes

2. Which notation is used to represent minterms in SOP expressions?

(a) A + B
(b) A * B
(c) Σ(A, B)
(d) ∏(A, B)

SELF-ASSESSMENT QUESTIONS

3. What is the primary goal of grouping in Karnaugh Maps?

(a) To make the map look organized

(b) To create larger groups

(c) To identify adjacent cells with '1'

(d) To separate '1' and '0' values

4. How many cells are in a 2-variable Karnaugh Map?

(a) 4

(b) 8

(c) 2

(d) 16

TERMINAL QUESTIONS

Short answer questions:

1. Develop a truth table that represents the Boolean equation. F = A'B'C + AB'C' + ABC' + ABC = ∑ m (1,4,6,7).

Long answer questions:

1. Optimize the four variable function F (A,B,C,D) = ∑m (0,1,4,5,6,10,13) + d (2,3) using K-Maps.
2. Represent the given expression in canonical POS form Y = (A + B)(B + C)(A + C)
3. Optimize the equation F (A, B, C) = AB'C + A'B'C + A'BC + A'B'C' + AB'C' using K-Maps and realize the resultant expression using logic gates.
4. Represent the given expression in canonical SOP form Y = AC + AB + BC.

TERMINAL QUESTIONS

Long answer questions:

5. Optimize the given function using K-map F (W, X,Y, Z) = ∑m (1, 3, 4, 5, 6, 7, 11, 14, 15) and implement using logic gates.
6. Optimize the 4 variable function F (W,X,Y,Z) = ∑m (1,3,7,11,15) + d (0,2,5) using K-Maps and realize the minimized expression using logic gates.

REFERENCES FOR FURTHER LEARNING OF THE SESSION

Reference Books:

1. Computer System Architecture by M. Moris Mano
2. Fundamentals of Digital Logic with Verilog HDL by Stephen Brown and ZvonkoVranesic

Sites and Web links:

1. https://www.geeksforgeeks.org/introduction-of-k-map-karnaugh-map/
2. https://www.gatevidyalay.com/tag/k-map-sop-and-pos/#google_vignette

THANK YOU

(DEEMED TO BE UNIVERSITY)

Team – Digital Design & Computer Architecture