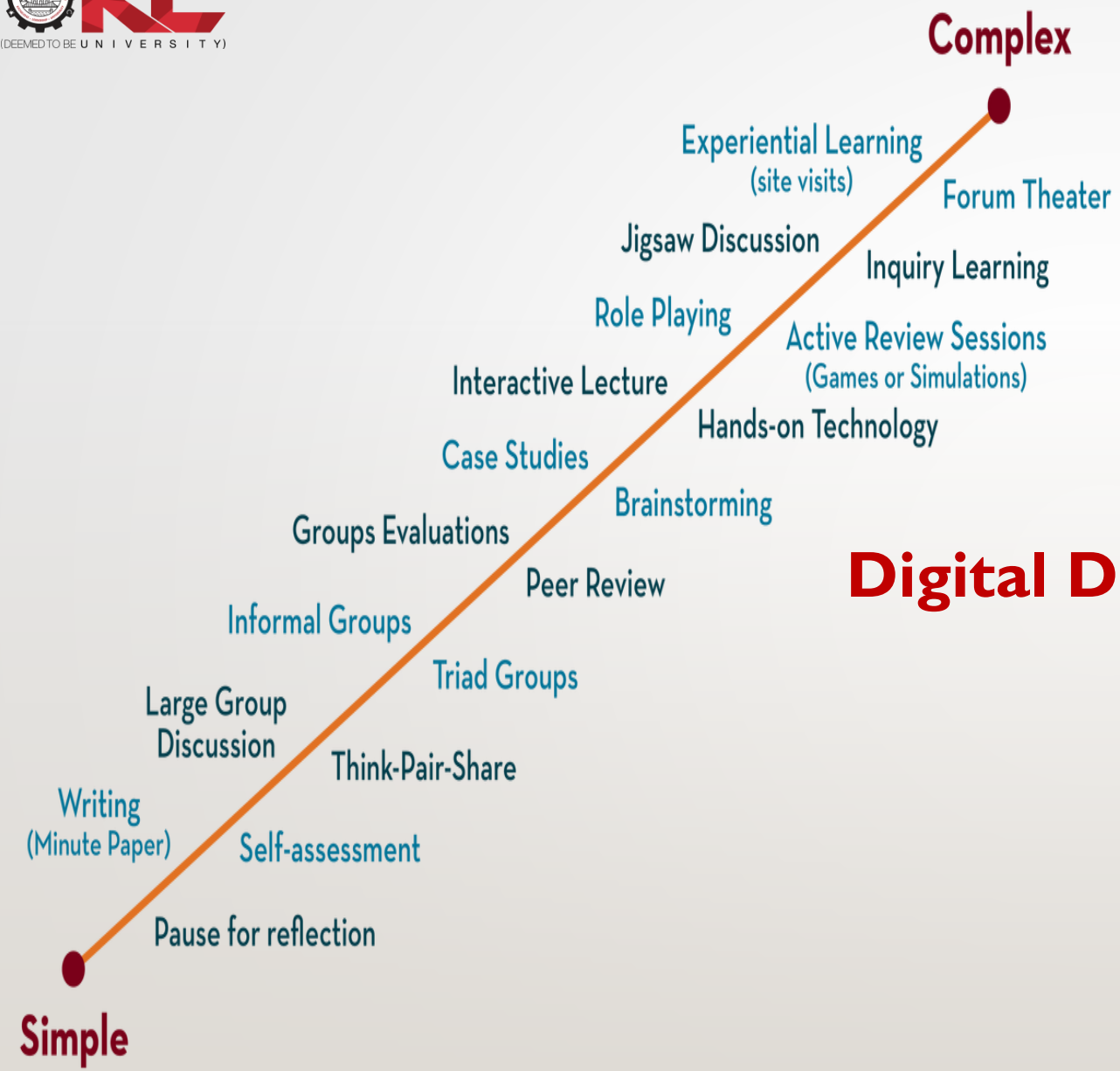


Department of BES-II

Digital Design and Computer Architecture
23EC1202

Topic:

CPLD & FPGA

Session No: 9 & 10

AIM OF THE SESSION

To familiarize students with the basic concept of CPLD & FPGA design.

INSTRUCTIONAL OBJECTIVES

This Session is designed to:

1. Discuss about other Programmable Logic Devices CPLD and FPGA
2. Design implement complex logic functions using CPLD and FPGA.
3. Differences between CPLD and FPGA.

LEARNING OUTCOMES

At the end of this session, you should be able to:

1. Define CPLD, FPGA and difference between them.
2. Design complex functions using CPLD and FPGA.

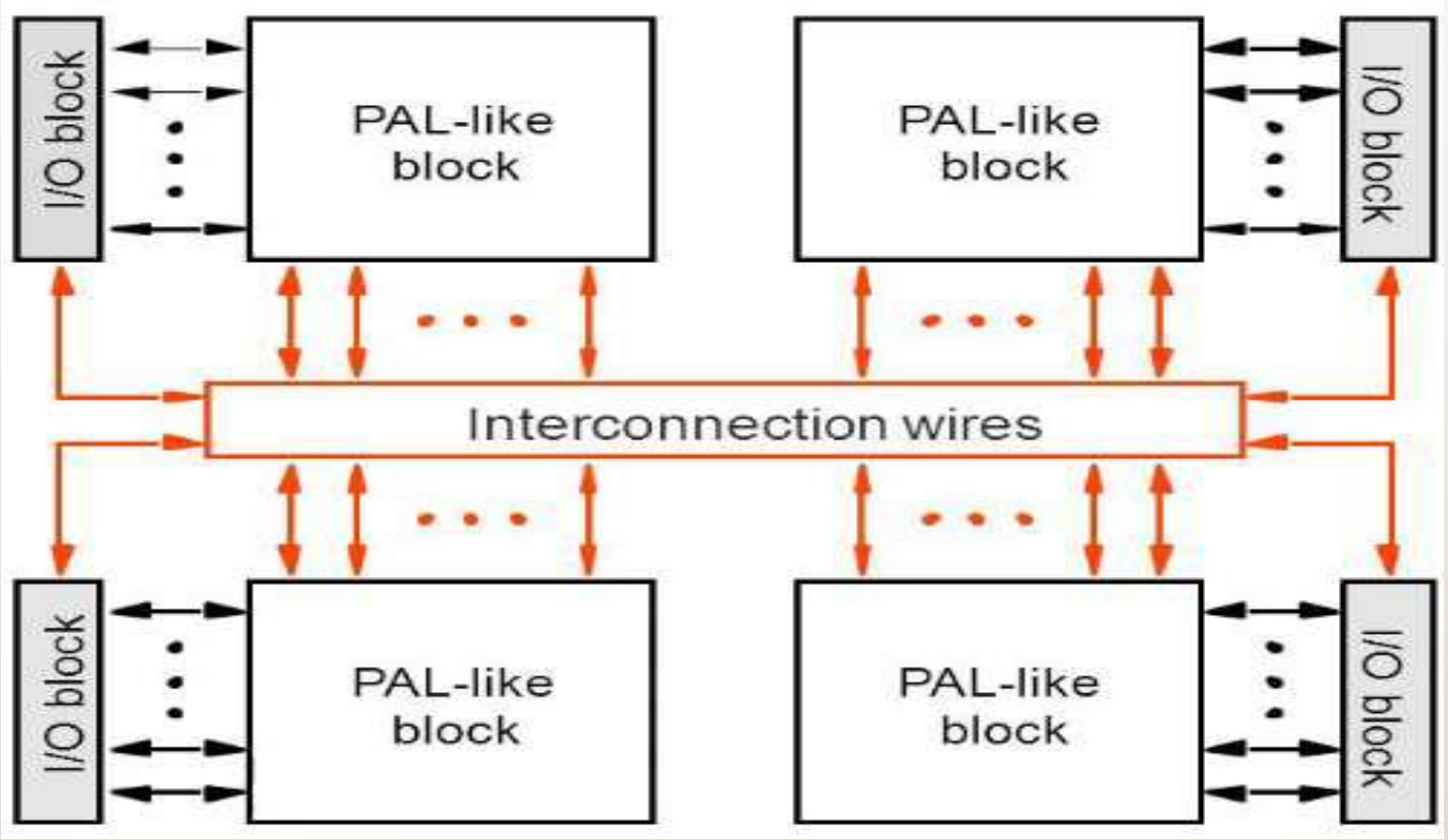
WHY CPLDS?

- SPLDs have limitations in terms of the number of input product terms and outputs, which restricts their use in applications such as traffic controllers and memory mapping.
- For industries requiring a higher number of inputs, outputs, or product terms—like commercial, automotive, and industrial automation found in cars and electronic devices—PLDs can be expanded by cascading them to meet these demands.

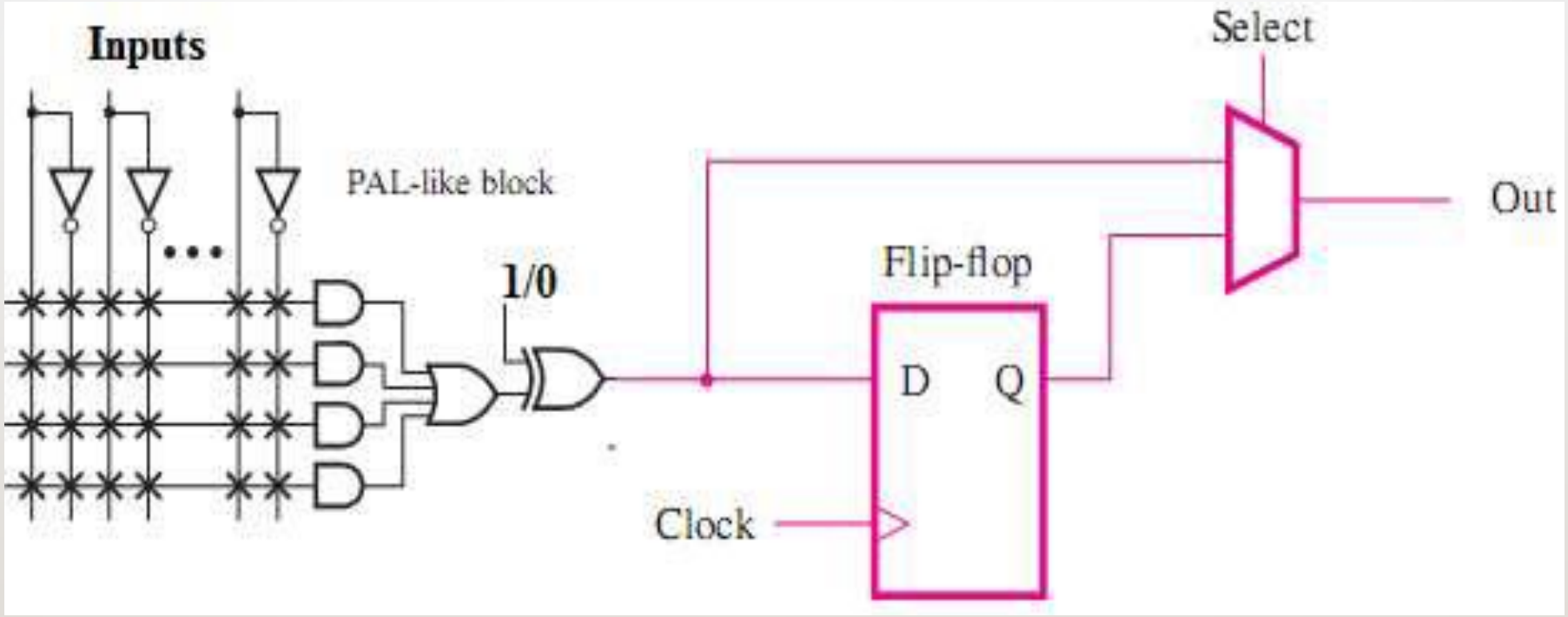
CPLD

- CPLD stands for Complex Programmable Logic Device.
- It is a type of programmable logic device that integrates multiple programmable logic blocks (like programmable array Logic(PAL)) and a programmable interconnect that interconnects on a single chip.
- CPLDs are used **to implement digital logic circuits and can be reprogrammed multiple times.**
- They offer a flexible and cost-effective solution for designing complex digital systems.

ARCHITECTURE OF CPLD

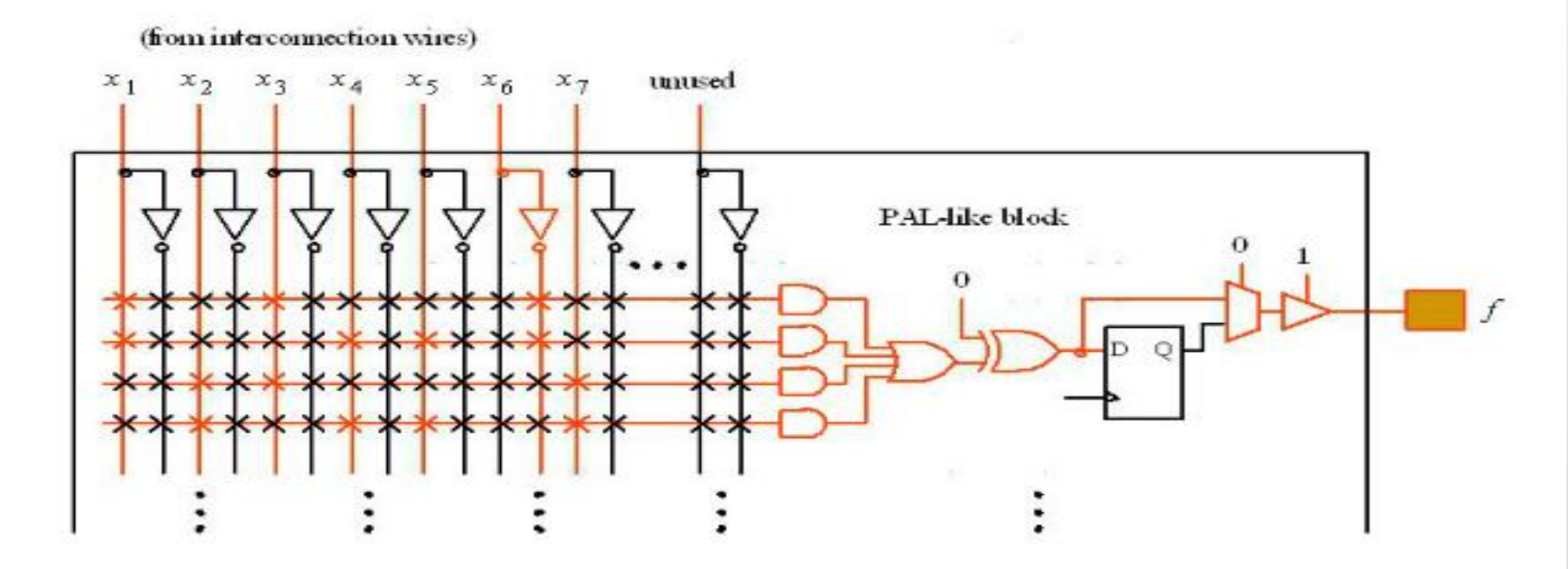


Internal Structure of a PAL like Block (Macro Cell)

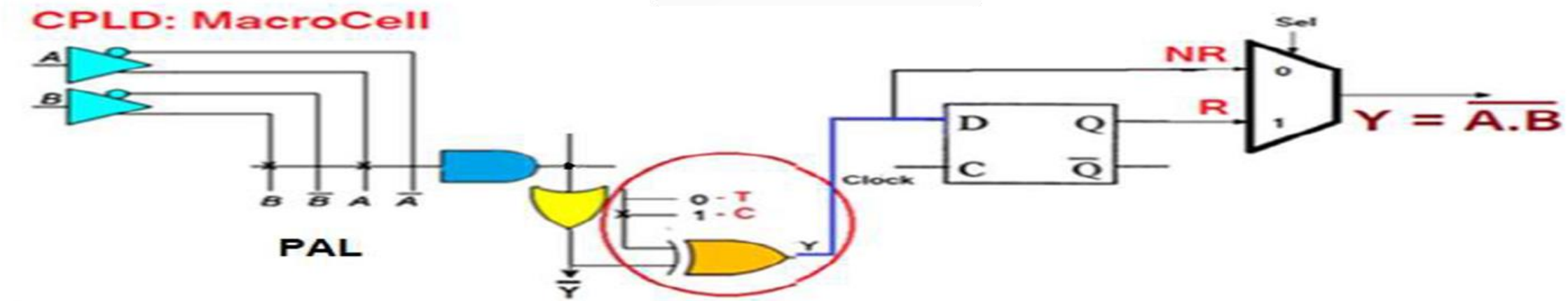


Implementation using CPLD

Example: Implement the given Boolean function using CPLD. $F = x_1 x_3 x_6' + x_1 x_4 x_5 x_6' + x_2 x_3 x_7 + x_2 x_4 x_5 x_7$



Problem 2: Implement the Boolean function Y = (A.B) ' = ∑ m (0,1,2) using macro-cell.



A	B	CLK	NR	R	SEL	Y
0	0	0	1	Z	0	1
0	1	0	1	Z	0	1
1	0	0	1	Z	0	1
1	1	0	0	Z	0	0
1	0	0	1	Z	1	Z

A	B	CLK	NR	R	SEL	Y
0	0	1	1	1	1	1
0	1	1	1	1	1	1
1	0	1	1	1	1	1
1	1	1	0	0	1	0
1	0	0	1	Z	0	1

Applications of CPLD

- CPLDs are ideal for high performance, critical control applications.
- CPLDs are used to implement control logic in embedded systems.
- CPLDs are employed in DSP applications to enable parallel processing, optimizing the execution of algorithms that require simultaneous data processing.
- CPLDs are utilized to implement complex state machines, enabling efficient control and sequencing of operations in applications such as communication protocols and digital controllers.

WHY FPGAS?

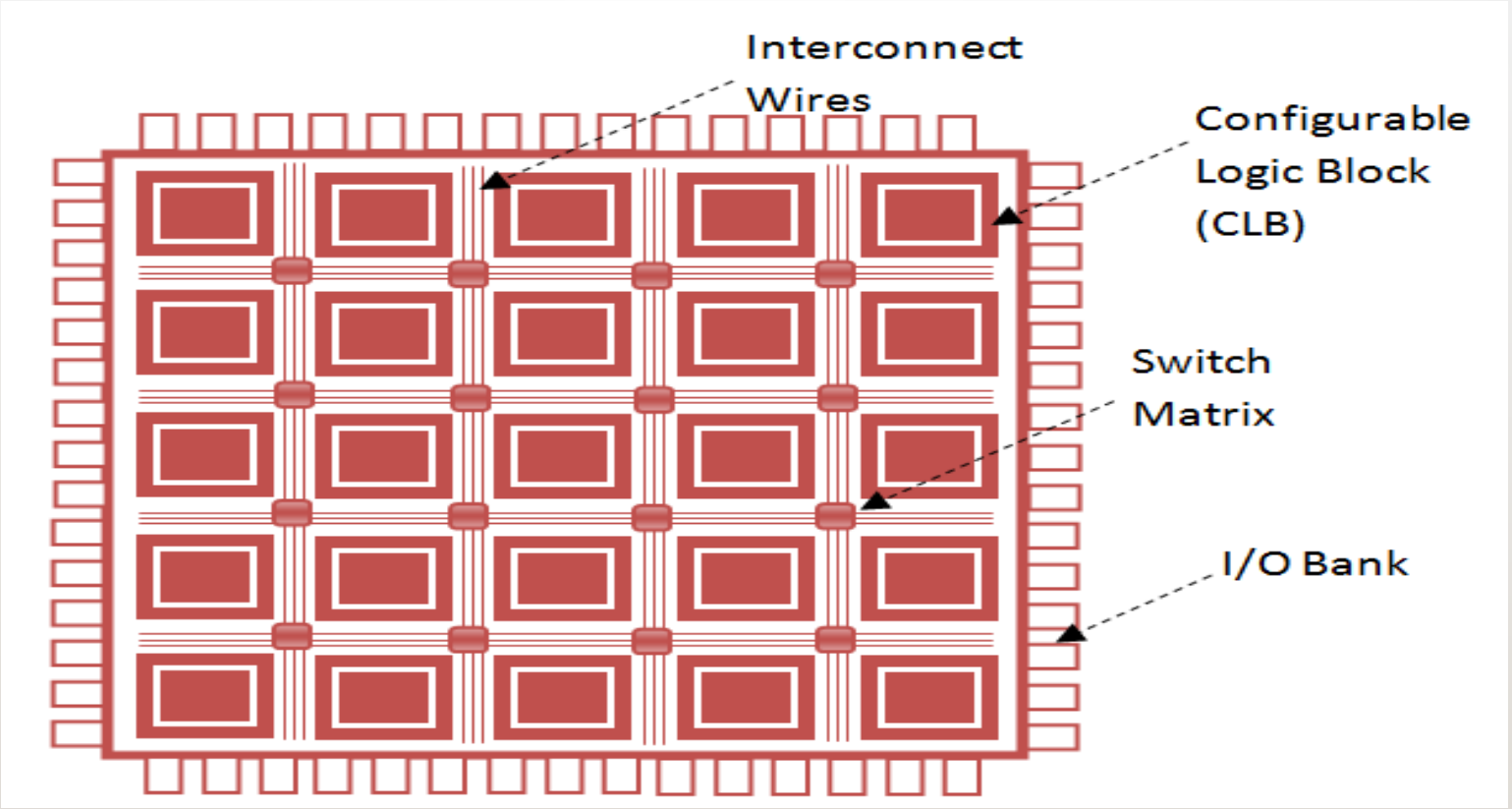
- CPLDs are faster and more power-efficient for simple logic operations.
- FPGAs have higher logic density and are better for complex logic operations.
- FPGAs are more flexible, scalable, and suitable for larger tasks.
- FPGAs usually more expensive than CPLDs due to their size and integration.
- FPGAs are used in data processing, storage, signal processing, instrumentation, and telecommunications.

FPGA

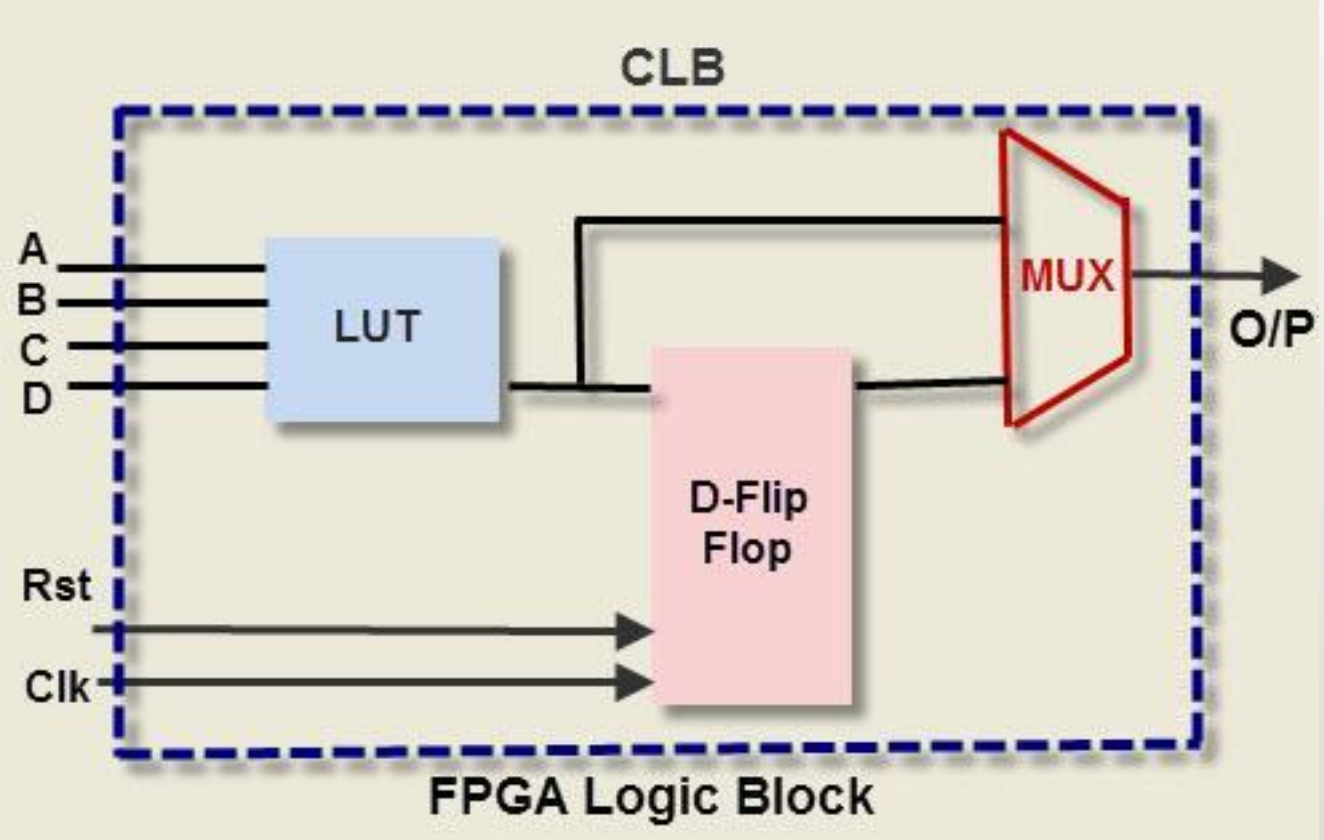
- A Field Programmable Gate Array has an entire logic system integrated on a single chip. It offers excellent flexibility for reprogramming to the system designers.
- The general FPGA architecture consists of three types of modules.

  I/O blocks or Pads , Switch Matrix/ Interconnection Wires, Configurable logic blocks (CLB)
- CLB (Configurable Logic Block) contains MUX, D flip flop and LUT which implements the user logic.
- LUT is useful for combinational logical function implementation; the MUX is used for selection logic, and D flip flop stores the output of the LUT.

FPGA Architecture

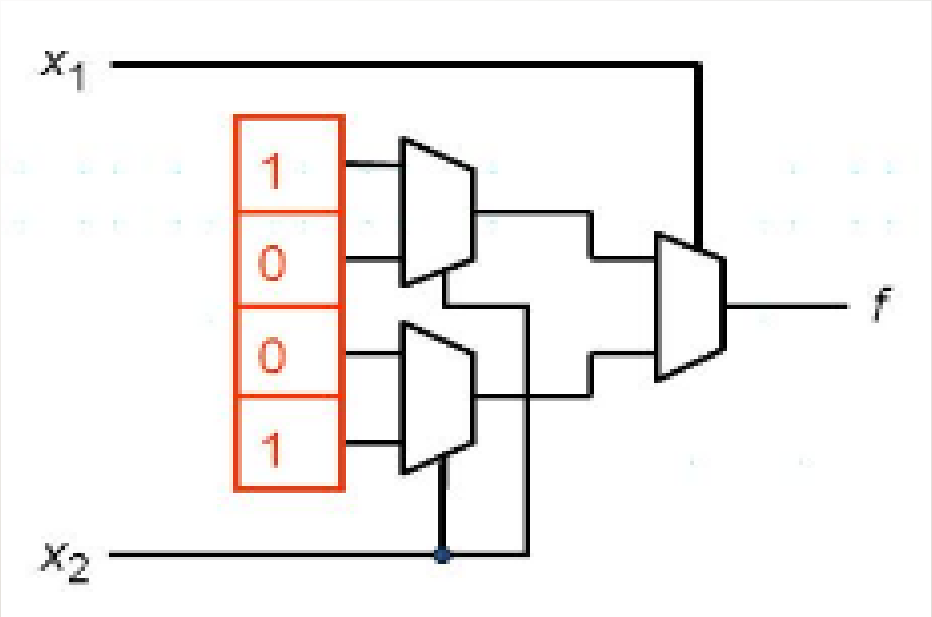


Configurable Logic Block (CLB)



Look-Up Table (LUT)

- LUTs comprise of 1-bit SRAM cells to hold either '0' or '1" and a set of multiplexers.
- The number of inputs available for a LUT determine its size.
- In general, a LUT with *n* inputs comprise of 2^n single-bit SRAM memory cells followed by a 2^n -1 multiplexers.



Use an FPGA with 2 input LUTS to implement the function,

$$f = x_1x_3x_6' + x_1x_4x_5x_6' + x_2x_3x_7 + x_2x_4x_5x_7$$

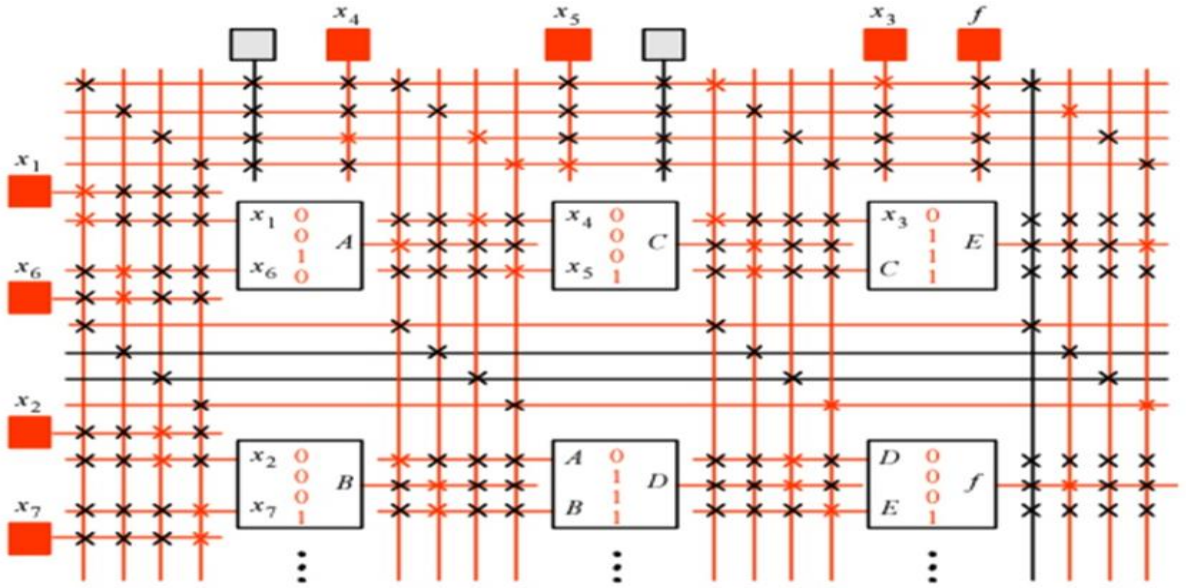
Fan-in of expression is too large for FPGA. This was simple to do in a CPLD

Factor *f* to get sub-expressions with max fan-in = 2

$$f = x_1x_6'(x_3 + x_4x_5) + x_2x_7(x_3 + x_4x_5)$$

$$= (x_1x_6' + x_2x_7)(x_3 + x_4x_5)$$ (Implementation shown in figure)

Could use Shannon's expansion instead. Goal is to build expressions out of 2-input LUTs



Use an FPGA with 2 input LUTS to implement the function, $f = x_1x_3x_6' + x_1x_4x_5x_6' + x_2x_3x_7 + x_2x_4x_5x_7$

f can be written as $f = x_1x_6'(x_3 + x_4x_5) + x_2x_7(x_3 + x_4x_5) = (x_1x_6' + x_2x_7)(x_3 + x_4x_5)$

Goal is to build expressions out of 2-input LUTs

$F= (x_1x_6' + x_2x_7)(x_3 + x_4x_5)$

f= (A + B) (x3 + C)

f= D . E

Here A block produces x_1x_6'

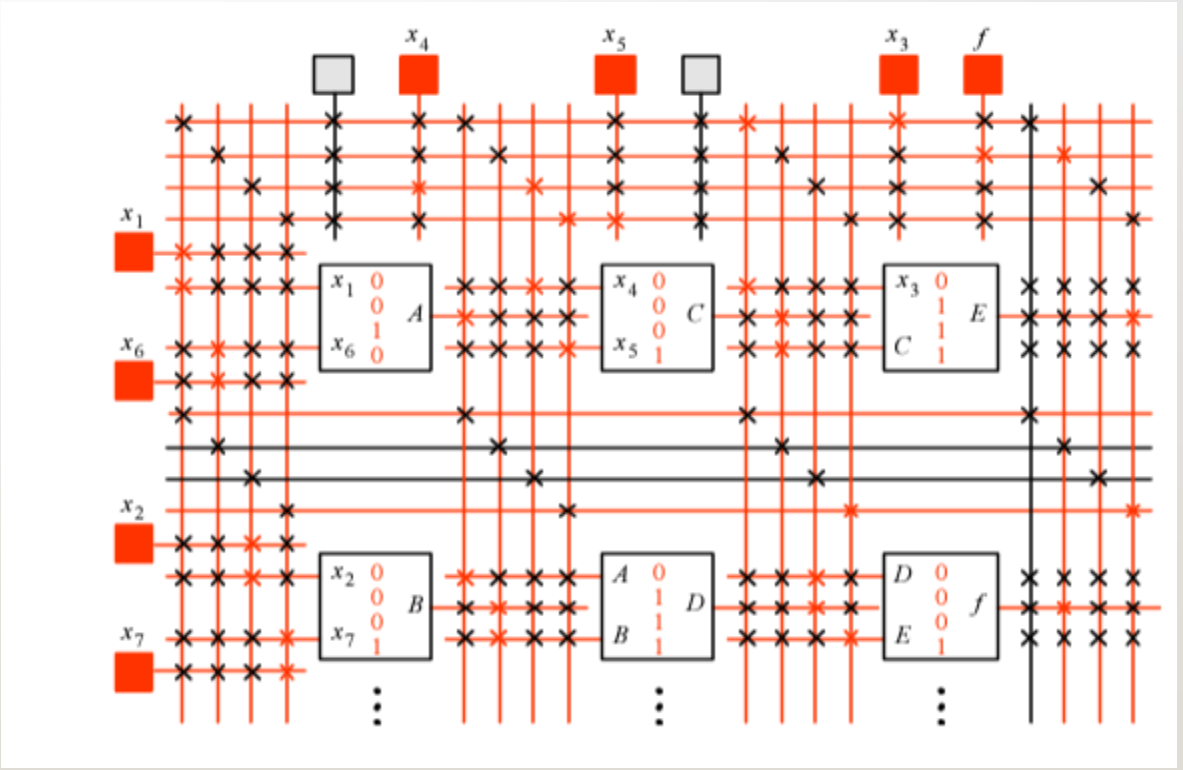
B block produces x_2x_7

C produces x_4x_5

D is Sum of A and B

E is sum of X_3 and C

last f= D.E

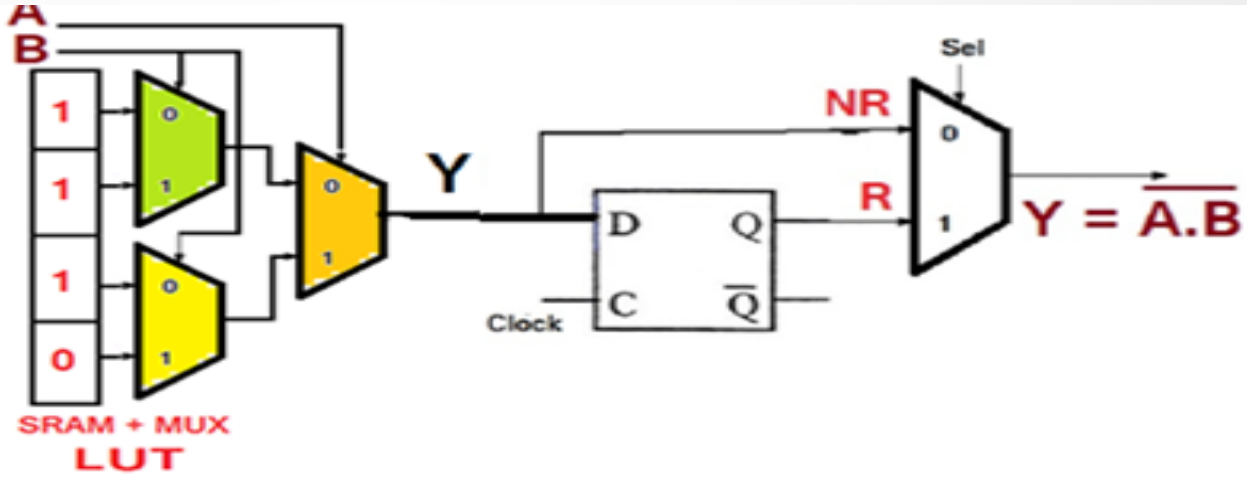


Implementation of CLB in FPGA

Example: Implement the CLB for the given Boolean function Y=(A.B)‘ or Y(A,B)= ∑m(0,1,2)

FPGA: CLB

A	B	Σm	Y
0	0	0	1
0	1	1	1
1	0	2	1
1	1	3	0
NAND Gate			



A	B	CLK	NR	R	SEL	Y
0	0	0	1	Z	0	1
0	1	0	1	Z	0	1
1	0	0	1	Z	0	1
1	1	0	0	Z	0	0
1	0	0	1	Z	1	Z

A	B	CLK	NR	R	SEL	Y
0	0	1	1	1	1	1
0	1	1	1	1	1	1
1	0	1	1	1	1	1
1	1	1	0	0	1	0
1	0	0	1	Z	0	1

Applications of FPGA

- Implementation of random logic
- Reconfigurable hardware
- Prototyping
- Special-purpose computation engines

CPLD (Vs) FPGA

Characteristics	CPLD	FPGA
Logic Cells	It has a small number of logic cells.	It has a large number of logic cells.
Interconnect Structure	It has a fixed interconnect structure.	It has a flexible interconnect structure.
Flexibility	Less Flexible	More Flexible
Cost	Low Cost	High Cost
Power Consumption	Less power consumption	Higher power consumption
Reconfigurability	Less reconfigurability	More reconfigurability
Density	Low to medium	Medium to high
Flip-flop ratios	Less flip-flop ratio	More flip-flop ratio
Applications	Best for simple applications	Best for complex applications

SUMMARY

- In conclusion, FPGAs contain a far higher number of logic cells and a more flexible connection topology, making them better suited for larger, more complicated designs.
- They provide greater reconfigurability and can serve a broader range of applications. Their more complex architecture can result in longer design times, higher prices, and higher power consumption.
- CPLDs feature fewer logic cells and are best suited for simpler logic functions and smaller designs.
- They have a simpler architecture with a set connecting structure, which can result in quicker design times and reduced costs. They also consume less electricity and are better suited for low-volume production runs.

SELF-ASSESSMENT QUESTIONS

1. The complex programmable logic device contains several PLD blocks and _____

a) A language compiler

b) AND/OR arrays

c) Global interconnection matrix

d) Field-programmable switches

2. Which type of device FPGA are?

a) SLD

b) SROM

c) EPROM

d) PLD

SELF-ASSESSMENT QUESTIONS

3. In FPGA, vertical and horizontal directions are separated by _____

a) A line

b) A channel

c) A strobe

d) A flip-flop

4. SPLDs, CPLDs, and FPGAs are all which type of device?

a) PAL

b) PLD

c) EPROM

d) SRAM

TERMINAL QUESTIONS

Short answer questions:

1. Draw the architecture of a Complex Programmable Logic Device (CPLD) and its key components.
2. Discuss the role of macro cells in CPLD architecture.

Long answer questions:

1. Design a Configurable Logic Block (CLB) for the given Boolean function $Y(A,B) = \Sigma m(0,1,2)$.
2. Illustrate the flexibility and programmability enabled by configuring Look-Up Tables (LUTs) in FPGAs.
3. Compare and contrast CPLD and FPGA architectures.
4. Illustrate the internal structure of Macrocell in CPLD using D Flip-flop and give the insights.

THANK YOU

(DEEMED TO BE UNIVERSITY)

Team – Digital Design & Computer Architecture