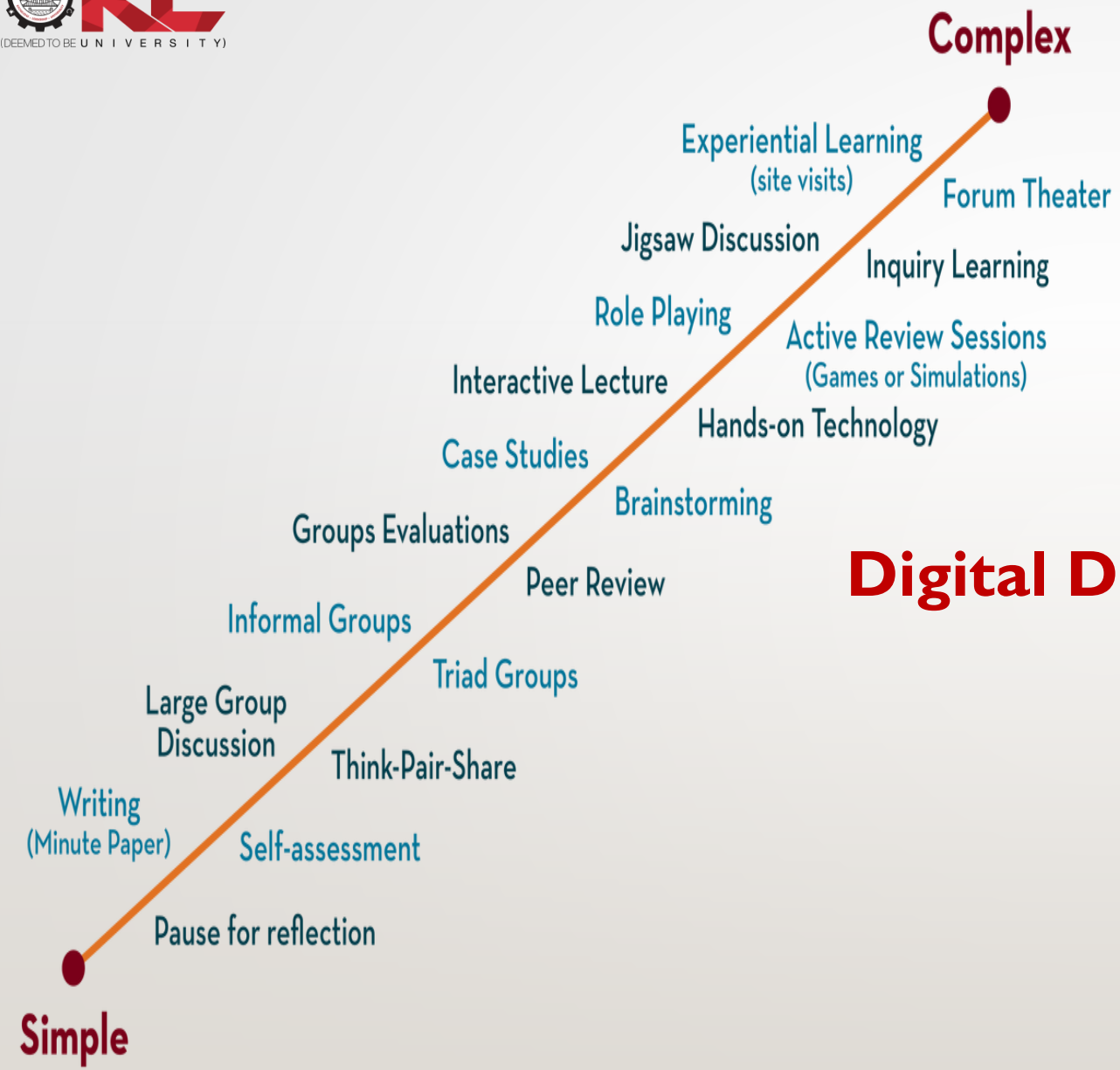


Department of BES-II

Digital Design and Computer Architecture

23EC1202

Topic:

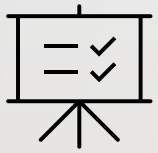
PAL and PLA design

Session No: 08

AIM OF THE SESSION

To familiarize students with the basic concept of PAL and PLA design

INSTRUCTIONAL OBJECTIVES



This Session is designed to:

1. Discuss about other Programmable Logic Devices like PAL and PLA
2. Design implement complex logic functions using PAL and PLA.
3. Differences between PAL and PLA.

LEARNING OUTCOMES

At the end of this session, you should be able to:

1. Define PAL,PLA and difference between them.
2. Design complex functions using PAL and PLA

SESSION INTRODUCTION

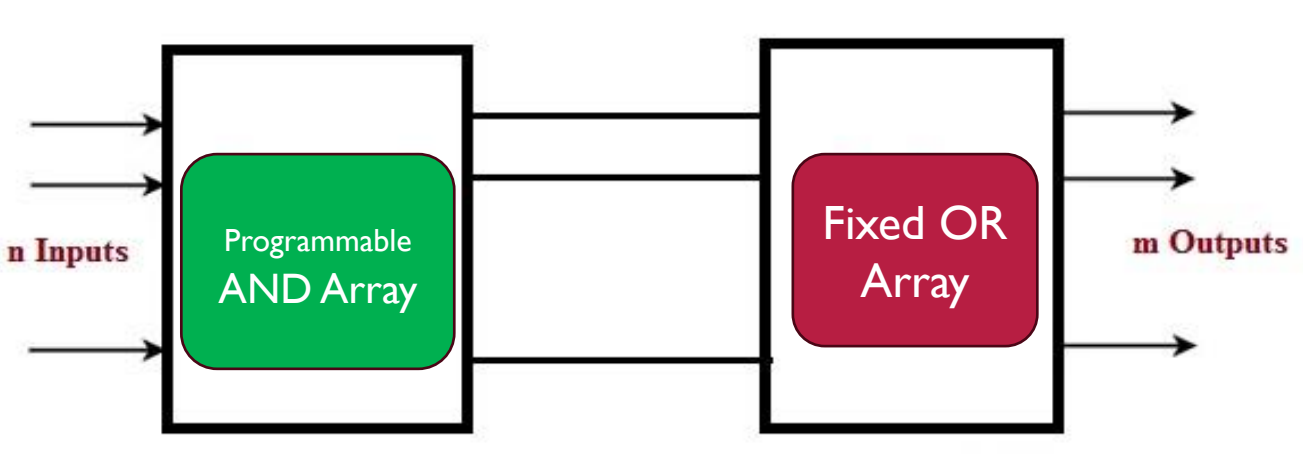
What are PAL and PLA?

- Both Programmable Array Logic and Programmable Logic Array are types of PLDs (programmable logic devices), and these are mainly used for designing combination logic mutually by sequential logic.

- The main difference among these two is that **PAL** can be designed with a collection of AND gates and fixed collection of OR gates whereas **PLA** can be designed with a programmable array of AND as well as OR gate.

Programmable Array Logic

- PAL is a programmable logic device that has Programmable AND array & fixed OR array.
- The advantage of PAL is that we can generate only the required product terms of Boolean function instead of generating all the min terms by using programmable AND gates.

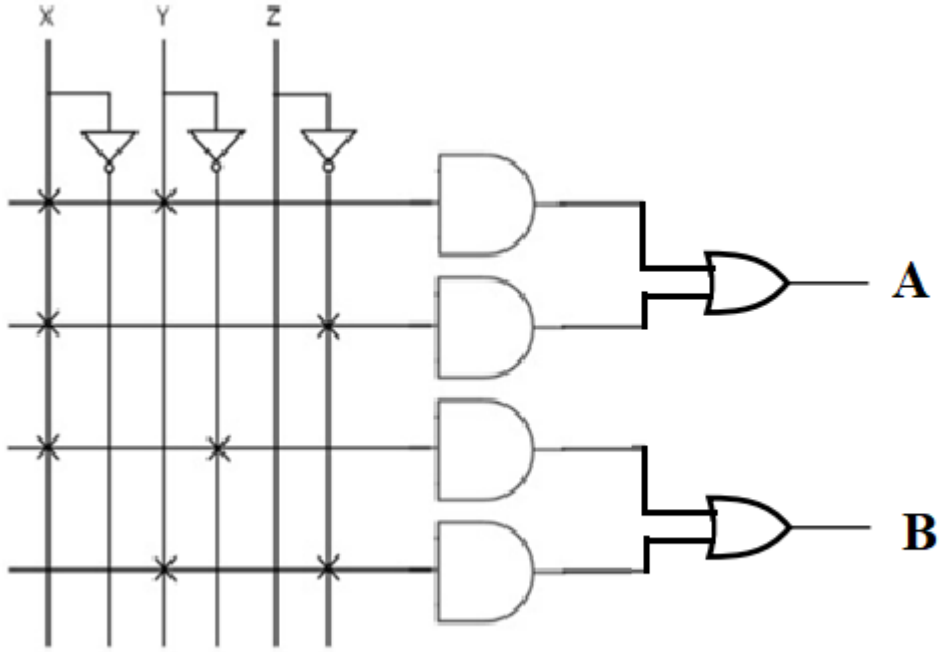


Implementation using Programmable Array Logic

Example: Implement the following Boolean functions using PAL.

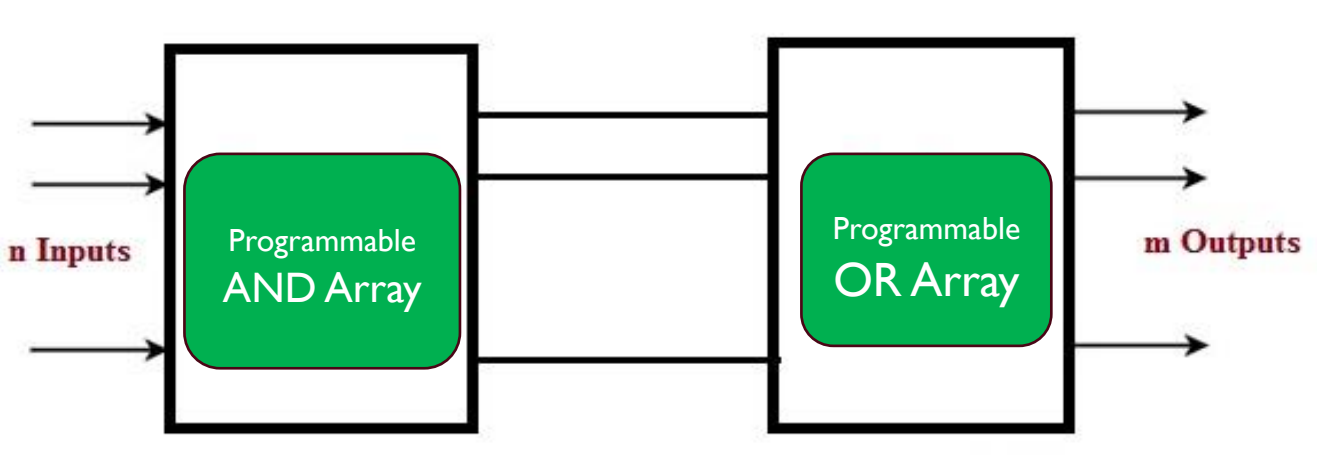
$$A = XY + X\overline{Z} \qquad B = X\overline{Y} + Y\overline{Z}$$

Here, we require four programmable AND gates & two fixed OR gates for producing those two functions.



Programmable Logic Array

- PLA is a programmable logic device that has both Programmable AND array & Programmable OR array.
- We can generate the required product terms and required sum terms by using AND gates and OR gates.

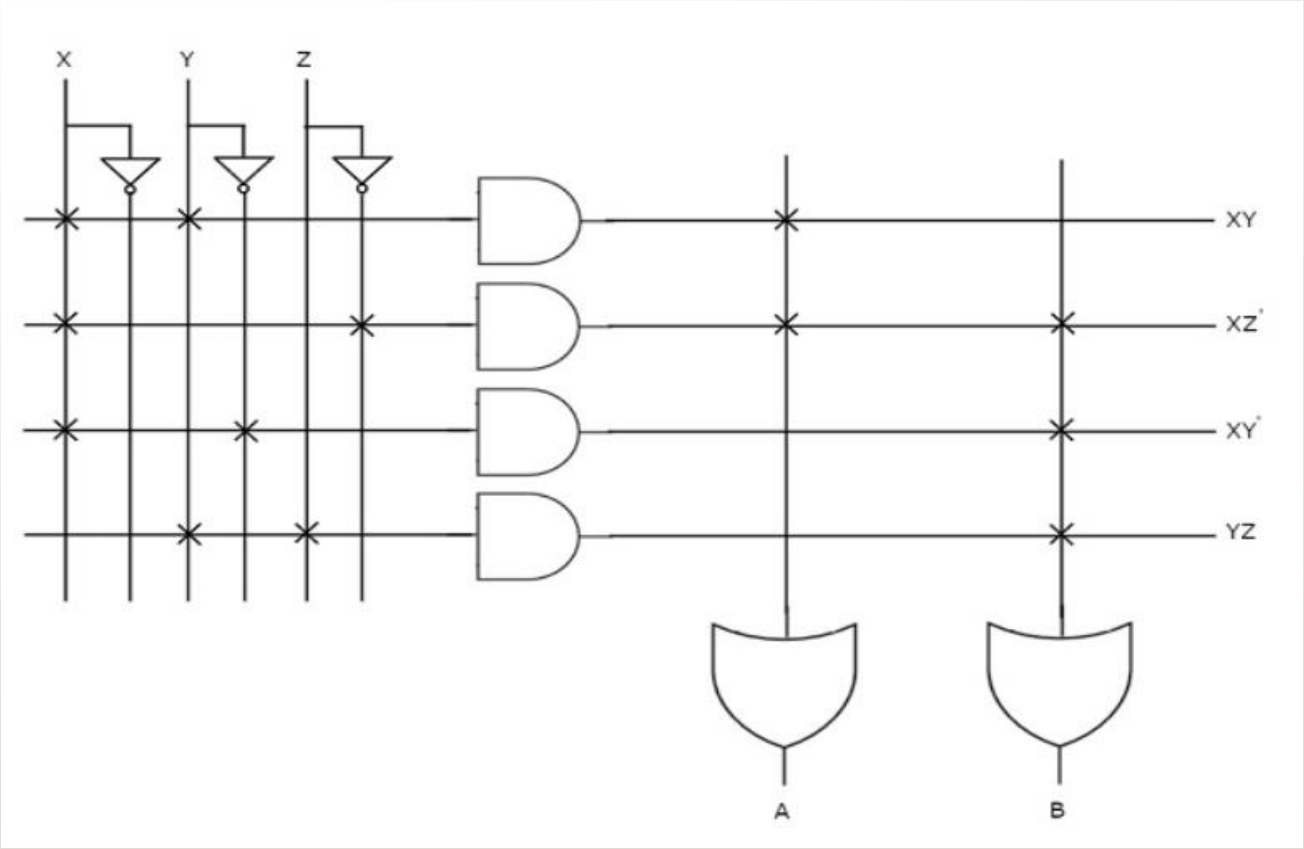


Implementation using Programmable Logic Array

Example: Implement the following Boolean functions using PLA.

$$A = XY + X\overline{Z} \qquad B = X\overline{Y} + YZ + X\overline{Z}$$

One product term, Z'X is common in each function. So, we require four programmable AND gates & two programmable OR gates for producing those two functions.



ACTIVITIES/ CASE STUDIES/ IMPORTANT FACTS RELATED TO THE SESSION

Implement Full Adder by using PAL

SUM = $\bar{A}.\bar{B}.C + A.\bar{B}.\bar{C} + \bar{A}.B.\bar{C} + A.B.C$

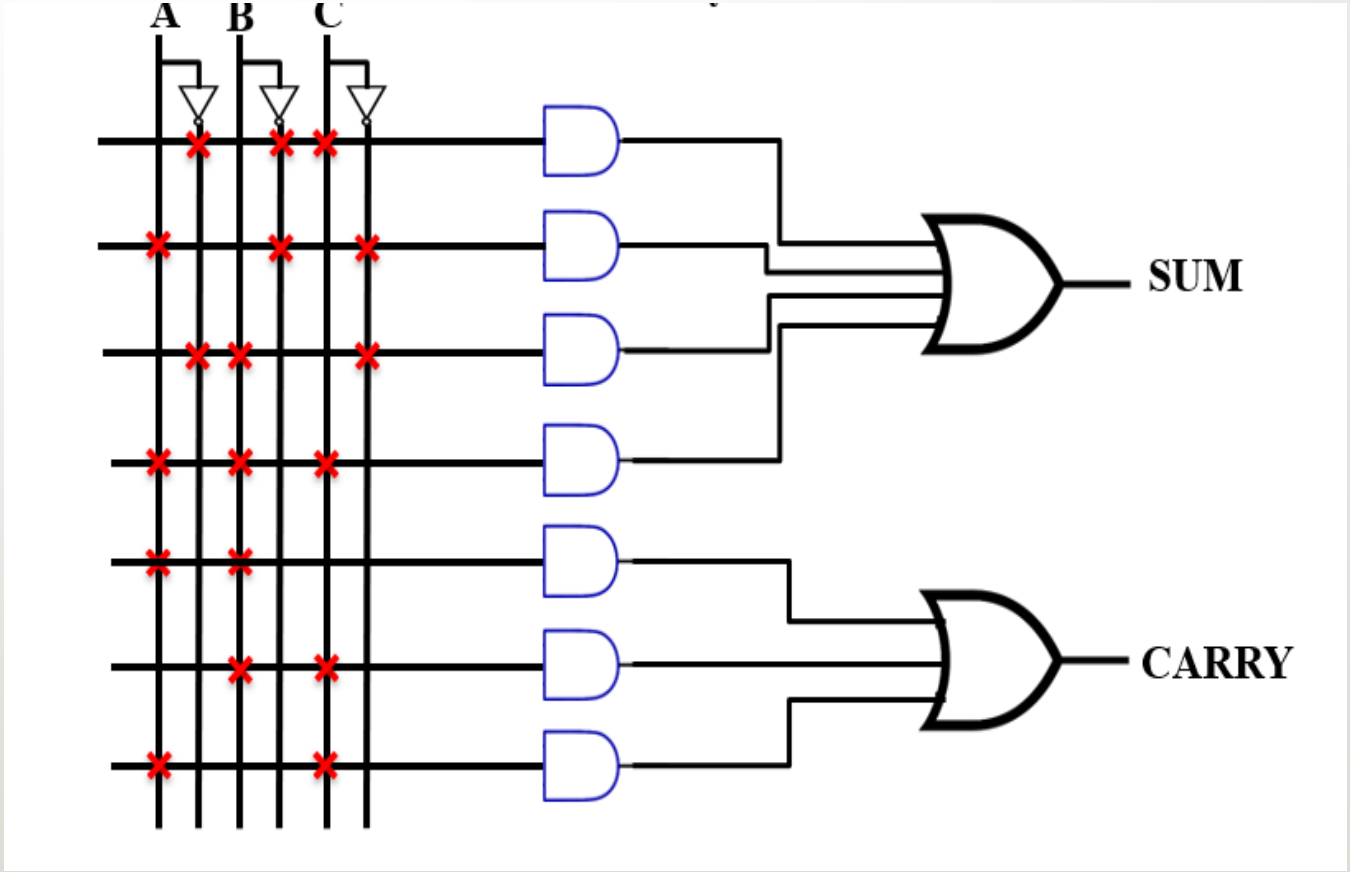
Carry = AB + BC + AC

Min Term	AND Inputs			Outputs
	A	B	C	
$\bar{A}.\bar{B}.C$	0	0	1	SUM = $\bar{A}.\bar{B}.C + A.\bar{B}.\bar{C} + \bar{A}.B.\bar{C} + A.B.C$
$A.\bar{B}.\bar{C}$	1	0	0	
$\bar{A}.B.\bar{C}$	0	1	0	
A.B.C	1	1	1	
AB	1	1	-	Carry = AB + BC + AC
BC	-	1	1	
AC	1	-	1	

CONTINUED ..

SUM = $\bar{A}.\bar{B}.C + A.\bar{B}.\bar{C} + \bar{A}.B.\bar{C} + A.B.C$

Carry = AB + BC + AC



ACTIVITIES/ CASE STUDIES/ IMPORTANT FACTS RELATED TO THE SESSION

Implement Full Adder by using PLA

SUM = $\bar{A}.\bar{B}.C + A.\bar{B}.\bar{C} + \bar{A}.B.\bar{C} + A.B.C$

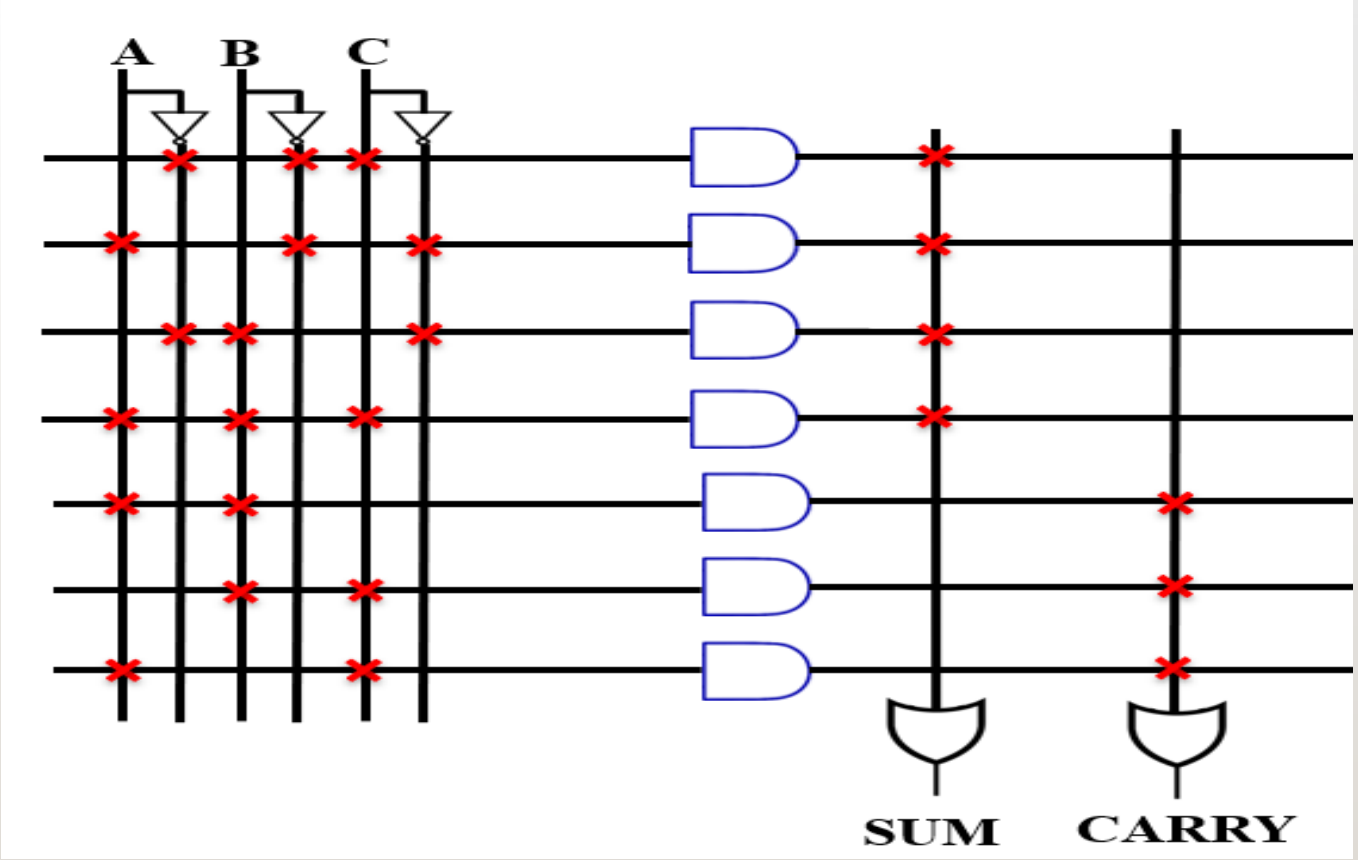
Carry = AB + BC + AC

Min Term	AND Inputs			OR Outputs	
	A	B	C	SUM	CARRY
$\bar{A}.\bar{B}.C$	0	0	1	1	-
$A.\bar{B}.\bar{C}$	1	0	0	1	-
$\bar{A}.B.\bar{C}$	0	1	0	1	-
A.B.C	1	1	1	1	-
AB	1	1	-	-	1
BC	-	1	1	-	1
AC	1	-	1	-	1

Continued..

SUM = $\bar{A}.\bar{B}$.C + $A.\bar{B}.\bar{C}$ + $\bar{A}$.B.$\bar{C}$ + A.B.C

Carry = AB + BC + AC



Applications of PAL & PLA

PLA Applications:

- Versatile implementation of complex combinational logic functions.
- Commonly used in microprocessor design and arithmetic operations.
- Suitable for the implementation of control units in digital systems.

PAL Applications:

- Applied in scenarios requiring simpler combinational logic functions.
- Commonly used in memory address decoding.
- Cost-effective solution for applications with less complex logic requirements.
- Suitable for the implementation of straightforward control circuits.

Differences Between PROM, PAL & PLA

S. No.	PROM	PAL	PLA
1	AND array is fixed and OR array is programmable	OR array is fixed and AND array is programmable	Both AND and OR arrays are programmable
2	Cheaper and simple to use	Moderate cost and simpler	Costliest and complex than PAL and PROMs
3	Fast read access (fixed content)	Less flexible than PLA (fixed OR plane)	Slower (due to full programmability)
4	Very limited Flexibility (only stores data)	Any Boolean function in SOP form can be implemented using PLA	Fully flexible logic implementation

SELF-ASSESSMENT QUESTIONS

1. PLA contains _____

a) AND and OR arrays

b) NAND and OR arrays

c) NOT and AND arrays

d) NOR and OR arrays

2. A PLA is similar to a ROM in concept except that _____

a) It hasn't capability to read only

b) It hasn't capability to read or write operation

c) It doesn't provide full decoding to the variables

d) It hasn't capability to write only

SELF-ASSESSMENT QUESTIONS

3. The difference between a PAL & a PLA is _____

a) PALs and PLAs are the same thing
b) The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane
c) The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane
d) The PAL has more possible product terms than the PLA

4. If a PAL has been programmed once _____

a) Its logic capacity is lost
b) Its outputs are only active HIGH
c) Its outputs are only active LOW
d) It cannot be reprogrammed

TERMINAL QUESTIONS

Short answer questions:

1. Sketch a basic block diagram for a Programmable Array Logic (PAL) device.
2. Sketch the block diagram for a Programmable Logic Array (PLA) device.

Long answer questions:

1. Design the following Boolean functions using PAL. A (X,Y,Z) = Sum of Even Numbers (include Zero also) and B (X,Y,Z) = Sum of Odd Numbers
2. Design the circuit with a PLA having three inputs and two outputs. i) F1 (A, B, C) = ∑m (3, 5, 6, 7) ii) F2 (A, B, C) = ∑(0, 2, 4, 7)
5. Compare and contrast PROM, PAL & PLA using schematic diagrams.

REFERENCES FOR FURTHER LEARNING OF THE SESSION

Reference Books:

1. Computer System Architecture by M. Moris Mano
2. Fundamentals of Digital Logic with Verilog HDL by Stephen Brown and ZvonkoVranesic

Sites and Web links:

1. https://www.tutorialspoint.com/digital_circuits/digital_circuits_programmable_logic_devices.htm
2. https://www.geeksforgeeks.org/programming-array-logic/
3. https://www.electrically4u.com/programmable-array-logic/

THANK YOU

(DEEMED TO BE UNIVERSITY)

Team – Digital Design & Computer Architecture