DDCA – CO 3 & 4 - SHORT ANSWERS TERMINAL QUESTIONS AND ANSWERS

1. What are the common types of operands, give examples.

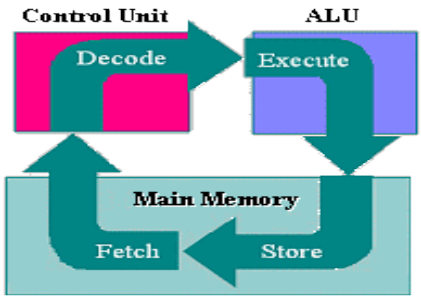
Operands are values used in arithmetic or logical operations. Common types include integers, floating point numbers, and booleans.

Example: In the operation x = y + z,

y and z are the operands. The computer retrieves their values from memory, performs the addition, and stores the result in x.

2. What is the role of the fetching phase in a machinecycle.

The fetching phase in a machine cycle retrieves the next instruction from memory for execution by the CPU.



3. Highlight the advantages of hardwired realization.

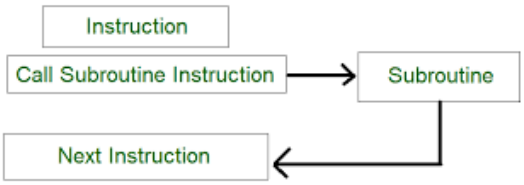
- **Speed:** Hardwired realization offers faster execution of instructions since the control signals are directly generated by hardware circuits without the need for interpretation or sequencing.
- **Simplicity:** Hardwired control units typically have simpler designs compared to micro-programmed control units, leading to reduced complexity in the overall microprocessor architecture. This simplicity often results in lower cost and power consumption.

4. Highlight the advantages of microprogrammed realization.

- **Flexibility:** Microprogramming allows for easy modification and debugging of control signals without altering the hardware. This flexibility simplifies the design process and facilitates quick adaptation to changing requirements or debugging needs.
- **Reduced Hardware Complexity:** Microprogrammed control units typically require fewer hardware components compared to hardwired control units. This reduction in hardware complexity leads to lower production costs, decreased power consumption, and easier maintenance.

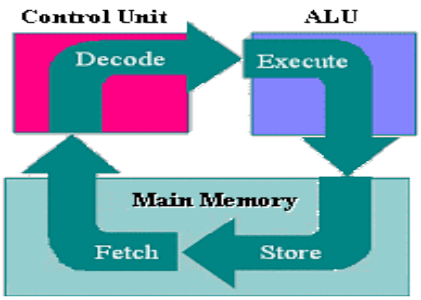
5. Specify the purpose of subroutine call in computerprogramming.

- The purpose of a subroutine call in computer programming is to execute a specific sequence of code that performs a particular task or function.



6. Explore the role of the decoding phase in a machinecycle.

- The decoding phase in a machine cycle interprets the instruction fetched from memory and determines the specific operation to be executed by the CPU.



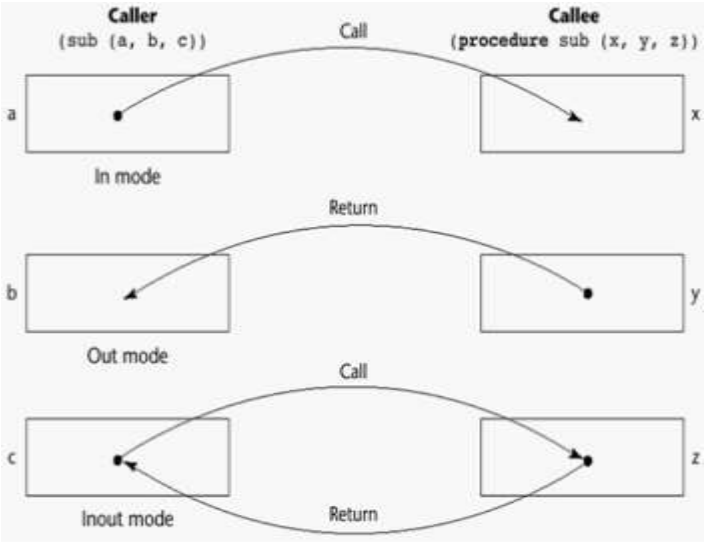
7. Illustrate the cause of structural hazards in pipelining.

- **Limited Resources:** When multiple instructions in the pipeline compete for the same hardware resource (like an ALU or register) in the same cycle, a conflict arises.
- **Resource Bottlenecks:** If a particular stage in the pipeline has a slower processing unit compared to others, it can create a bottleneck.

8. Explore the significance of a microprocessor in modern computing devices.

- **Central Processing Unit (CPU):** Microprocessors form the CPU of computing devices, performing arithmetic, logic, and control operations.
- **Versatility and Integration:** Microprocessors enable the integration of multiple functionalities onto a single chip, allowing for the creation of versatile and compact computing devices such as smartphones, tablets, and IoT devices.

9. Draw the illustration of subroutine call and return mechanism in computer programming.



10. Write the characteristics of a multicycle implementation in processor design.

- Reuse of Hardware Components
- Variable Execution Time
- Control Logic Complexity
- Efficiency and Performance

11. Identify the different types of RAM according to their characteristics.

- SRAM (Static RAM)
- DRAM (Dynamic RAM)
- DDR SDRAM (Double Data Rate Synchronous DRAM)
- LPDDR (Low Power DDR SDRAM)
- GDDR (Graphics Double Data Rate SDRAM)

12. Discuss cache performance and its purpose.

- Cache memory speeds up computer programs by storing frequently accessed data in a **faster** location closer to the CPU.
- The parameter of measuring cache performance is known as the Hit Ratio.
- Hit ratio = (Number of cache hits)/ (Number of searches)

13. Summarize potential reasons for buffering in IO operations.

- **Speed Mismatch:** Buffers bridge the gap between slow and fast devices. For example, a hard drive might be slow compared to the CPU.
- **Block Size Difference:** Devices often have different preferred data transfer sizes. Buffers act as an intermediary, allowing data to be transferred in larger blocks between devices and the CPU, optimizing performance.

14. Highlight various policies of cache data replacement.

- Least Recently Used (LRU)
- First-In, First-Out (FIFO)
- Random Replacement
- Least Frequently Used (LFU)
- Most Recently Used (MRU)
- Optimal Replacement

15. List the various data transfer methods in IO communication.

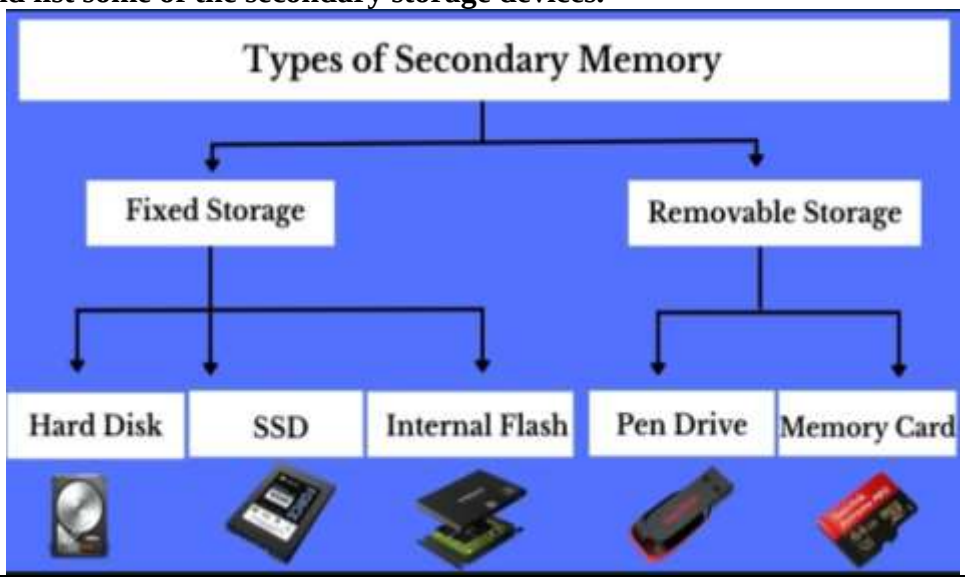
- Programmed I/O (PIO)
- Interrupt-Driven I/O
- Direct Memory Access (DMA)
- Memory Mapped I/O

16. Represent the use of virtual memory in computer system.

Virtual memory acts like a larger, **contiguous** memory space for programs even though physical RAM is limited. This allows:

- **Running larger programs:** By utilizing disk space as an extension of RAM, programs exceeding physical RAM capacity can still run.
- **Multitasking:** Multiple programs can be loaded partially into RAM, swapped with data on disk as needed, enabling efficient multitasking.

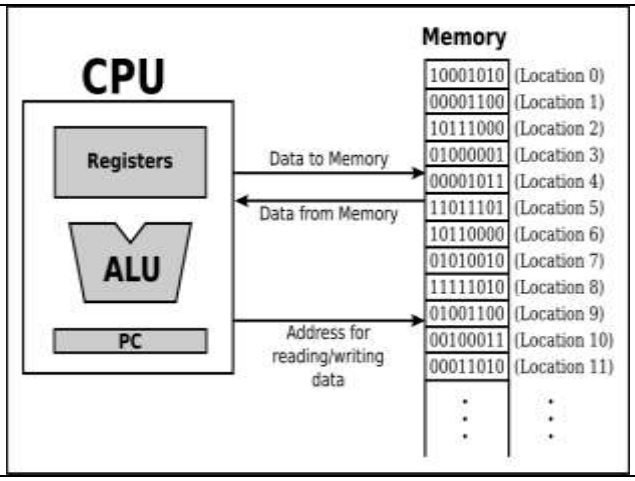
17. Identify and list some of the secondary storage devices.



18. Specify the role of memory cell in the context of memory organization.

- **Basic Storage Unit:** It's the fundamental unit that stores a single bit of data (0 or 1).
- **Building Block:** Groups of memory cells are combined to form words (e.g., 4 bits, 8 bits) which are the basic units of data transfer and addressing within the memory.

19. Sketch the memory addressing diagram.



20. List various types of buffering techniques.

- Single Buffering
- Double Buffering
- Circular buffering

21. Summarize various Asynchronous Data Transfer methods.

• **Strobe Control:** Uses a single control signal to synchronize data transfer. One device (sender or receiver) initiates the transfer with a strobe pulse, indicating the exact moment for data exchange.

• **Hand shaking:** Employs dedicated control signals for both sender and receiver. The sender transmits data along with a signal indicating its availability. The receiver acknowledges receipt with another signal, ensuring reliable data transfer.