

## DDCA – CO 1 – SHORT ANSWER QUESTIONS WITH ANSWERS

1. Apply Demorgan's theorem to the expression  $\overline{(A + B) \cdot (C + D)}$

$$\begin{aligned} F &= \overline{(A + B)} + \overline{(C + D)} \quad \text{By applying } \overline{A \cdot B} = \bar{A} + \bar{B} \\ &= \bar{A} \cdot \bar{B} + \bar{C} \cdot \bar{D} \quad \text{By applying } \overline{A + B} = \bar{A} \cdot \bar{B} \end{aligned}$$

2. Simplify the expression  $F = A B D + A B'$  using Boolean identities.

$$\begin{aligned} F &= A B D + A B' \\ &= A (B D + B') \\ &= A (B + B') \cdot (D + B') \\ &= A \cdot (D + B') \end{aligned}$$

3. Reduce  $A (A + B)$  to the least number of terms.

$$\begin{aligned} \text{Given } A (A + B) \\ &= A \cdot A + A \cdot B \\ &= A + A \cdot B \\ &= A \cdot (1 + B) \\ &= A \cdot 1 \\ &= A \end{aligned}$$

4. Simplify the expressions

$$F = A B' D + A B' D' \quad \& \quad F = \bar{A} \cdot (A + B) + A \cdot \bar{B}$$

$$\begin{aligned} \text{Given } F &= A B' D + A B' D' \\ &= A B' (D + D') \\ &= A B' \cdot 1 \\ &= A B' \end{aligned}$$

$$\begin{aligned} \text{Given } F &= \bar{A} \cdot (A + B) + A \cdot \bar{B} \\ &= \bar{A} \cdot A + \bar{A} \cdot B + A \cdot \bar{B} \\ &= 0 + \bar{A} \cdot B + A \cdot \bar{B} \\ &= A \oplus B \end{aligned}$$

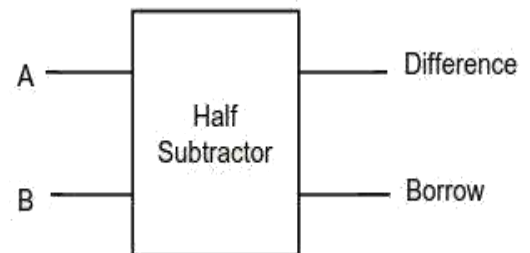
5. Develop a truth table that represents the Boolean equation.

$$F = A'B'C + AB'C' + ABC' + ABC = \sum m(1, 4, 6, 7)$$

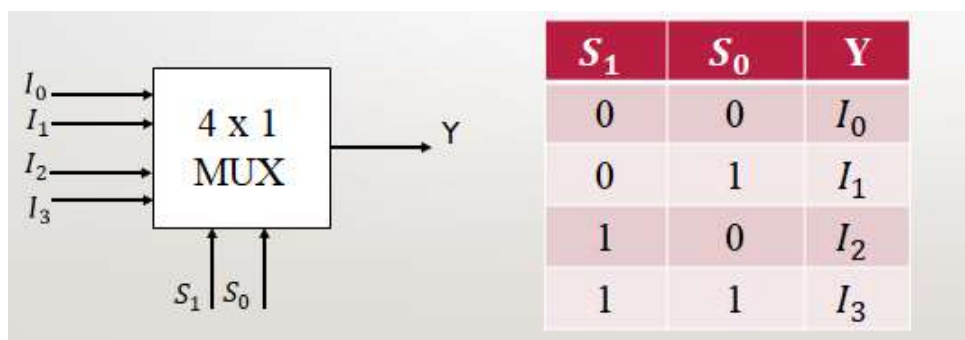
A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

6. Draw a half subtractor principle with input and output and truth table.

Inputs		Outputs	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0



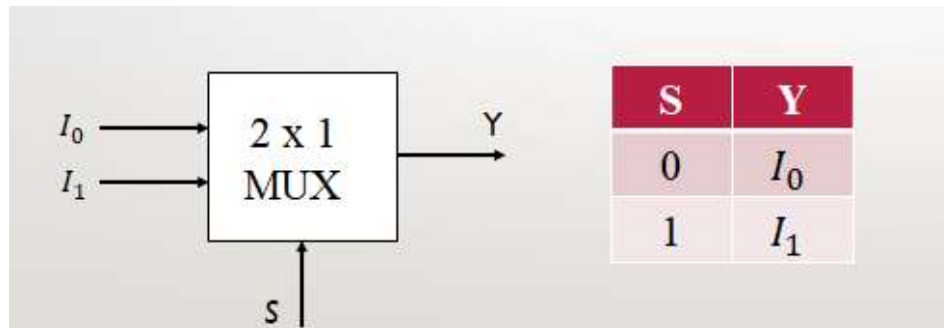
7. Provide the symbol and truth table for a 4-to-1 multiplexer.



8. In a 2-to-1 multiplexer, how many input lines are there, and how many control lines are required to select one of the inputs?

Data Inputs = 2

Control line/ select inputs to select the data inputs = 1



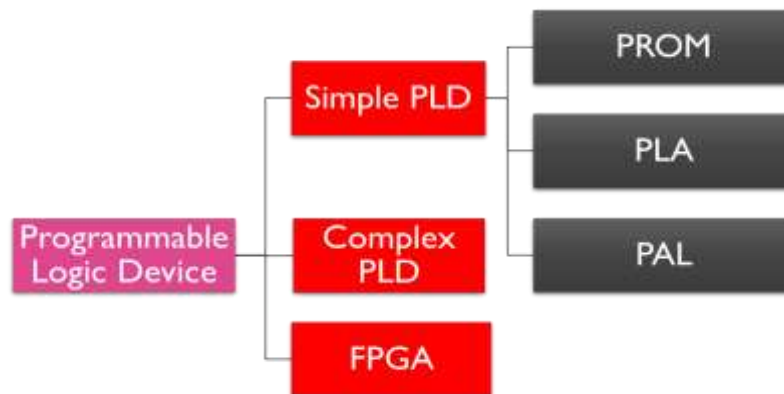
9. Draw the truth table of a 8:3 encoder.

$I_7$	$I_6$	$I_5$	$I_4$	$I_3$	$I_2$	$I_1$	$I_0$	$Y_2$	$Y_1$	$Y_0$
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

10. Name any two practical applications where an encoder is commonly used.

- **Remote Controls:** Encoders are commonly used in remote controls for various devices such as televisions, DVD players, and audio systems. They encode user input into digital signals that are transmitted wirelessly to the corresponding device for control.
- **Digital Communications:** Encoders play a vital role in digital communication systems, where they convert analog signals (such as voice or video) into digital format for transmission over communication channels like the internet, telephone lines, or radio waves.

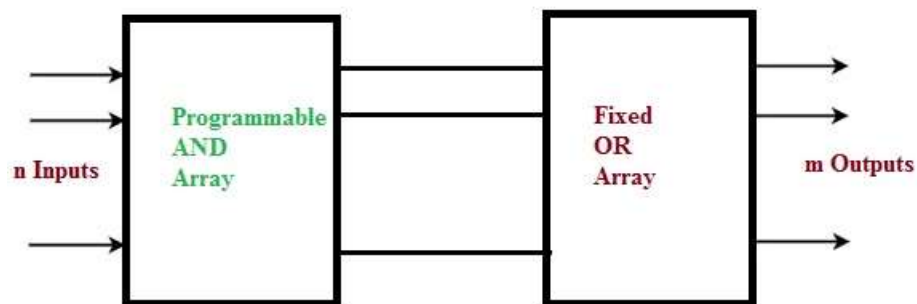
11. Draw the classification diagram of Programmable Logic Devices (PLDs).



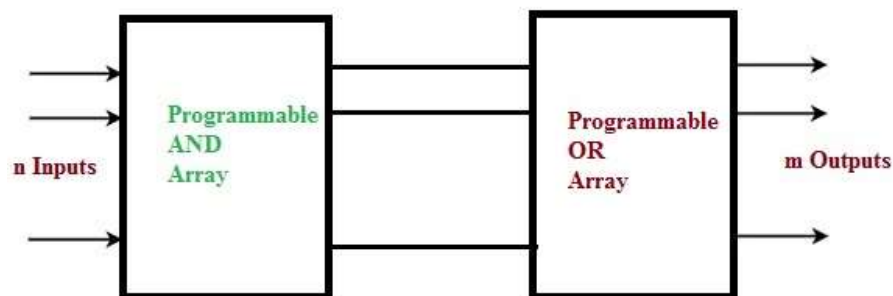
12. List the applications of PROM in digital circuit design, considering factors such as flexibility and reprogrammability.

- Look-Up Tables (LUTs)
- Custom Logic Functions
- Multiplexers and Decoders
- Digital Calibration
- Security Key Storage
- Data and Configuration Storage

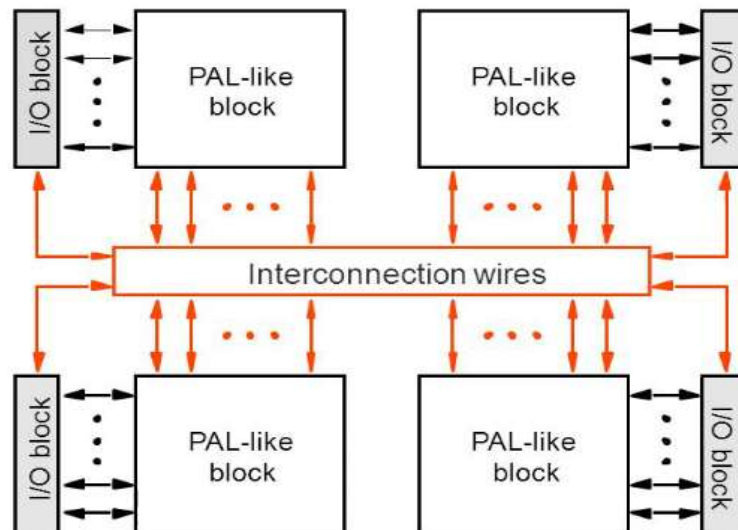
13. Sketch a basic block diagram for a Programmable Array Logic (PAL) device.



14. What is the schematic representation of a Programmable Logic Array (PLA)?



15. Draw the architecture of a Complex Programmable Logic Device (CPLD) and its key components.



16. Discuss the role of macro cells in CPLD architecture.

- **Customizable Logic Functions:** Macro cells in CPLD (Complex Programmable Logic Device) architecture are configurable blocks that can be programmed to implement specific logic functions, allowing designers to create custom logic circuits tailored to their application requirements.
- **Flexibility and Reconfigurability:** Macro cells provide flexibility by offering a variety of logic elements such as AND, OR, XOR gates, flip-flops, and registers. They can be interconnected and configured dynamically to perform different tasks, enabling the CPLD to adapt to changing system needs or design iterations without requiring hardware changes.