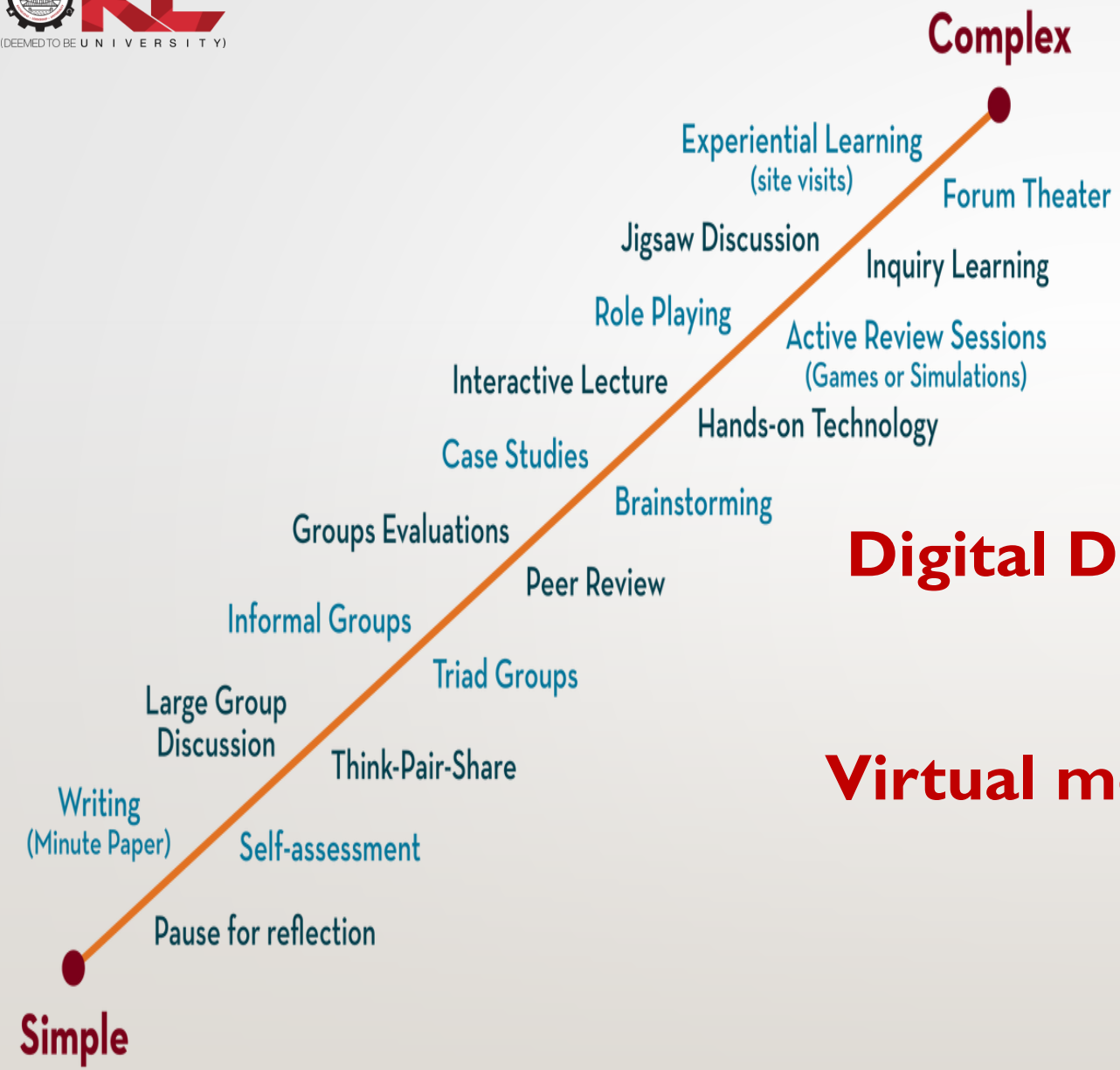


Department of BES-II

Digital Design and Computer Architecture

23EC1202

Topic:

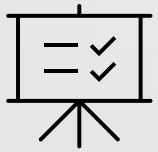
Virtual memory system: page table and TLB

Session No: 36

AIM OF THE SESSION

To familiarize students with the basic concept of Virtual memory System, Page table and TLB

INSTRUCTIONAL OBJECTIVES



This Session is designed to:

1. Demonstrate the virtual memory system
2. Describe the relation between page table and TLB
3. List out the types of addresses
4. Describe the mapping between addresses

LEARNING OUTCOMES

At the end of this session, you should be able to:

1. Define virtual memory system
2. Describe the page table and TLB
3. Summarize the virtual memory , relation between page table and TLB, mapping between the addresses

INTRODUCTION

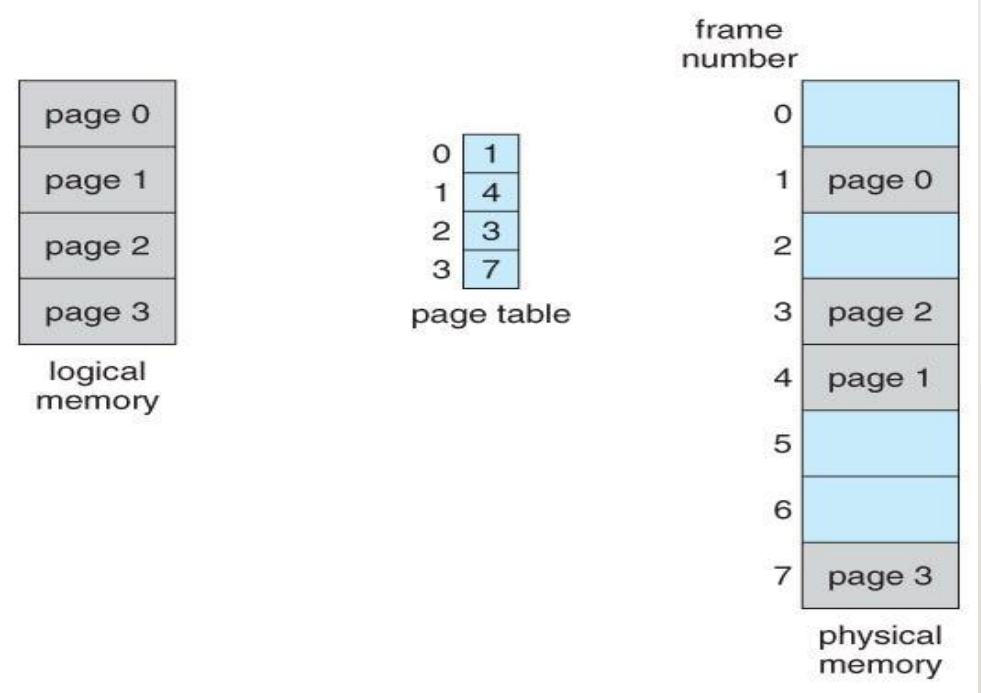
- In modern computer systems, Virtual memory as an alternate set of memory addresses. Programs use these virtual addresses rather than real addresses to store instructions and data. When the program is actually executed, the virtual addresses are converted into real memory addresses.
- Virtual memory might contain twice as many addresses as main memory. When a computer is executing many programs at the same time, Virtual memory make the computer to share memory efficiently.
- To facilitate copying virtual memory into real memory, the operating system divides virtual memory into pages, each of which contains a fixed number of addresses.
- Each page is stored on a disk until it is needed. When the page is needed, the operating system copies it from disk to main memory, translating the virtual addresses into real addresses.

Page Table

In modern computer systems, Virtual memory as an alternate set of memory addresses. Programs use these virtual addresses rather than real addresses to store instructions and data. When the program is actually executed, the virtual addresses are converted into real memory addresses.

Page Table: The data structure that is used by the virtual memory system in the operating system of a computer in order to store the mapping between physical and logical addresses is commonly known as **Page Table**.

Purpose of page table: Page table mainly provides the corresponding frame number (base address of the frame) where that page is stored in the main memory.



Page Table

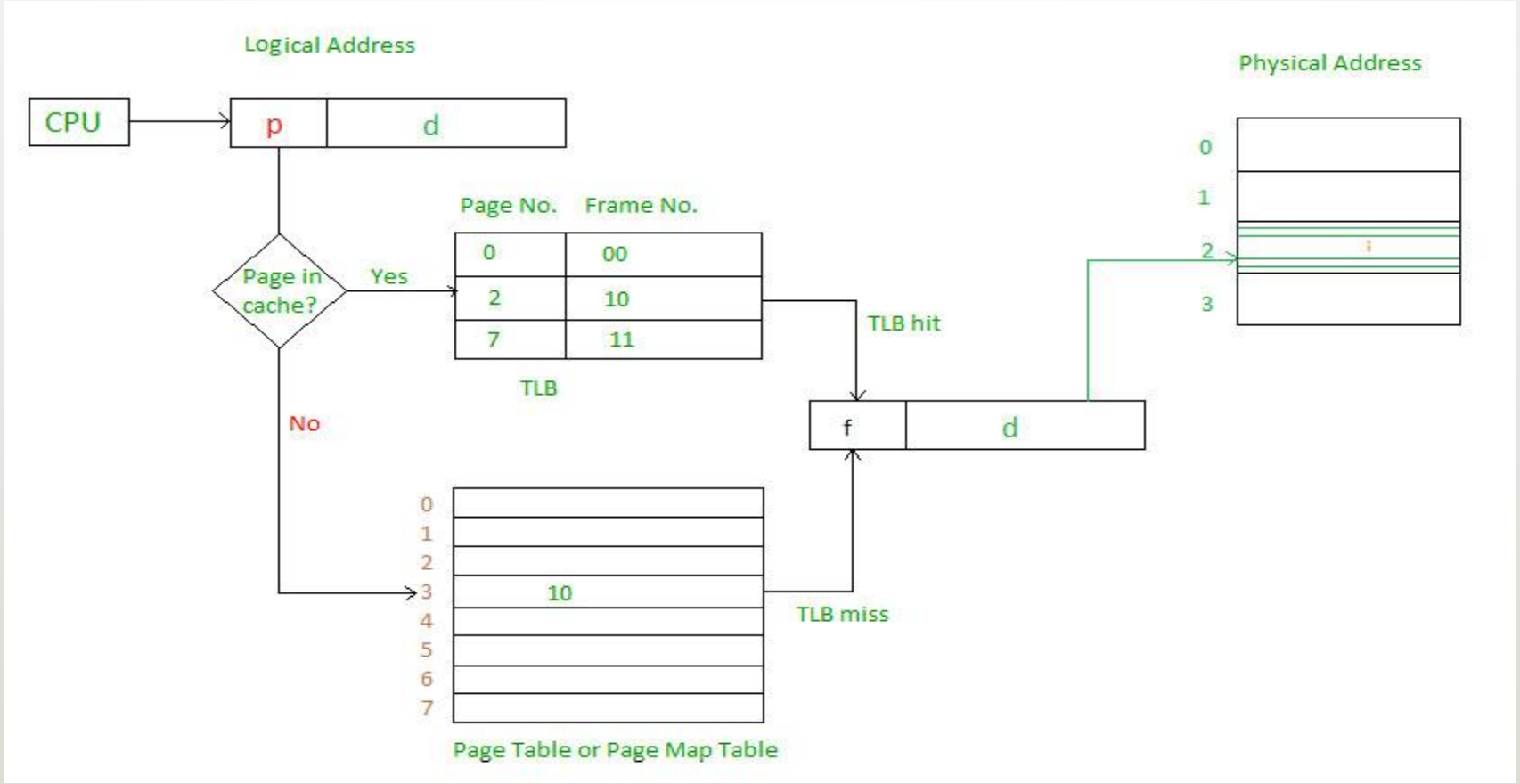
Organization: The page table typically consists of a set of page table entries (PTEs), with each entry containing information about a specific page of virtual memory, such as its corresponding physical address, access permissions, and other control bits.

Access: Accessing the page table can introduce overhead, as it requires memory accesses. To mitigate this, page tables are often cached in high-speed memory structures like the Translation Lookaside Buffer (TLB).

Translation Lookaside Buffer (TLB)

- Translation Lookaside Buffer (TLB) is a special cache used to keep track of recently used transactions. TLB contains page table entries that have been most recently used.
- Given a virtual address, the processor examines the TLB if a page table entry is present (TLB hit), the frame number is retrieved and the real address is formed. If a page table entry is not found in the TLB (TLB miss), the page number is used as an index while processing the page table.
- TLB first checks if the page is already in main memory, if not in main memory a page fault is issued then the TLB is updated to include the new page entry.

Translation Lookaside Buffer (TLB)



Steps in TLB

Steps in TLB hit

- CPU generates a virtual (logical) address., It is checked in TLB (present).
- The corresponding frame number is retrieved, which now tells where the main memory page lies.

Steps in TLB miss

- CPU generates a virtual (logical) address, It is checked in TLB (not present).
- Now the page number is matched to the page table residing in the main memory (assuming the page table contains all PTE).
- The corresponding frame number is retrieved, which now tells where the main memory page lies.
- The TLB is updated with new PTE (if space is not there, one of the replacement techniques comes into the picture i.e either FIFO, LRU or MFU etc).

SELF-ASSESSMENT QUESTIONS

1. What is the primary function of a page table in a virtual memory system?

A) To store the contents of the RAM.
B) To manage the mapping between virtual and physical memory addresses.
C) To manage the cache memory hierarchy.
D) To handle input/output operations.

2. Which of the following is a typical component of a page table entry (PTE)?

A) Cache tag
B) Virtual address
C) CPU instruction
D) Control register

SELF-ASSESSMENT QUESTIONS

3. What is the purpose of the Translation Lookaside Buffer (TLB) in a virtual memory system?

A) To store virtual memory addresses.
B) To manage page table entries.
C) To cache recently accessed virtual-to-physical address translations.
D) To manage input/output operations.

4. What happens when a virtual address translation is not found in the TLB?

A) The CPU accesses the page table to fetch the translation.
B) The CPU executes a cache miss.
C) The CPU directly accesses the physical memory.
D) The CPU halts the execution of the program.

TERMINAL QUESTIONS

Short answer questions:

1. Represent the use of virtual memory in computer system.

Long answer questions:

1. Describe the virtual memory system, focusing on the role of page tables.

REFERENCES FOR FURTHER LEARNING OF THE SESSION

Reference Books:

1. Computer Organization by Carl Hamacher, Zvonko Vranesic and Saftwat Zaky.
2. Computer System Architecture by M. Morris Mano
3. Computer Organization and Architecture by William Stallings

Sites and Web links:

1. https://www.geeksforgeeks.org/translation-lookaside-buffer-tlb-in-paging/

THANK YOU

(DEEMED TO BE UNIVERSITY)

Team – Digital Design & Computer Architecture