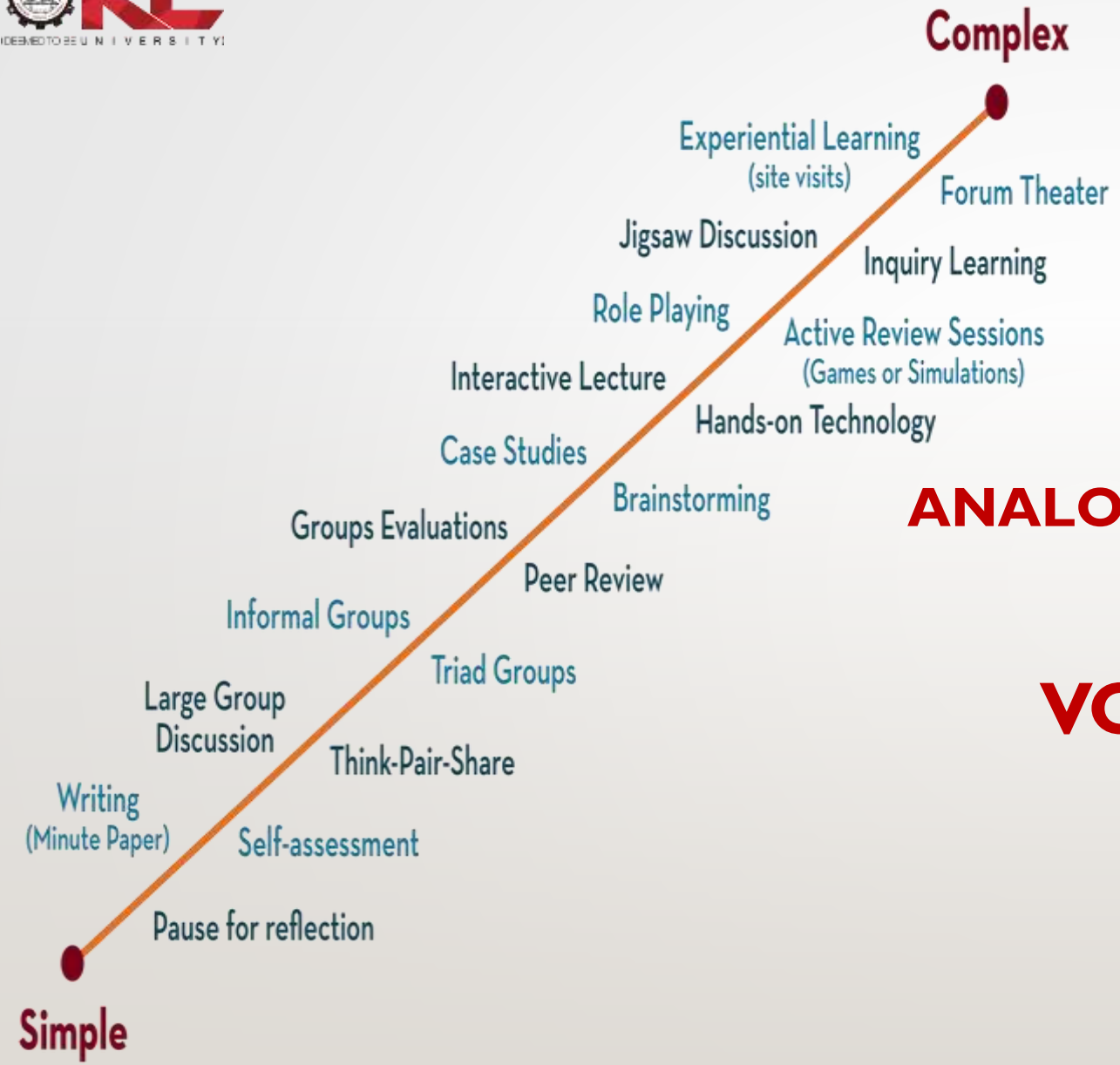


AY-2025-2026
ODD SEM

Department of ECE

ANALOG ELECTRONIC CIRCUIT DESIGN

24EC2104

Topic:

VOLTAGE DIVIDER BIAS

Session - 05

SESSION CONTENT

- Voltage Divider Bias Circuit
- Equivalent Circuit
- Analysis
- Design of Bias

AIM OF THE SESSION

To demonstrate Biasing of BJT using Voltage Divider Bias

INSTRUCTIONAL OBJECTIVES

This Session is designed to:

1. Demonstrate Voltage divider bias for BJT
2. Select bias components

LEARNING OUTCOMES

At the end of this session, you should be able to:

1. Describe voltage divider biasing circuit
2. Design component values for desired operating point

VOLTAGE DIVIDER BIAS

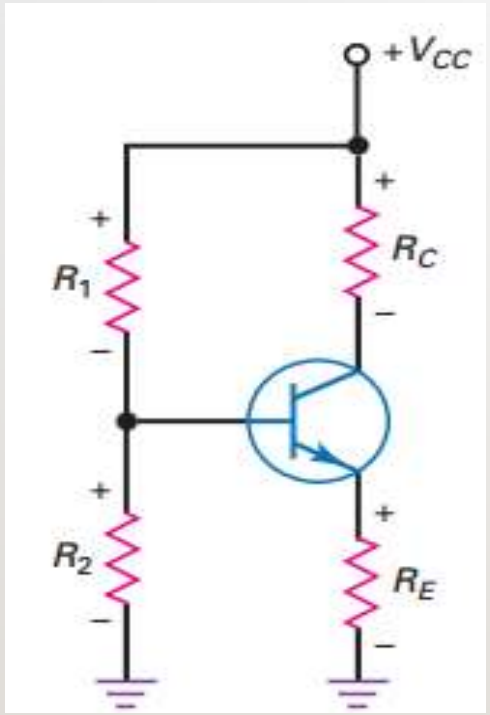


Fig. 5.1. Voltage divider bias for BJT

V_{CC}, R_1, R_2, and R_C control the saturation current and the cutoff voltage. A change in any of these quantities will change $I_{C(sat)}$ and/or $V_{CE(cutoff)}$.

Once the designer has established the values of the foregoing variables, the emitter resistance is varied to set the Q point at any position along the load line.

If R_E is too large, the Q point moves into the cutoff point. If R_E is too small, the Q point moves into saturation. Usually designers set the Q point at the middle of the load line.

When we examine transistor amplifiers, the dc load line Q point will be adjusted from the middle of the dc load line to achieve maximum output signal.

THEVENIN'S VOLTAGE AT INPUT TERMINALS

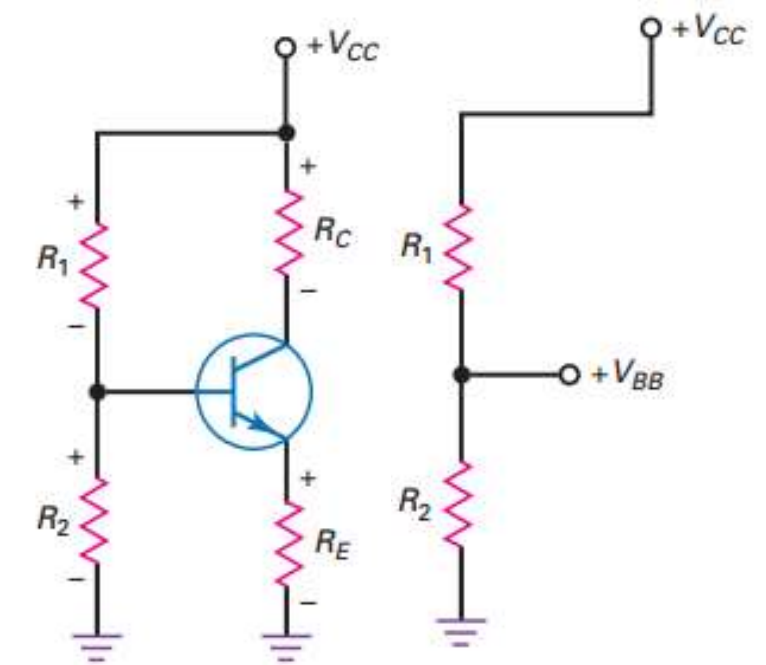


Fig. 5.2. Voltage divider bias for BJT – Equivalent Thevenin's voltage across base-ground terminals

Open the load terminals to obtain equivalent as shown in Fig. 5.2.

Now, Determine the open circuit voltage.

Applying series voltage division rule

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC}$$

THEVENIN'S RESISTANCE AT INPUT TERMINAL

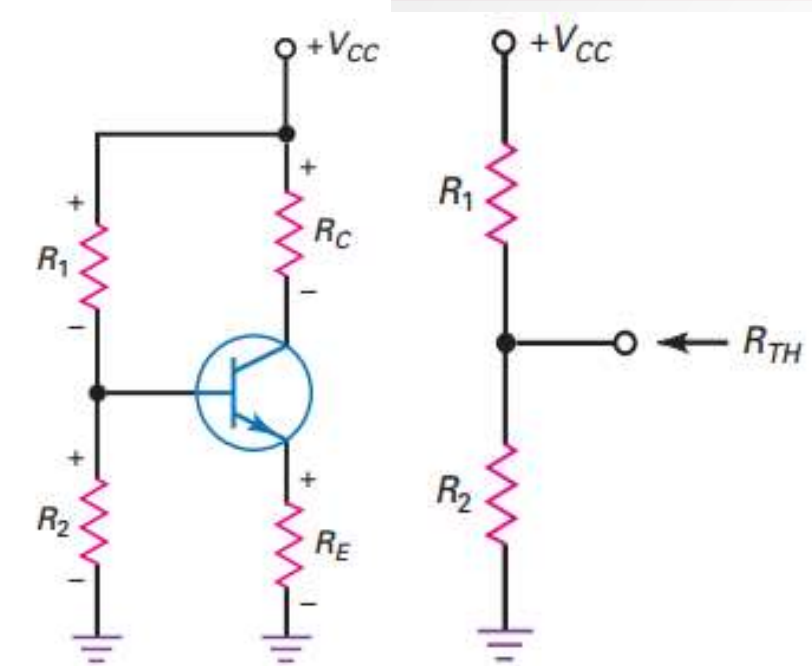


Fig. 5.3. Voltage divider bias for BJT – Equivalent Thevenin's Resistance across base-ground terminals

Consider the terminals as shown in Fig. 5.3.

Now, Determine the Resistance seen through the terminal.

While finding equivalent resistance the idel voltage sources are short circuited. Therefore

$R_{TH} = R_1 // R_2$

ANALYSIS

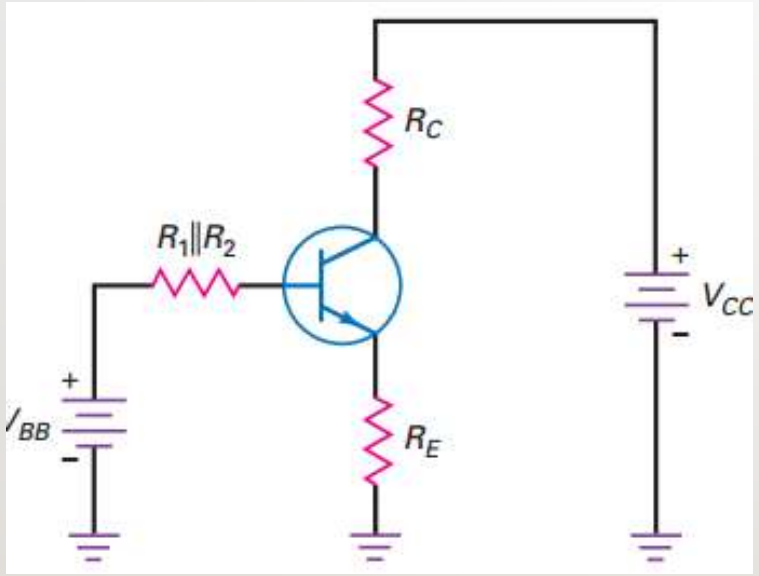


Fig. 5.4. Voltage divider bias for BJT – Equivalent circuit with Thevenin's equivalent in input loop

- Circuit Equations

Applying KVL in the input loop:

$V_{BB} = I_B R_{TH} + V_{BE} + I_E R_E$

Now, $I_B = I_E/\beta_{DC}$

Therefore,

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + (R_1 \| R_2)/\beta_{dc}}$$

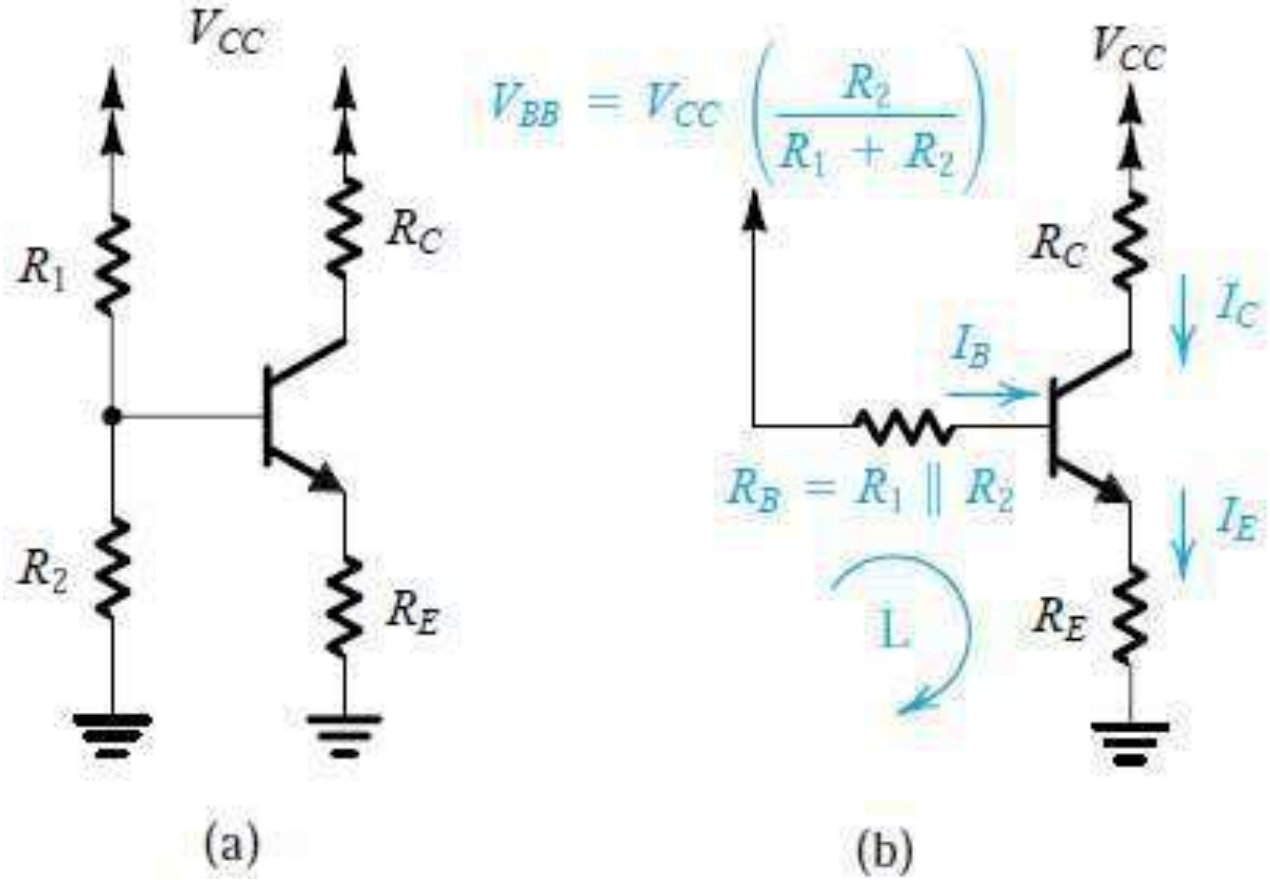
Applying KVL in the output loop:

$$I_C \approx I_E$$

$$V_C = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E$$

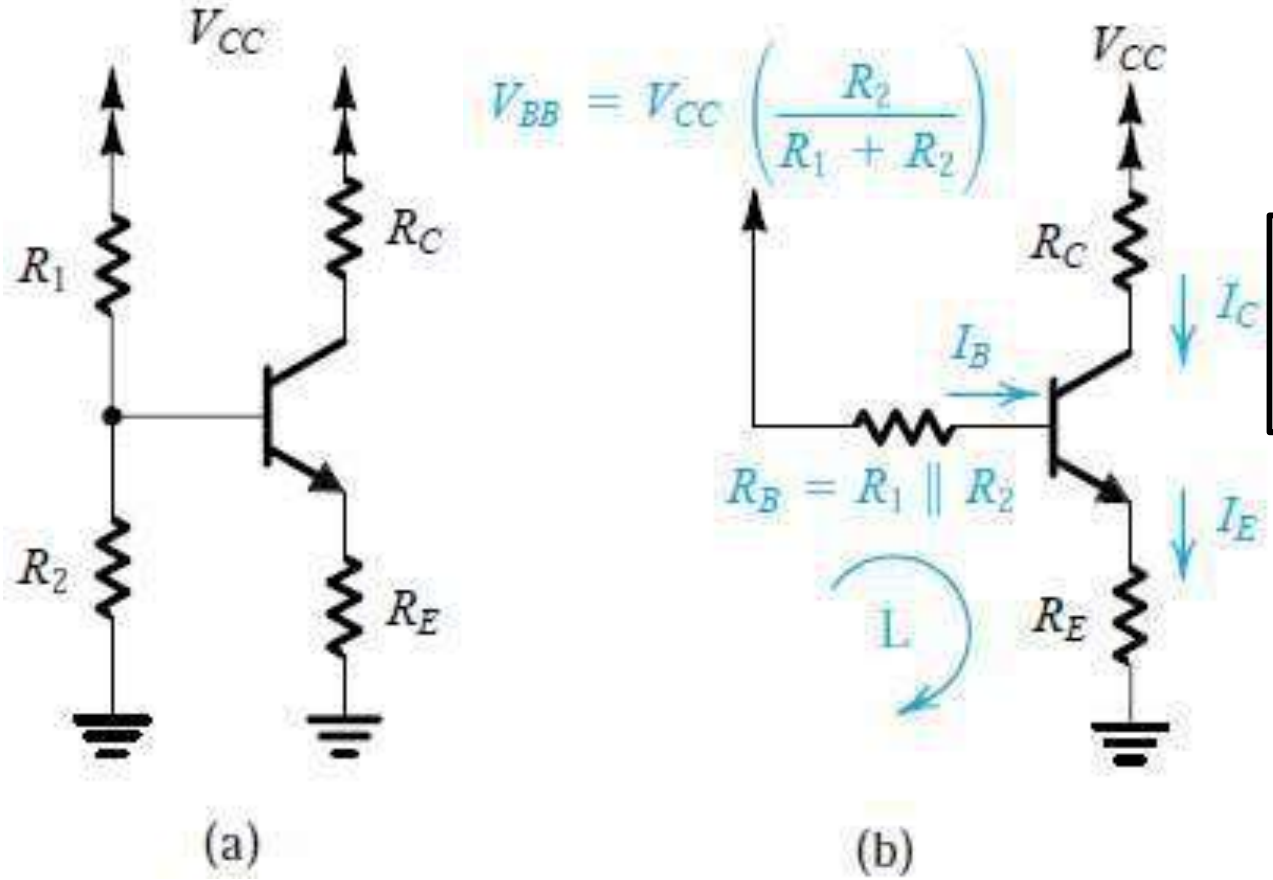
Self Bias/Voltage Divider Bias



Classical biasing for BJTs using a single power supply: **(a) circuit; (b) circuit with the** voltage divider supplying the base replaced with its Thévenin equivalent.

- The arrangement most commonly used for biasing a discrete-circuit transistor amplifier if only a **single power supply** is available.
- The technique consists of supplying the base of the transistor with a fraction of the supply voltage *VCC through the* ***voltage*** **divider *R1, R2.***
- *In addition,* ***a resistor RE*** *is connected to the emitter.*

Self Bias/Voltage Divider Bias

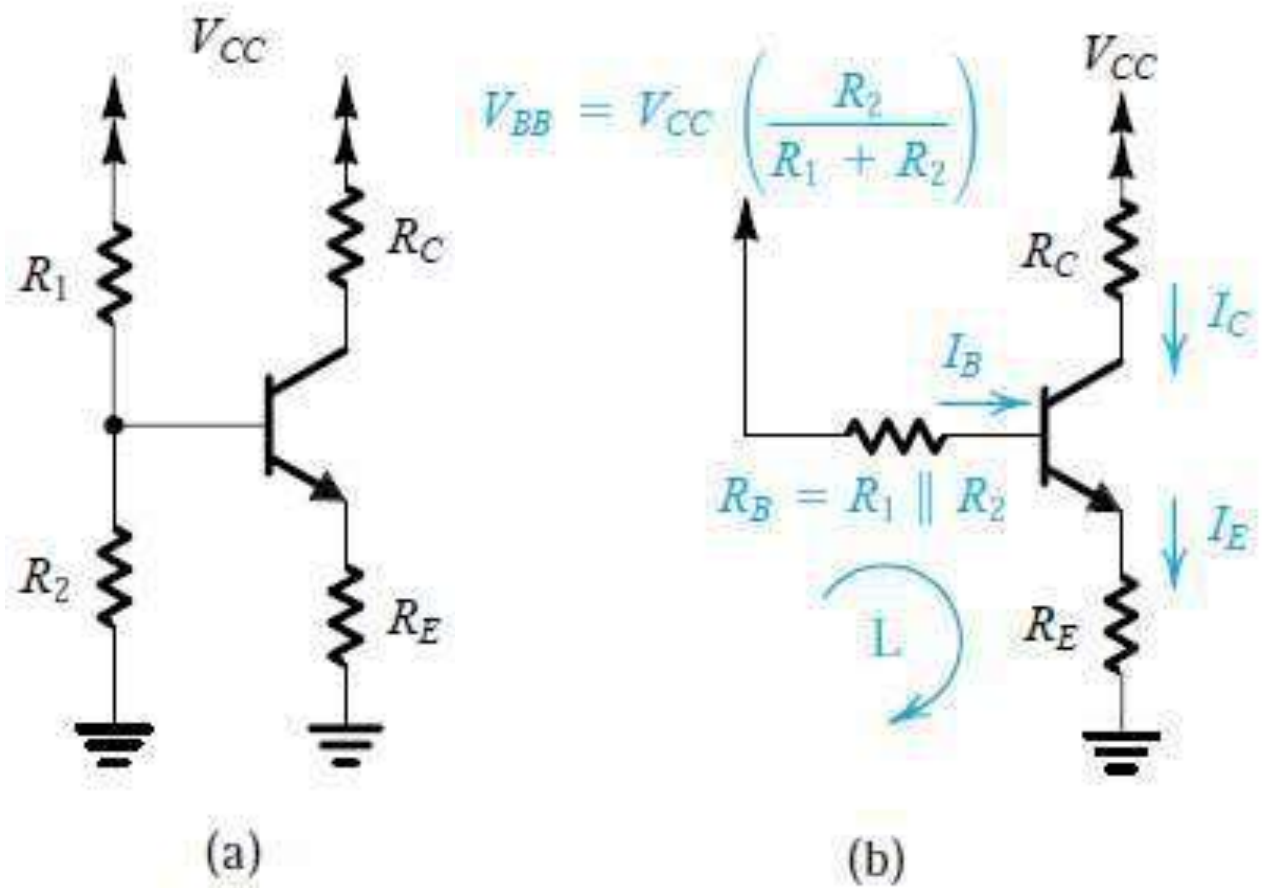


$$V_{BB} = V_{CC}\left(\frac{R_2}{R_1 + R_2}\right)$$

$$R_B = \left(\frac{R_1 R_2}{R_1 + R_2}\right)$$

Classical biasing for BJTs using a single power supply: **(a) circuit; (b) circuit with the** voltage divider supplying the base replaced with its Thévenin equivalent.

Self Bias/Voltage Divider Bias



Classical biasing for BJTs using a single power supply: **(a) circuit; (b) circuit with the** voltage divider supplying the base replaced with its Thévenin equivalent.

The current *IE can be determined by writing a Kirchhoff loop equation for the base–emitter–* ground loop, labeled L, and substituting

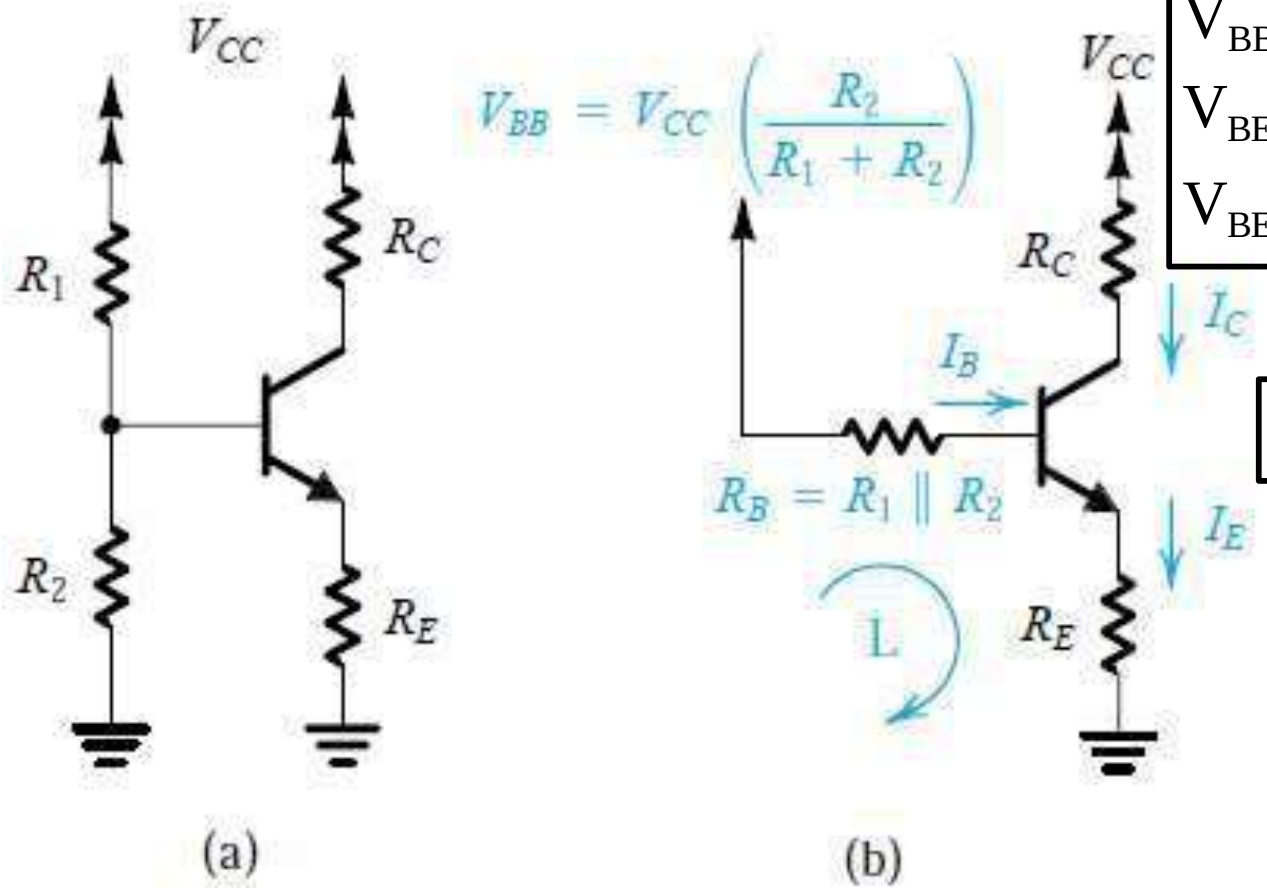
$$I_B = \frac{I_E}{\beta + 1}$$

$$V_{BB} = I_B R_B + V_{BE} + I_E R_E$$

$$V_{BB} = \left(\frac{I_E}{\beta + 1}\right) R_B + V_{BE} + I_E R_E$$

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + \frac{R_B}{\beta + 1}}$$

Self Bias/Voltage Divider Bias



$$V_{BB} = V_{BE} + I_B R_B + I_E R_E$$

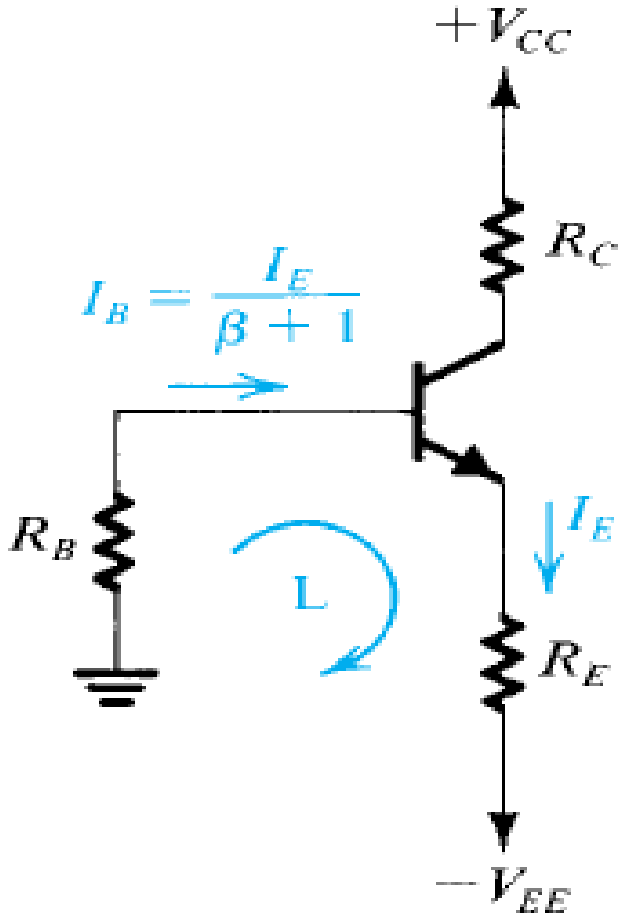
$$V_{BE} = V_{BB} - I_B R_B - (I_B + I_C) R_E$$

$$V_{BE} = V_{BB} - I_B (R_B + R_E) - I_C R_E$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

Classical biasing for BJTs using a single power supply: **(a) circuit; (b) circuit with the** voltage divider supplying the base replaced with its Thévenin equivalent.

Self Bias/Voltage Divider Bias



❖Biasing the BJT using two power supplies. Resistor *RB is* needed only if the signal is to be capacitively coupled to the base.

❖ Otherwise, the base can be connected directly to ground, or to a grounded signal source, resulting in almost total β -independence of the bias current.

$$I_E = \frac{V_{EE} - V_{BE}}{R_E + \frac{R_B}{\beta + 1}}$$

DESIGN OF VOLTAGE DIVIDER BIAS

The circuit is biased for VCE to be at a midpoint value with a specified collector current. Start by making the emitter voltage approximately one-tenth of the supply voltage:

$$V_E = 0.1\,V_{CC}$$

calculate the value of R_E to set up the specified collector current

$$R_E = V_E / I_E$$

Since the Q point needs to be at approximately the middle of the dc load line, about $0.5V_{CC}$ appears across the collector-emitter terminals. The remaining $0.4\,V_{CC}$ appears across the collector resistor; therefore:

$$R_C = 4\,R_E$$

Design for a stiff voltage divider using the 100 :1 rule:

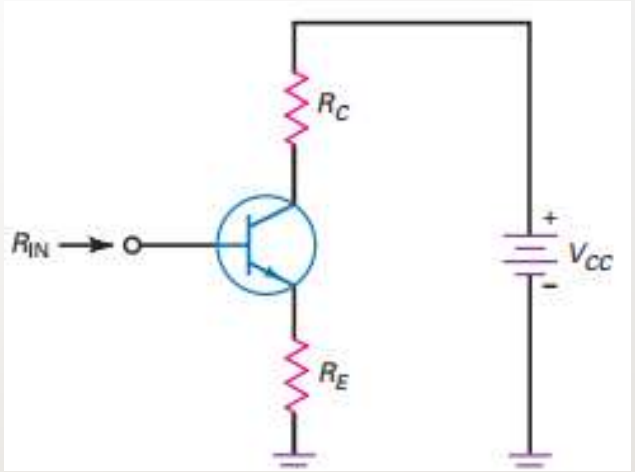


Fig. 5.5. Input Resistance seen by source terminals

$R_{TH} <= 0.01\ \beta_{dc}\ R_E$ Usually, R_2 is very small, therefore

$R_2 <= 0.01\ \beta_{dc}\ R_E$ and $R_1 = (V_1/V_2)R_2$

Example Problems

5.1 Calculate the Q-point for voltage divider bias as shown in Fig. 5.6 for R_E= 1 kΩ, and 2.2 kΩ, and 510 Ω Consider β_{DC} of BJT to be 100.

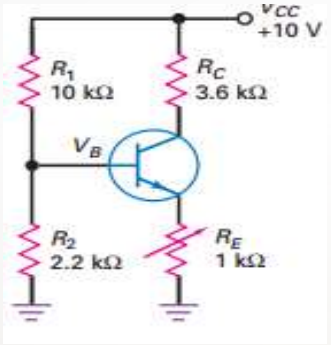


Fig. 5.6. Voltage Divider Bias

Solution:

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + (R_1 \| R_2)/\beta_{dc}}$$

Considering $I_E \sim I_C$ and

Now, I_E = 1.08 mA

And $V_E = I_E R_E$ = 1.08 mA * 1 kΩ = 1.08 V

$V_{CE} = V_{CC} - I_C R_C - V_E$ = 10-(1.08 mA * 3.6 kΩ)-1.08 =5.032 V

Similarly, for R_E= 2.2 kΩ, the Q-point is (7.12 V,0.495 mA). It is observed that Q-point is moved down on load line.
And for R_E= 2.2 kΩ, the Q-point is (1.45 V, 2.08 mA). It is observed that Q-point is moved up on load line.

Example Problems

5.2. Design voltage divider bias for circuit shown in Fig. 5.7 to meet the following specifications

$V_{CC} = 10V$	V_{CE} @ midpoint
$I_C = 10$ mA	2N3904's $\beta_{dc} = 100–300$

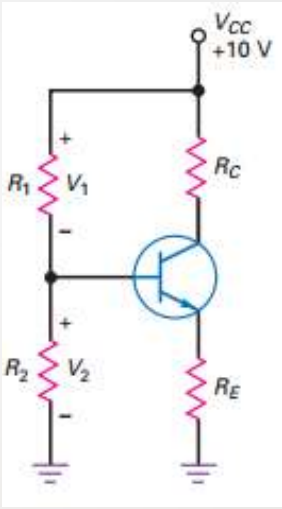


Fig. 5.7. Voltage divider for BJT

SOLUTION First, establish the emitter voltage by:

$$V_E = 0.1\ V_{CC}$$

$$V_E = (0.1)\ (10\ \text{V}) = 1\ \text{V}$$

The emitter resistor is found by:

$$R_E = \frac{V_E}{I_E}$$

$$R_E = \frac{1\ \text{V}}{10\ \text{mA}} = 100\ \Omega$$

The collector resistor is:

$$R_C = 4\ R_E$$

$$R_C = (4)\ (100\ \Omega) = 400\ \Omega\ (\text{use } 390\ \Omega)$$

Next, choose either a stiff or firm voltage divider. A stiff value of R_2 is found by:

$$R_2 \leq 0.01\ \beta_{dc}\ R_E$$

$$R_2 \leq (0.01)\ (100)\ (100\ \Omega) = 100\ \Omega$$

Now, the value of R_1 is:

$$R_1 = \frac{V_1}{V_2} R_2$$

$$V_2 = V_E + 0.7\ \text{V} = 1\ \text{V} + 0.7\ \text{V} = 1.7\ \text{V}$$

$$V_1 = V_{CC} - V_2 = 10\ \text{V} - 1.7\ \text{V} = 8.3\ \text{V}$$

$$R_1 = \left(\frac{8.3\ \text{V}}{1.7\ \text{V}}\right)(100\ \Omega) = 488\ \Omega\ (\text{use } 490\ \Omega)$$

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SELF-ASSESSMENT QUESTIONS

1. Which Bias is suitable for Amplifier?

(a) Emitter Bias
(b) Base Bias
(c) Collector feedback Bias
(d) Voltage divider bias

2. Which of the following bias is less effected by Beta variation?

(a) Voltage divider bias
(b) Collector feedback bias

SELF-ASSESSMENT QUESTIONS

3. Which of the following is usual design for operating point voltge?

(a) $0.8V_{CC}$
(b) $0.2V_{CC}$
(c) $0.5V_{CC}$
(d) $0.1V_{CC}$

4. Operating point of the BJT does not depend on Current Gain

(a) False
(b) True

ANSWERS

1. D
2. A
3. C
4. A

TERMINAL QUESTIONS

1. Describe the operation of Voltage Divider bias. Sketch circuit and obtain operating point.
2. Describe the equivalent input loop circuit for voltage divider bias.
3. Obtain the input and output circuit equations for voltage divider bias.
4. Identify the circuit requirements to design voltage divider bias.
5. Develop the design steps to bias BJT in to middle point of load line using voltage divider bias.

REFERENCES FOR FURTHER LEARNING OF THE SESSION

Reference Books:

1. Albert Malvino, David Bate, "Electronic Principles"
2. Robert L. Boylestad and Louis Nashelsky - "Electronic Devices and Circuit Theory"

THANK YOU

(DEEMED TO BE UNIVERSITY)

Team – ANALOG ELECTRONIC CIRCUIT DESIGN

Prepared by – Mr. S. Ravi Teja