K L Deemed to be University
Department of Electronics and Communication Engineering -- KLVZA
Course Handout
2024-2025, Even Sem

Course Title	:DIGITAL DESIGN AND COMPUTER ARCHITECTURE
Course Code	:23EC1202
L-T-P-S Structure	: 3-0-2-0
Pre-requisite	:
Credits	: 4
Course Coordinator	:APPIKATLA PHANI KUMAR
Team of Instructors	:
Teaching Associates	:

Syllabus :CO 1: Combinational Digital Logic Circuits: Boolean Algebra, Digital Logic SOP/POS representation and optimization techniques. Adders, Subtractors, Multiplexers, De-Multiplexers, Decoder, Encoder, Concept of Reversible Gates. Programmable Logic Devices: PROM, PAL, and PLA design. Implementation of CPLD (Macrocells) and FPGA (CLB/LUT) based digital logic modules and their applications. CO-2: Design of Sequential and Memory Circuits: Latches and Flip-Flops, Modeling of memory ,registers and Shift registers, Timing and sequence control modules using Asynchronous/Synchronous counters, Ring and Johnson counter as timing and control units. Random Access Memory (RAM) and Memory decoding. CO-3: Basic Computer Architecture and Instructions: Features of Micro Computer, Operands, Addressing modes, Instruction formats, Machine cycle, Instruction sets, subroutine call and return mechanisms. Instruction set architectures - CISC and RISC architectures. Hardwired realization vs micro-programmed realization, multi-cycle implementation, Instruction level parallelism, instruction pipelining and pipeline hazards. CO-4: Memory Architecture and I/O Organization Storage systems, introduction to memory hierarchy: importance of temporal and spatial locality; main memory organization, cache memory: address mapping, block size, replacement, and store policies. Virtual Memory System: page table and TLB. External storage; IO fundamentals: handshaking, buffering, programmed IO, interrupt driven IO.

Text Books :1. Computer System Architecture by M. Moris Mano, 3rd edition published by Pearson/PHI 2. Fundamentals of Digital Logic with Verilog HDL by Stephen Brown and ZvonkoVranesic, 3rd edition, Published by Mc Graw Hill

Reference Books :1. Computer Organization and Design by DA Patterson and JL Hennessy,4th edition published by Morgan Kaufmann Publisher 2. Computer Organization and Architecture, by W. Stalling published by PHI.

Web Links :[1]. https://nptel.ac.in/courses/117106086 [2]. https://archive.nptel.ac.in/courses/106/105/106105163/

MOOCS :[1]. https://www.edx.org/learn/design/harvey-mudd-college-digital-design [2]. https://ocw.mit.edu/courses/6-823-computer-system-architecture-fall-2005/ [3]. https://www.coursera.org/learn/digital-systems

COURSE OUTCOMES (COs):

CO NO	Course Outcome (CO)	PO/PSO	Blooms Taxonomy Level (BTL)
CO1	Build the combinational and programmable digital logic circuits using logic gates and optimization methods	PSO1,PO1,PO2	3
CO2	Construct the sequential and memory circuits using flip-flops	PSO1,PO1,PO2	3
CO3	Able to organize computer architecture and instructions sequence	PSO1,PO1,PO2	3
CO4	Model the Memory Architecture and I/O Organization modules	PSO1,PO1,PO2	3
CO5	Develop and analyze of computer architecture modules using basic combinational, sequential and memory logics	PSO1,PO1,PO3,PO5	4

COURSE OUTCOME INDICATORS (COIs)::

Outcome No.	Highest BTL	COI-1	COI-2
CO1	3	**Btl-2** This course provides a comprehensive introduction to digital logic design and Boolean algebra, covering fundamental concepts, representation techniques, and optimization strategies. Students will gain a deep understanding of the building blocks of digital systems and learn how to design and optimize circuits for various applications.	**Btl-3** Understanding this course delves into the realm of Programmable Read-Only Memory (PROM), Programmable Array Logic (PAL), and Programmable Logic Array (PLA), exploring their design principles and applications. Students will gain a comprehensive understanding of these devices and their role in modern digital systems.

CO2	3	**Btl-2** This course empowers the knowledge by Studying latches, flip-flops, memory modeling, and register design provides essential knowledge for creating digital circuits with effective data storage. Exploring timing controls using asynchronous/synchronous counters ensures accurate sequencing, while understanding shift registers enables serial data manipulation.	**Btl-3** The study of Ring and Johnson counters provides insights into advanced sequential control mechanisms, improving students' understanding of precise timing in digital systems. Exploring Random Access Memory (RAM) and Memory decoding enhances their knowledge of efficient data storage and retrieval, contributing to the optimization of digital circuits.
CO3	3	**Btl-2** Understanding an in-depth exploration of microcomputer architecture and programming, covering essential features, addressing modes, instruction formats, machine cycles, and subroutine call and return mechanisms. Students will gain a comprehensive understanding of the fundamental components that constitute a microcomputer system and the intricacies of programming at the machine level.	**Btl-3** This course explores Instruction Set Architectures (ISAs), covering Complex Instruction Set Computing (CISC) and Reduced Instruction Set Computing (RISC). Topics include hardwired versus micro-programmed realization, multi-cycle implementations, and advanced concepts like instruction-level parallelism, instruction pipelining, and pipeline hazard mitigation.
CO4	3	**Btl-2** Understanding the storage systems and memory hierarchy, students delve into the hierarchical organization of computer memory. Emphasizing the significance of temporal and spatial locality, this provides students with a thorough understanding of the principles governing efficient data retrieval in computer architecture.	**Btl-3** The study of virtual memory system, emphasizing page tables and TLBs for streamlined virtual-to-physical memory mapping. The course further covers external storage and IO fundamentals, including handshaking, buffering, programmed IO, and interrupt-driven IO. This provides a comprehensive grasp of organizational elements in virtual memory systems and principles governing Input/Output operations in computer architecture.
CO5	4	**Btl-4** Students analyze practical applications in digital electronics, including tasks like LED control, car security system design, and participant selection using multiplexers. They also analyze projects involving digital displays, random number generators, and computational processing systems. These hands-on activities offer a valuable opportunity for students to analyze and understand the diverse applications of digital electronics in real-world scenarios.	

PROGRAM OUTCOMES & PROGRAM SPECIFIC OUTCOMES (POs/PSOs)

Po No.	Program Outcome
PO1	Engineering Knowledge:Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO2	Problem Analysis: Identify, formulate, review research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences and engineering sciences
PO3	Design/Development of Solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations
PO4	Conduct Investigations of Complex Problems:Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions for complex problems that cannot be solved by straightforward application of knowledge, theories and techniques applicable to the engineering discipline.
PO5	Modern Tool Usage:Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
PO6	The Engineer and Society:Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO7	Environment and Sustainability:Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development
PO8	Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice
PO9	Individual and Team Work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10	Communication:Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions

PO11	Project Management and Finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	Life-long Learning: Recognize the need for, and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change.
PSO1	An ability to solve Electronics engineering problems, using latest hardware and software tools, to obtain appropriate solutions in the domain of embedded systems and Internet of things.
PSO2	Ability to design web applications by applying the knowledge of cyber security.

Lecture Course DELIVERY Plan:

Sess.No.	CO	COI	Topic	Book No[CH No] [Page No]	Teaching-Learning Methods	EvaluationComponents
1	CO1	COI-1	Course Handout	NA	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM1,SEM-EXAM2
2	CO1	COI-1	Introduction, Boolean Algebra	T BOOK [1], CH 2, Page no 1-24	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM1
3	CO1	COI-1	Digital Logic SOP/POS representation and optimization techniques	T BOOK [1], CH 2, Page no 25-37	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM1
4	CO1	COI-1	Adders, Subtractors	T BOOK [1], CH 2, Page no 38-42	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM1
5	CO1	COI-1	Multiplexers, De-Multiplexers	T BOOK [1], CH 6, Page no 303-314	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM1
6	CO1	COI-1	Decoder, Encoder	T BOOK [1], CH 2, Page no 314-317	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM1
7	CO1	COI-2	Introduction to PLD's, PROM	T BOOK [1], CH 2, Page no 87-92	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM1
8	CO1	COI-2	PAL and PLA design	T BOOK [1], CH 2, Page no 47-49	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM1
9	CO1	COI-2	Implementation of CPLD (Macrocells) based digital logic modules and their applications	T BOOK [1], CH 2, Page no 92-101	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM1
10	CO1	COI-2	FPGA (CLB/LUT) based digital logic modules and their applications	T BOOK [1], CH 2, Page no 102-108	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM1
11	CO1	COI-2	Concept of Reversible Gates	T BOOK [1], CH 2, Page no 62-63	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM1
12	CO2	COI-1	Introduction to sequential circuits, Latches	T BOOK [1], CH 2, Page no 497-499	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM1
13	CO2	COI-1	Flip-Flops	T BOOK [1], CH 2, Page no 499-502	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM1
14	CO2	COI-1	Modeling of memory and registers	T BOOK [1], CH 2, Page no 68-71	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM1
15	CO2	COI-1	Shift Registers	T BOOK [1], CH 5, Page no 160 - 165	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM1

Sess.No.	CO	COI	Topic	Book No[CH No] [Page No]	Teaching-Learning Methods	EvaluationComponents
16	CO2	COI-2	Timing and sequence control modules using Asynchronous counters	T BOOK [1], CH 5, Page no 155	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM1
17	CO2	COI-2	Timing and sequence control modules using Synchronous counters	T BOOK [1], CH 5, Page no 156	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM1
18	CO2	COI-2	Ring counter as timing and control units	T BOOK [1], CH 5, Page no 157-158	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM1
19	CO2	COI-2	Johnson counter as timing and control units	T BOOK [1], CH 5, Page no 159-161	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM1
20	CO2	COI-2	Random Access Memory (RAM)	T BOOK [1], CH 5, Page no 609 - 610	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM1
21	CO2	COI-2	Memory decoding	T BOOK [1], CH 5, Page no 611	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM1
22	CO3	COI-1	Introduction, Features of Micro Computer	T BOOK [1], CH 5, Page no 123 - 126	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM2
23	CO3	COI-1	Operands, Addressing modes, Instruction formats	T BOOK [1], CH 5, Page no 186 - 190	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM2
24	CO3	COI-1	Machine cycle, Instruction sets	T BOOK [1], CH 7, Page no 174-179	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM2
25	CO3	COI-1	subroutine call and return mechanisms	T BOOK [1], CH 7, Page no 213-220	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM2
26	CO3	COI-2	Instruction set architectures - CISC and RISC architectures	T BOOK [1], CH 7, Page no 262	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM2
27	CO3	COI-2	Hardwired realization vs micro-programmed realization	T BOOK [1], CH 7, Page no 282-285	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM2
28	CO3	COI-2	Multi-cycle implementation	T BOOK [1], CH 7, Page no 286-288	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM2
29	CO3	COI-2	Instruction level parallelism	T BOOK [1], CH 9, Page no 310-315	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM2
30	CO3	COI-2	Instruction pipelining and pipeline Hazards	T BOOK [1], CH 9, Page no 316-320	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM2
31	CO4	COI-1	Introduction, Storage systems	T BOOK [1], CH 12, Page no 445	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM2
32	CO4	COI-1	Introduction to memory hierarchy: Importance of temporal and spatial locality	T BOOK [1], CH 12, Page no 446-448	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM2

Sess.No.	CO	COI	Topic	Book No[CH No] [Page No]	Teaching-Learning Methods	EvaluationComponents
33	CO4	COI-1	Main memory organization	T BOOK [2], CH 12, Page no 448-452	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM2
34	CO4	COI-1	Cache memory: address mapping, Block size	T BOOK [2], CH 12, Page no 462-465	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM2
35	CO4	COI-1	Replacement, and Store policies	T BOOK [2], CH 12, Page no 466-469	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM2
36	CO4	COI-2	Virtual memory system: page table and TLB	T BOOK [2], CH 12, Page no 469-476	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM2
37	CO4	COI-2	External storage	T BOOK [2], CH 12, Page no 478	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM2
38	CO4	COI-2	IO fundamentals: handshaking, buffering	T BOOK [2], CH 11, Page no 392-396	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM2
39	CO4	COI-2	Programmed IO, Interrupt driven IO	T BOOK [2], CH 11, Page no 402-407	Chalk,PPT,Talk	End Semester Exam,SEM-EXAM2

Lecture Session wise Teaching – Learning Plan

SESSION NUMBER : 1

Session Outcome: 1 Course introduction session

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	1	Talk	--- NOT APPLICABLE ---
20	Discussion on course objectives, course outcomes, and course outcome indicators	1	PPT	--- NOT APPLICABLE ---
20	Discussion on evaluation plan	1	PPT	--- NOT APPLICABLE ---
5	Summary & Conclusion	1	PPT	--- NOT APPLICABLE ---

SESSION NUMBER : 2

Session Outcome: 1 Students gain fundamental knowledge in computer science, digital logic, mathematical principles essential for understanding the inner workings of computer

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	1	Talk	One minute paper
20	Introduction	1	PPT	One minute paper
20	Boolean Algebra	1	PPT	One minute paper
5	Summary & Conclusion	1	PPT	One minute paper

SESSION NUMBER : 3

Session Outcome: 1 Students get knowledge and skills in representing Boolean expressions optimizing digital circuits for efficiency

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	1	Talk	One minute paper
20	Digital logic SOP/POS representation	1	PPT	One minute paper
20	Optimization techniques	1	PPT	One minute paper
5	Summary & Conclusion	1	PPT	One minute paper

SESSION NUMBER : 4

Session Outcome: 1 Students explores the building blocks like adders, subtractors and grasp the applications of these circuits.

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	1	Talk	--- NOT APPLICABLE ---
20	Half adder, Full adder	1	PPT	One minute paper
20	Half subtractor, Full subtractor	1	PPT	One minute paper
5	Summary & Conclusion	1	PPT	One minute paper

SESSION NUMBER : 5

Session Outcome: 1 Students gains the knowledge of versatile components used in digital systems for routing, signal selection, and circuit expansion.

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	1	Talk	--- NOT APPLICABLE ---
20	Multiplexer	1	PPT	One minute paper
20	De-Multiplexer	1	PPT	One minute paper
5	Summary & Conclusion	1	PPT	One minute paper

SESSION NUMBER : 6

Session Outcome: 1 Students understand the essential components used in encoding and decoding the information in various digital systems

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	1	Talk	--- NOT APPLICABLE ---
20	Decoder	1	PPT	One minute paper
20	Encoder	1	PPT	One minute paper
5	Summary & Conclusion	1	PPT	One minute paper

SESSION NUMBER : 7

Session Outcome: 1 Students gets the fundamental understanding of programmable logic devices

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	2	Talk	--- NOT APPLICABLE ---
20	Introduction to PLD's	2	PPT	Sketching & Drawing
20	PROM	2	PPT	Sketching & Drawing
5	Summary & Conclusion	2	PPT	Sketching & Drawing

SESSION NUMBER : 8

Session Outcome: 1 Students gain the deep understanding of two types of PLD's

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	2	Talk	--- NOT APPLICABLE ---
20	Programmable Array Logic (PAL)	2	PPT	Sketching & Drawing
20	Programmable Logic Array (PLA)	2	PPT	Sketching & Drawing
5	Summary & Conclusion	2	PPT	Sketching & Drawing

SESSION NUMBER : 9

Session Outcome: 1 Students experience the designing of digital circuits using CPLD and macrocells

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	2	Talk	--- NOT APPLICABLE ---
20	CPLD structure	2	PPT	Sketching & Drawing
20	Implementation of CPLD (macrocells)	2	PPT	Sketching & Drawing
5	Summary & Conclusion	2	PPT	Sketching & Drawing

SESSION NUMBER : 10

Session Outcome: 10 Students acquires the skills for designing digital circuits using FPGA

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	2	Talk	--- NOT APPLICABLE ---
20	FPGA Stucture	2	PPT	Sketching & Drawing
20	Implementation of FPGA	2	PPT	Sketching & Drawing
5	Summary & Conclusion	2	PPT	Sketching & Drawing

SESSION NUMBER : 11

Session Outcome: 1 Students gets the knowledge on the concept of reversible gates

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	2	Talk	--- NOT APPLICABLE ---
20	Types of reversible gates	2	PPT	Sketching & Drawing
20	Operation of reversible gates	2	PPT	Sketching & Drawing
5	Summary & Conclusion	2	PPT	Sketching & Drawing

SESSION NUMBER : 12

Session Outcome: 1 Students gain the fundamental knowledge on sequential circuits, latches

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	1	Talk	Problem-Based Learning
20	Sequential circuits-Introduction	1	PPT	Problem-Based Learning
20	Concept of latches	1	PPT	Problem-Based Learning
5	Summary & Conclusion	1	PPT	Problem-Based Learning

SESSION NUMBER : 13

Session Outcome: 1 Students gain the conceptual understanding of types of flip flops

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	1	Talk	--- NOT APPLICABLE ---
20	Concept of Flip-Flops	1	PPT	Problem-Based Learning
20	Types of Flip-Flops	1	PPT	Problem-Based Learning
5	Summary & Conclusion	1	PPT	Problem-Based Learning

SESSION NUMBER : 14

Session Outcome: 1 Students gain the knowledge on memory and registers

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	1	Talk	--- NOT APPLICABLE ---
20	Modelling of memory	1	PPT	Problem-Based Learning
20	Registers	1	PPT	Problem-Based Learning
5	Summary & Conclusion	1	PPT	Problem-Based Learning

SESSION NUMBER : 15

Session Outcome: 1 Students gain the practical skills applicable to shift registers

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	1	Talk	--- NOT APPLICABLE ---
20	Types of shift registers	1	PPT	Problem-Based Learning
20	Operation of Shift registers	1	PPT	Problem-Based Learning
5	Summary & Conclusion	1	PPT	Problem-Based Learning

SESSION NUMBER : 16

Session Outcome: 1 Students able to understand the Timing and sequence control modules using Asynchronous counters

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	2	Talk	--- NOT APPLICABLE ---
20	Asynchronous counters	2	PPT	Design Thinking
20	Asynchronous counters- Timing and sequence control modules	2	PPT	Design Thinking
5	Summary & Conclusion	2	PPT	Design Thinking

SESSION NUMBER : 17

Session Outcome: 1 Students gain the knowledge on Timing and sequence control modules using Synchronous counters

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	2	Talk	--- NOT APPLICABLE ---
20	Synchronous counters	2	PPT	Design Thinking
20	Synchronous counters- Timing and sequence control modules	2	PPT	Design Thinking
5	Summary & Conclusion	2	PPT	Design Thinking

SESSION NUMBER : 18

Session Outcome: 1 Students gets the knowledge of Ring counter as timing and control units

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	2	Talk	--- NOT APPLICABLE ---
20	Ring counter	2	PPT	Design Thinking
20	Operation of ring counter	2	PPT	Design Thinking
5	Summary & Conclusion	2	PPT	Design Thinking

SESSION NUMBER : 19

Session Outcome: 1 Students gets the knowledge on Johnson counter as timing and control units

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	2	Talk	--- NOT APPLICABLE ---
20	Johnson counter	2	PPT	Design Thinking
20	Operation of Johnson counter	2	PPT	Design Thinking
5	Summary & Conclusion	2	PPT	Design Thinking

SESSION NUMBER : 20

Session Outcome: 1 Students acquires the knowledge of Random Access Memory

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	2	Talk	--- NOT APPLICABLE ---
40	Random Access Memory (RAM) and its application in computer architecture	2	PPT	Design Thinking
5	Summary & Conclusion	2	PPT	Design Thinking

SESSION NUMBER : 21

Session Outcome: 1 Students master memory decoding and skill in digital systems

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	2	Talk	--- NOT APPLICABLE ---
40	Memory decoding	2	PPT	Design Thinking
5	summary and conclusion	2	PPT	Design Thinking

SESSION NUMBER : 22

Session Outcome: 1 Students gets the comprehensive understanding of micro computer

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	1	Talk	--- NOT APPLICABLE ---
20	Introduction to computer architecture	1	PPT	One minute paper
20	Features of micro computer	1	PPT	One minute paper
5	Summary & Conclusion	1	PPT	One minute paper

SESSION NUMBER : 23

Session Outcome: 1 Students can understand how the instruction executed in the computer

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	1	Talk	--- NOT APPLICABLE ---
20	Operand, addressing modes	1	PPT	One minute paper
20	Instruction formats	1	PPT	One minute paper
5	Summary & Conclusion	1	PPT	One minute paper

SESSION NUMBER : 24

Session Outcome: 1 Students will develop the strong foundation on instruction sets

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	1	Talk	--- NOT APPLICABLE ---
20	Instruction sets	1	PPT	One minute paper
20	Machine cycle	1	PPT	One minute paper
20	Summary & Conclusion	1	PPT	One minute paper

SESSION NUMBER : 25

Session Outcome: 1 Students gets the deep understanding of subroutine call and return mechanisms

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	1	Talk	--- NOT APPLICABLE ---
20	Types of subroutines	1	PPT	One minute paper
20	subroutine call and return mechanisms	1	PPT	One minute paper
5	Summary & Conclusion	1	PPT	One minute paper

SESSION NUMBER : 26

Session Outcome: 1 Students gain the insights into design principles of modern computers

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	2	Talk	--- NOT APPLICABLE ---
20	CISC architecture	2	PPT	One minute paper
20	RISC architecture	2	PPT	One minute paper
5	Summary & Conclusion	2	PPT	One minute paper

SESSION NUMBER : 27

Session Outcome: 1 Students comprehend the trade off between Hardwired realization vs micro-programmed realization

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	2	Talk	--- NOT APPLICABLE ---
20	Hardwired realization	2	PPT	One minute paper
20	micro-programmed realization	2	PPT	One minute paper
5	Summary & Conclusion	2	PPT	One minute paper

SESSION NUMBER : 28

Session Outcome: 1 Students grasp the concept of Multi-cycle implementation

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	2	Talk	--- NOT APPLICABLE ---
40	Multi-cycle implementation	2	PPT	One minute paper
5	Summary & Conclusion	2	PPT	One minute paper

SESSION NUMBER : 29

Session Outcome: 1 Students gets the knowledge of instruction level pipelining and instruction level parallelism

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	2	Talk	--- NOT APPLICABLE ---
20	Instruction level pipelining	2	PPT	One minute paper
20	Instruction level parallelism	2	PPT	One minute paper
5	Summary & Conclusion	2	PPT	One minute paper

SESSION NUMBER : 30

Session Outcome: 1 students understand the Instruction pipelining and pipeline Hazards

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	2	Talk	--- NOT APPLICABLE ---
20	Instruction pipelining	2	PPT	One minute paper
20	pipeline Hazards	2	PPT	One minute paper
5	Summary & Conclusion	2	PPT	One minute paper

SESSION NUMBER : 31

Session Outcome: 1 Students understand the role of storage in micro computers

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	1	Talk	--- NOT APPLICABLE ---
40	Introduction to Storage systems	1	PPT	Group Discussion
5	Summary & Conclusion	1	PPT	Group Discussion

SESSION NUMBER : 32

Session Outcome: 1 Students gets the knowledge on Introduction to memory hierarchy: Importance of temporal and spatial locality

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	1	Talk	--- NOT APPLICABLE ---
20	Introduction to memory hierarchy	1	PPT	Group Discussion
20	Importance of temporal and spatial locality	1	PPT	Group Discussion
5	Summary & Conclusion	1	PPT	Group Discussion

SESSION NUMBER : 33

Session Outcome: 1 Students gain the deeper insight into memory organization

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	1	Talk	--- NOT APPLICABLE ---
40	Main memory organization	1	PPT	Group Discussion
5	Summary & Conclusion	1	PPT	Group Discussion

SESSION NUMBER : 34

Session Outcome: 1 students gain the deeper insight into the concept of cache memory

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	1	Talk	--- NOT APPLICABLE ---
20	Cache memory: address mapping	1	PPT	Group Discussion
20	Block size	1	PPT	Group Discussion
5	Summary & Conclusion	1	PPT	Group Discussion

SESSION NUMBER : 35

Session Outcome: 1 Students gain the knowledge on cache mapping techniques

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	1	Talk	--- NOT APPLICABLE ---
20	Concept of Replacement	1	PPT	Group Discussion
20	Concept of Store policies	1	PPT	Group Discussion
5	Summary & Conclusion	1	PPT	Group Discussion

SESSION NUMBER : 36

Session Outcome: 1 Students grasp the step by step process of converting virtual address to physical address

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	1	Talk	--- NOT APPLICABLE ---
20	Virtual memory system: page table	1	PPT	Group Discussion
20	Virtual memory system: TLB	1	PPT	Group Discussion
5	Summary & Conclusion	1	PPT	Group Discussion

SESSION NUMBER : 37

Session Outcome: 1 Students gain the comprehensive understanding of external storage

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	2	Talk	--- NOT APPLICABLE ---
40	External storage	2	PPT	Group Discussion
5	Summary & Conclusion	2	PPT	Group Discussion

SESSION NUMBER : 38

Session Outcome: 1 Students gain th insights into the concept of IO fundamentals: handshaking, buffering

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	2	Talk	--- NOT APPLICABLE ---
20	IO fundamentals: handshaking	2	PPT	Group Discussion
20	IO fundamentals: buffering	2	PPT	Group Discussion
5	Summary & Conclusion	2	PPT	Group Discussion

SESSION NUMBER : 39

Session Outcome: 1 Students gain the knowledge on Programmed IO, Interrupt driven IO

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	2	Talk	--- NOT APPLICABLE ---
20	Programmed IO	2	PPT	Group Discussion
20	Interrupt driven IO	2	PPT	Group Discussion
5	Summary & Conclusion	2	PPT	Group Discussion

Tutorial Course DELIVERY Plan: NO Delivery Plan Exists

Tutorial Session wise Teaching – Learning Plan

No Session Plans Exists

Practical Course DELIVERY Plan:

Tutorial Session no	Topics	CO-Mapping
1	Introduction and Verification of logic gates	CO5
2	Design and Realization of logic Gates using universal Gates	CO5
3	Combinational Circuit Based Car Security System	CO5

Tutorial Session no	Topics	CO-Mapping
4	Participant selection in Competitions Using Multiplexer	CO5
5	Digital Display of the Department Name using 7-segment decoder	CO5
6	Design of Computational Processing System for Arithmetic and Logical Operations	CO5
7	Random Number Generator for Gaming Using D-Flip- flop	CO5
8	Digital Unlocking System using Shift Register	CO5
9	Design of 4-bit asynchronous counter	CO5
10	Implementation of Information Transmission System	CO5
11	Development of Instruction Processing System from Fetching to Execution	CO5
12	Implementation of Cache Memory	CO5
13	Choice Based Control of Vending Machine	CO5
14	Implementation of 3-Stage Pipelining	CO5

Practical Session wise Teaching – Learning Plan

SESSION NUMBER : 1

Session Outcome: 1 Students able to develop the practical skills in digital design ang computer architecture through hands-on laboratory experience

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
10	Attendance	4	Talk	--- NOT APPLICABLE ---
20	Introduction to logisim	4	PPT	--- NOT APPLICABLE ---
30	Introduction to hardware components	4	PPT	--- NOT APPLICABLE ---
30	Verification of logic gates	4	PPT	--- NOT APPLICABLE ---
10	Summary & Conclusion	4	PPT	--- NOT APPLICABLE ---

SESSION NUMBER : 2

Session Outcome: 1 Students able to design all logic gates using universal gates

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
10	Attendance	4	Talk	--- NOT APPLICABLE ---
20	Description- Realization of logic Gates using universal Gates	4	PPT	--- NOT APPLICABLE ---
30	Implementation of logic Gates using universal Gates	4	PPT	--- NOT APPLICABLE ---
30	Results & Discussion	4	PPT	--- NOT APPLICABLE ---
10	Summary & Conclusion	4	PPT	--- NOT APPLICABLE ---

SESSION NUMBER : 3

Session Outcome: 1 Students able to design all logic gates using universal gates

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
10	Attendance	4	Talk	--- NOT APPLICABLE ---
20	Description- Combinational Circuit Based Car Security System	4	PPT	--- NOT APPLICABLE ---
30	Implementation- Combinational Circuit Based Car Security System	4	PPT	--- NOT APPLICABLE ---
30	Results & Discussion	4	PPT	--- NOT APPLICABLE ---
10	Summary & Conclusion	4	PPT	--- NOT APPLICABLE ---

SESSION NUMBER : 4

Session Outcome: 1 Students able to utilize multiplexers for efficient participant selection in competitions, showcasing the application of digital circuits in event management

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
10	Attendance	4	Talk	--- NOT APPLICABLE ---
20	Description- Participant selection in Competitions Using Multiplexer	4	PPT	--- NOT APPLICABLE ---
30	Implementation- Participant selection in Competitions Using Multiplexer	4	PPT	--- NOT APPLICABLE ---
30	Results & Discussion	4	PPT	--- NOT APPLICABLE ---
10	Summary & Conclusion	4	PPT	--- NOT APPLICABLE ---

SESSION NUMBER : 5

Session Outcome: 1 Students able to create Digital Display of the Department Name using 7-segment decoder

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
10	Attendance	4	Talk	--- NOT APPLICABLE ---
20	Description- Digital Display of the Department Name using 7-segment decoder	4	PPT	--- NOT APPLICABLE ---
30	Implementation- Digital Display of the Department Name using 7-segment decoder	4	PPT	--- NOT APPLICABLE ---
30	Results & Discussion	4	PPT	--- NOT APPLICABLE ---
10	Summary & Conclusion	4	PPT	--- NOT APPLICABLE ---

SESSION NUMBER : 6

Session Outcome: 1 Students able to develop a Computational Processing System for Arithmetic and Logical Operations

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
10	Attendance	4	Talk	--- NOT APPLICABLE ---
20	Description- Computational Processing System for Arithmetic and Logical Operations	4	PPT	--- NOT APPLICABLE ---

30	Implementation- Computational Processing System for Arithmetic and Logical Operations	4	PPT	--- NOT APPLICABLE ---
30	Results & Discussion	4	PPT	--- NOT APPLICABLE ---
10	Summary & Conclusion	4	PPT	--- NOT APPLICABLE ---

SESSION NUMBER : 7

Session Outcome: 1 Students able to design a Random Number Generator for Gaming Using D-Flip- flop

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
10	Attendance	4	Talk	--- NOT APPLICABLE ---
20	Description- Random Number Generator for Gaming Using D-Flip- flop	4	PPT	--- NOT APPLICABLE ---
30	Implementation- Random Number Generator for Gaming Using D-Flip-flop	4	PPT	--- NOT APPLICABLE ---
30	Results & Discussion	4	PPT	--- NOT APPLICABLE ---
10	Summary & Conclusion	4	PPT	--- NOT APPLICABLE ---

SESSION NUMBER : 8

Session Outcome: 1 Students able to develop a secure Digital Unlocking System using Shift Register

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
10	Attendance	4	Talk	--- NOT APPLICABLE ---
20	Description- Digital Unlocking System using Shift Register	4	PPT	--- NOT APPLICABLE ---
30	Implementation- Digital Unlocking System using Shift Register	4	PPT	--- NOT APPLICABLE ---
30	Results & Discussion	4	PPT	--- NOT APPLICABLE ---
10	Summary & Conclusion	4	PPT	--- NOT APPLICABLE ---

SESSION NUMBER : 9

Session Outcome: 1 Students bale to design an asynchronous counter using flip- flops

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
10	Attendance	4	Talk	--- NOT APPLICABLE ---
20	Description- 4-bit asynchronous counter	4	PPT	--- NOT APPLICABLE ---
30	Implementation- 4-bit asynchronous counter	4	PPT	--- NOT APPLICABLE ---
30	Results & Discussion	4	PPT	--- NOT APPLICABLE ---
10	Summary & Conclusion	4	PPT	--- NOT APPLICABLE ---

SESSION NUMBER : 10

Session Outcome: 1 Students able to Implement an Information Transmission System

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
5	Attendance	4	Talk	--- NOT APPLICABLE ---
20	Description- Information Transmission System	4	PPT	--- NOT APPLICABLE ---
30	Implementation- Information Transmission System	4	PPT	--- NOT APPLICABLE ---
30	Results & Discussion	4	PPT	--- NOT APPLICABLE ---
10	Summary & Conclusion	4	PPT	--- NOT APPLICABLE ---

SESSION NUMBER : 11

Session Outcome: 1 Students able to optimize the instruction processing system seamlessly integrating stages from instruction fetching to execution for enhanced performance

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
10	Attendance	4	Talk	--- NOT APPLICABLE ---
20	Description- Instruction Processing System from Fetching to Execution	4	PPT	--- NOT APPLICABLE ---
30	Implementation- Instruction Processing System from Fetching to Execution	4	PPT	--- NOT APPLICABLE ---
30	Results & Discussion	4	PPT	--- NOT APPLICABLE ---
10	Summary & Conclusion	4	PPT	--- NOT APPLICABLE ---

SESSION NUMBER : 12

Session Outcome: 1 Students able to understand the cache memory for efficient storage and retrieval of frequently accessed data

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
10	Attendance	4	Talk	--- NOT APPLICABLE ---
20	Description of cache memory	4	PPT	--- NOT APPLICABLE ---
30	Implementation of Cache Memory	4	PPT	--- NOT APPLICABLE ---
30	Results & Discussion	4	PPT	--- NOT APPLICABLE ---
10	Summary & Conclusion	4	PPT	--- NOT APPLICABLE ---

SESSION NUMBER : 13

Session Outcome: 1 Students able to understand the functionality of vending machine using choice based control system

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
10	Attendance	4	Talk	--- NOT APPLICABLE ---
20	Description- Choice Based Control of Vending Machine	4	PPT	--- NOT APPLICABLE ---
30	Implementation- Choice Based Control of Vending Machine	4	PPT	--- NOT APPLICABLE ---

30	Results & Discussion	4	PPT	--- NOT APPLICABLE ---
10	Summary & Conclusion	4	PPT	--- NOT APPLICABLE ---

SESSION NUMBER : 14

Session Outcome: 1 Students able to implement a three stage pipeline architecture

Time(min)	Topic	BTL	Teaching-Learning Methods	Active Learning Methods
10	Attendance	4	Talk	--- NOT APPLICABLE ---
20	Description of 3-Stage Pipelining	4	PPT	--- NOT APPLICABLE ---
30	Implementation of 3-Stage Pipelining	4	PPT	--- NOT APPLICABLE ---
30	Results & Discussion	4	PPT	--- NOT APPLICABLE ---
10	Summary & Conclusion	4	PPT	--- NOT APPLICABLE ---

Skilling Course DELIVERY Plan: NO Delivery Plan Exists

Skilling Session wise Teaching – Learning Plan

No Session Plans Exists

WEEKLY HOMEWORK ASSIGNMENTS/ PROBLEM SETS/OPEN ENDEDED PROBLEM-SOLVING EXERCISES etc:

Week	Assignment Type	Assignment No	Topic	Details	co
2	Weekly Homework Assignments	1	Multiplexer and Demultiplexer PLD's	1. Draw and explain the operation of 4:1 Mux and 1:4 demux. 2. How do AND gates and OR gates contribute to the implementation of combinational logic functions in PAL and PLA devices?	CO1
3	Weekly Homework Assignments	1	K-Maps & FPGA, CPLD's	1. Optimize the following 3-variable Boolean function: $F(A,B,C)=\Sigma(1,2,4,6)$ using Karnaugh Maps. 2. Sketch the digital logic modules of FPGA and CPLD	CO1
4	Weekly Homework Assignments	2	Counters and Memories	1. Explore the applications of Ring Counters in digital systems. How are they utilized in various scenarios, and what advantages do they offer over other types of counters? 2. Differentiate between volatile and non-volatile memory. Why is RAM considered volatile, and how does this characteristic influence its usage in a computer system?	CO2
5	Weekly Homework Assignments	2	D - Flip flops	2. Design a random number generator for gaming using D-flipflops	CO2
6	Weekly Homework Assignments	2	Shift Registers	1. Design a Digital Unlocking System using Shift Register	CO2
7	Weekly Homework Assignments	3	ALP, Hazards	1. Define operands in the context of computer instructions. What are the different types of operands commonly used in assembly language programming? 2. Explain the concept of pipeline hazards.	CO3

				What are data hazards, control hazards, and structural hazards, and how do they impact the smooth execution of instructions in a pipeline?	
9	Weekly Homework Assignments	3	Instruction cycle & CISC, RISC	1. Define a machine cycle and break down the components, including fetch, decode, execute, and store. 2. Explore and contrast the architectural features and design philosophies of RISC and CISC architectures.	CO3
10	Weekly Homework Assignments	4	Page Table	1. Provide examples of real-world scenarios where temporal locality is exhibited. How does the repeated use of certain data within a short time frame benefit from the concept of temporal locality? 2. Describe the typical structure of a page table. What information is stored in the page table entries, and how does the operating system use this information during address translation?	CO4
11	Weekly Homework Assignments	4	Main memory & Handshaking	1. Compare and contrast the characteristics and functionalities of main memory in a computer system. 2. How does handshaking facilitate communication between devices in a computer system?	CO4

COURSE TIME TABLE:

	Hour	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
Day	Component									
Mon	Theory	---	---	V-S15,V-S16	V-S15,V-S16	V-S7,V-S8,V-S9,V-S10,V-S11,V-S12	V-S7,V-S8	V-S35,V-S36	V-S35,V-S36	V-S47,V-S48
	Tutorial	---	---	--	--	--	--	--	--	--
	Lab	---	---	V-S13,V-S13,V-S13,V-S14,V-S14,V-S14	V-S13,V-S13,V-S13,V-S14,V-S14,V-S14	V-S5,V-S5,V-S5,V-S6,V-S6,V-S6	V-S5,V-S5,V-S5,V-S6,V-S6,V-S6	V-S33,V-S33,V-S33,V-S34,V-S34,V-S34	V-S33,V-S33,V-S33,V-S34,V-S34,V-S34	V-S45,V-S45,V-S45,V-S46,V-S46,V-S46
	Skilling	---	---	--	--	--	--	--	--	--
Tue	Theory	---	---	V-S13,V-S14	V-S13,V-S14	V-S5,V-S6	V-S5,V-S6	V-S33,V-S34,V-S41,V-S42,V-S43,V-S44	V-S33,V-S34	V-S45,V-S46,V-S53,V-S54,V-S55,V-S56
	Tutorial	---	---	--	--	--	--	--	--	--
	Lab	---	---	V-S15,V-S15,V-S15,V-S16,V-S16,V-S16	V-S15,V-S15,V-S15,V-S16,V-S16,V-S16	V-S7,V-S7,V-S7,V-S8,V-S8,V-S8	V-S7,V-S7,V-S7,V-S8,V-S8,V-S8	V-S35,V-S35,V-S35,V-S36,V-S36,V-S36	V-S35,V-S35,V-S35,V-S36,V-S36,V-S36	V-S47,V-S47,V-S47,V-S48,V-S48,V-S48
	Skilling	---	---	--	--	--	--	--	--	--
Wed	Theory	V-S13,V-S14,V-S15,V-S16,V-S27,V-S28	V-S27,V-S28	V-S19,V-S20	V-S19,V-S20	V-S11,V-S12	V-S11,V-S12	V-S39,V-S40	V-S39,V-S40	V-S49,V-S50,V-S51,V-S52,V-S55,V-S56
	Tutorial	--	--	--	--	--	--	--	--	--

	Lab	V-S25,V-S25,V-S25,V-S26,V-S26,V-S26	V-S25,V-S25,V-S25,V-S26,V-S26,V-S26	V-S17,V-S17,V-S17,V-S18,V-S18,V-S18	V-S17,V-S17,V-S17,V-S18,V-S18,V-S18	V-S9,V-S9,V-S9,V-S10,V-S10,V-S10	V-S9,V-S9,V-S9,V-S10,V-S10,V-S10	V-S37,V-S37,V-S37,V-S38,V-S38,V-S38	V-S37,V-S37,V-S37,V-S38,V-S38,V-S38	V-S53,V-S53,V-S53,V-S54,V-S54,V-S54
	Skilling	--	--	--	--	--	--	--	--	--
Thu	Theory	V-S25,V-S26	V-S25,V-S26	V-S17,V-S18,V-S21,V-S22,V-S23,V-S24	V-S17,V-S18	V-S1,V-S2,V-S3,V-S4,V-S9,V-S10	V-S9,V-S10	V-S33,V-S34,V-S35,V-S36,V-S37,V-S38	V-S37,V-S38	V-S45,V-S46,V-S47,V-S48,V-S51,V-S52
	Tutorial	--	--	--	--	--	--	--	--	--
	Lab	V-S27,V-S27,V-S27,V-S28,V-S28,V-S28	V-S27,V-S27,V-S27,V-S28,V-S28,V-S28	V-S19,V-S19,V-S19,V-S20,V-S20,V-S20	V-S19,V-S19,V-S19,V-S20,V-S20,V-S20	V-S11,V-S11,V-S11,V-S12,V-S12,V-S12	V-S11,V-S11,V-S11,V-S12,V-S12,V-S12	V-S39,V-S39,V-S39,V-S40,V-S40,V-S40	V-S39,V-S39,V-S39,V-S40,V-S40,V-S40	V-S49,V-S49,V-S49,V-S50,V-S50,V-S50
	Skilling	--	--	--	--	--	--	--	--	--
Fri	Theory	V-S25,V-S26,V-S27,V-S28	---	V-S23,V-S24	V-S23,V-S24	V-S3,V-S4	V-S3,V-S4	V-S43,V-S44	V-S37,V-S38,V-S39,V-S40,V-S43,V-S44	V-S53,V-S54
	Tutorial	--	---	--	--	--	--	--	--	--
	Lab	--	---	V-S21,V-S21,V-S21,V-S22,V-S22,V-S22	V-S21,V-S21,V-S21,V-S22,V-S22,V-S22	V-S1,V-S1,V-S1,V-S2,V-S2,V-S2	V-S1,V-S1,V-S1,V-S2,V-S2,V-S2	V-S41,V-S41,V-S41,V-S42,V-S42,V-S42	V-S41,V-S41,V-S41,V-S42,V-S42,V-S42	V-S55,V-S55,V-S55,V-S56,V-S56,V-S56
	Skilling	--	---	--	--	--	--	--	--	--
Sat	Theory	V-S5,V-S6,V-S7,V-S8	---	V-S17,V-S18,V-S19,V-S20,V-S21,V-S22	V-S21,V-S22	V-S1,V-S2	V-S1,V-S2	V-S41,V-S42	V-S41,V-S42	V-S49,V-S50
	Tutorial	--	---	--	--	--	--	--	--	--
	Lab	--	---	V-S23,V-S23,V-S23,V-S24,V-S24,V-S24	V-S23,V-S23,V-S23,V-S24,V-S24,V-S24	V-S3,V-S3,V-S3,V-S4,V-S4,V-S4	V-S3,V-S3,V-S3,V-S4,V-S4,V-S4	V-S43,V-S43,V-S43,V-S44,V-S44,V-S44	V-S43,V-S43,V-S43,V-S44,V-S44,V-S44	V-S51,V-S51,V-S51,V-S52,V-S52,V-S52
	Skilling	--	---	--	--	--	--	--	--	--
Sun	Theory	--	--	--	--	--	--	--	--	--
	Tutorial	--	--	--	--	--	--	--	--	--
	Lab	--	--	--	--	--	--	--	--	--
	Skilling	--	--	--	--	--	--	--	--	--

REMEDIAL CLASSES:

Supplement course handout, which may perhaps include special lectures and discussions that would be planned, and schedule notified according

SELF-LEARNING:

Assignments to promote self-learning, survey of contents from multiple sources.

S.no	Topics	CO	ALM	References/MOOCS

DELIVERY DETAILS OF CONTENT BEYOND SYLLABUS:

Content beyond syllabus covered (if any) should be delivered to all students that would be planned, and schedule notified accordingly.

S.no	Advanced Topics, Additional Reading, Research papers and any	CO	ALM	References/MOOCS

EVALUATION PLAN:

Evaluation Type	Evaluation Component	Weightage/Marks		Assessment Dates	Duration (Hours)	CO1	CO2	CO3	CO4	CO5
End Semester Summative Evaluation Total= 40 %	Lab End Semester Exam	Weightage	16	08.05.2025	120					16
		Max Marks	50							50
	End Semester Exam	Weightage	24	07.05.2025,08.05.2025,09.05.2025,10.05.2025	180	6	6	6	6	
		Max Marks	100			25	25	25	25	
In Semester Formative Evaluation Total= 24 %	Continuous Evaluation - Lab Exercise	Weightage	9	22.01.2025	100					9
		Max Marks	50							50
	Home Assignment and Textbook	Weightage	7	22.01.2025,23.02.2025,29.03.2025,01.05.2025	50	1.75	1.75	1.75	1.75	
		Max Marks	100			25	25	25	25	
	ALM	Weightage	8	22.01.2025,23.02.2025,29.03.2025,01.05.2025	50	2	2	2	2	
		Max Marks	100			25	25	25	25	
In Semester Summative Evaluation Total= 36 %	Lab In Semester Exam	Weightage	8	01.04.2025	100					8
		Max Marks	50							50
	Semester in Exam-II	Weightage	14	29.04.2025, 30.04.2025	90			7	7	
		Max Marks	50					25	25	
	Semester in Exam-I	Weightage	14	11.03.2025, 12.03.2025	90	7	7			
		Max Marks	50			25	25			

ATTENDANCE POLICY:

Every student is expected to be responsible for regularity of his/her attendance in class rooms and laboratories, to appear in scheduled tests and examinations and fulfill all other tasks assigned to him/her in every course
In every course, student has to maintain a minimum of 85% attendance to be eligible for appearing in Semester end examination of the course, for cases of medical issues and other unavoidable circumstances the students will be condoned if their attendance is between 75% to 85% in every course, subjected to submission of medical certificates, medical case file and other needful documental proof to the concerned departments

DETENTION POLICY :

In any course, a student has to maintain a minimum of 85% attendance and In-Semester Examinations to be eligible for appearing to the Semester End Examination, failing to fulfill these conditions will deem such student to have been detained in that course.

PLAGIARISM POLICY :

Supplement course handout, which may perhaps include special lectures and discussions

COURSE TEAM MEMBERS, CHAMBER CONSULTATION HOURS AND CHAMBER VENUE DETAILS:

Supplement course handout, which may perhaps include special lectures and discussions

Name of Faculty	Delivery Component of Faculty	Sections of Faculty	Chamber Consultation Day (s)	Chamber Consultation Timings for each day	Chamber Consultation Room No:	Signature of Course faculty:
Habibulla Khan	L	19-MA	-	-	-	-
Habibulla Khan	P	19-A	-	-	-	-
Siva Ganga Prasad Mutchakayala	L	11-MA,47-MA	-	-	-	-
Siva Ganga Prasad Mutchakayala	P	11-A,47-A	-	-	-	-
Ravi Kumar Mokkapati	L	48-MA	-	-	-	-

Ravi Kumar Mokkapati	P	12-C,42-C,48-A	-	-	-	-
Ravi Kallakunta	L	20-MA	-	-	-	-
Ravi Kallakunta	P	20-A	-	-	-	-
Suresh Namgiri	P	1-C,11-C,36-B,54-B	-	-	-	-
Sridhar Miriyala	L	9-MA,43-MA	-	-	-	-
Sridhar Miriyala	P	9-A,43-A	-	-	-	-
Venkata Durga Mareedu	L	6-MA,56-MA	-	-	-	-
Venkata Durga Mareedu	P	6-A,28-C,38-B,40-B,56-A	-	-	-	-
Rama Krishna Prasad Guda	L	17-MA,52-MA	-	-	-	-
Rama Krishna Prasad Guda	P	17-A,35-B,41-C,52-A	-	-	-	-
Subba Reddy Vasipalli	L	50-MA	-	-	-	-
Subba Reddy Vasipalli	P	50-A	-	-	-	-
BADUGU SURESH	P	8-C,28-B,39-C	-	-	-	-
C H Raghava Prasad	L	53-MA	-	-	-	-
C H Raghava Prasad	P	53-A	-	-	-	-
Siddaiah Nalluri	L	36-MA	-	-	-	-
Siddaiah Nalluri	P	25-B,36-A,38-C,41-B	-	-	-	-
China Satyanarayana Gubbala	P	2-B,4-C,10-B,49-B	-	-	-	-
Gopi Krishna Popuri	P	51-B	-	-	-	-
Banda Sandeep	L	28-MA	-	-	-	-
Banda Sandeep	P	13-B,28-A	-	-	-	-
Srikanth Palagani	L	14-MA	-	-	-	-
Srikanth Palagani	P	14-A,23-B,56-C	-	-	-	-
Katta Rajesh Babu	L	18-MA,41-MA	-	-	-	-
Katta Rajesh Babu	P	5-C,18-A,41-A	-	-	-	-
Kasi Prasad Mannepalli	P	6-C,8-B,39-B,44-C,56-B	-	-	-	-
Bhupati CH	P	1-B,19-B,51-C	-	-	-	-
Vipul Agarwal	L	21-MA,34-MA	-	-	-	-
Vipul Agarwal	P	21-A,34-A	-	-	-	-
Agilesh R	L	27-MA,39-MA	-	-	-	-
Agilesh R	P	6-B,19-C,24-B,27-A,35-C,39-A,52-B	-	-	-	-
Jyothi Ravi Kiran Kumar Dabbakuti	L	23-MA	-	-	-	-
Jyothi Ravi Kiran Kumar Dabbakuti	P	13-C,23-A	-	-	-	-
MOHAN K.N	L	4-MA,26-MA	-	-	-	-
MOHAN K.N	P	4-A,7-C,18-B,26-A,37-B,48-B	-	-	-	-
Venkata Daya Sagar Ketaraju	P	3-B,14-C,33-C	-	-	-	-
Kiran Kumar Eepuri	P	16-B,21-B,44-B,53-C	-	-	-	-

Hasane Shaik	L	12-MA,46-MA	-	-	-	-
Hasane Shaik	P	12-A,21-C,46-A,54-C	-	-	-	-
Sumit Bhushan	P	4-B,17-C	-	-	-	-
Gopi Chatragadda	L	5-MA,54-MA	-	-	-	-
Gopi Chatragadda	P	5-A,17-B,22-C,23-C,54-A	-	-	-	-
Nishant Kumar	L	10-MA,35-MA	-	-	-	-
Nishant Kumar	P	10-A,35-A	-	-	-	-
vyoma singh	L	37-MA	-	-	-	-
vyoma singh	P	22-B,37-A,46-B	-	-	-	-
NAGESH MANTRAVADI	P	7-B,11-B,49-C,55-C	-	-	-	-
VENKATA SAI BOKKISAM	P	27-C	-	-	-	-
SIVANI PINNABOINA	L	1-MA,51-MA	-	-	-	-
SIVANI PINNABOINA	P	1-A,9-C,16-C,45-C,47-B,51-A	-	-	-	-
NAGAMALLI ARASAVALLI	L	38-MA	-	-	-	-
NAGAMALLI ARASAVALLI	P	10-C,15-B,20-B,34-B,36-C,38-A	-	-	-	-
CHINTA MANJUSHA	L	8-MA,40-MA	-	-	-	-
CHINTA MANJUSHA	P	8-A,40-A	-	-	-	-
Suneetha Emmela	L	3-MA,49-MA	-	-	-	-
Suneetha Emmela	P	3-A,9-B,14-B,46-C,47-C,49-A	-	-	-	-
Lakshmi Kuruguntla	L	16-MA,44-MA	-	-	-	-
Lakshmi Kuruguntla	P	12-B,16-A,18-C,33-B,44-A,50-B	-	-	-	-
APPIKATLA PHANI KUMAR	L	13-MA,33-MA	-	-	-	-
APPIKATLA PHANI KUMAR	P	13-A,20-C,33-A,43-B,50-C	-	-	-	-
BANDARU MAMATHA	L	7-MA,45-MA	-	-	-	-
BANDARU MAMATHA	P	2-C,7-A,24-C,26-C,43-C,45-A,55-B	-	-	-	-
SRINIVASARAO ALLURI	P	53-B	-	-	-	-
LAKSHMUNAIDU M	P	48-C	-	-	-	-
RANJAN MAHAPATRA	L	2-MA,25-MA	-	-	-	-
RANJAN MAHAPATRA	P	2-A,15-C,25-A,37-C,52-C	-	-	-	-
SALA SUREKHA	L	24-MA	-	-	-	-
SALA SUREKHA	P	5-B,24-A,45-B	-	-	-	-
ADITYA ANKANA	P	3-C,34-C,42-B	-	-	-	-
Vineetha K V	L	15-MA	-	-	-	-

Vineetha K V	P	15-A	-	-	-	-
GANESH BABU RAJENDRAN	P	26-B	-	-	-	-
Anand Dhanakotti	L	55-MA	-	-	-	-
Anand Dhanakotti	P	27-B,55-A	-	-	-	-
Sourabh Jain	L	22-MA,42-MA	-	-	-	-
Sourabh Jain	P	22-A,25-C,40-C,42-A	-	-	-	-

GENERAL INSTRUCTIONS

Students should come prepared for classes and carry the text book(s) or material(s) as prescribed by the Course Faculty to the class.

NOTICES

Most of the notices are available on the LMS platform.

All notices will be communicated through the institution email.

All notices concerning the course will be displayed on the respective Notice Boards.

Signature of COURSE COORDINATOR

(APPIKATLA PHANI KUMAR)

Signature of Department Prof. Incharge Academics & Vetting Team Member

Department Of DBES-2

HEAD OF DEPARTMENT:

Approval from: DEAN-ACADEMICS
(Sign with Office Seal) [object HTMLDivElement]