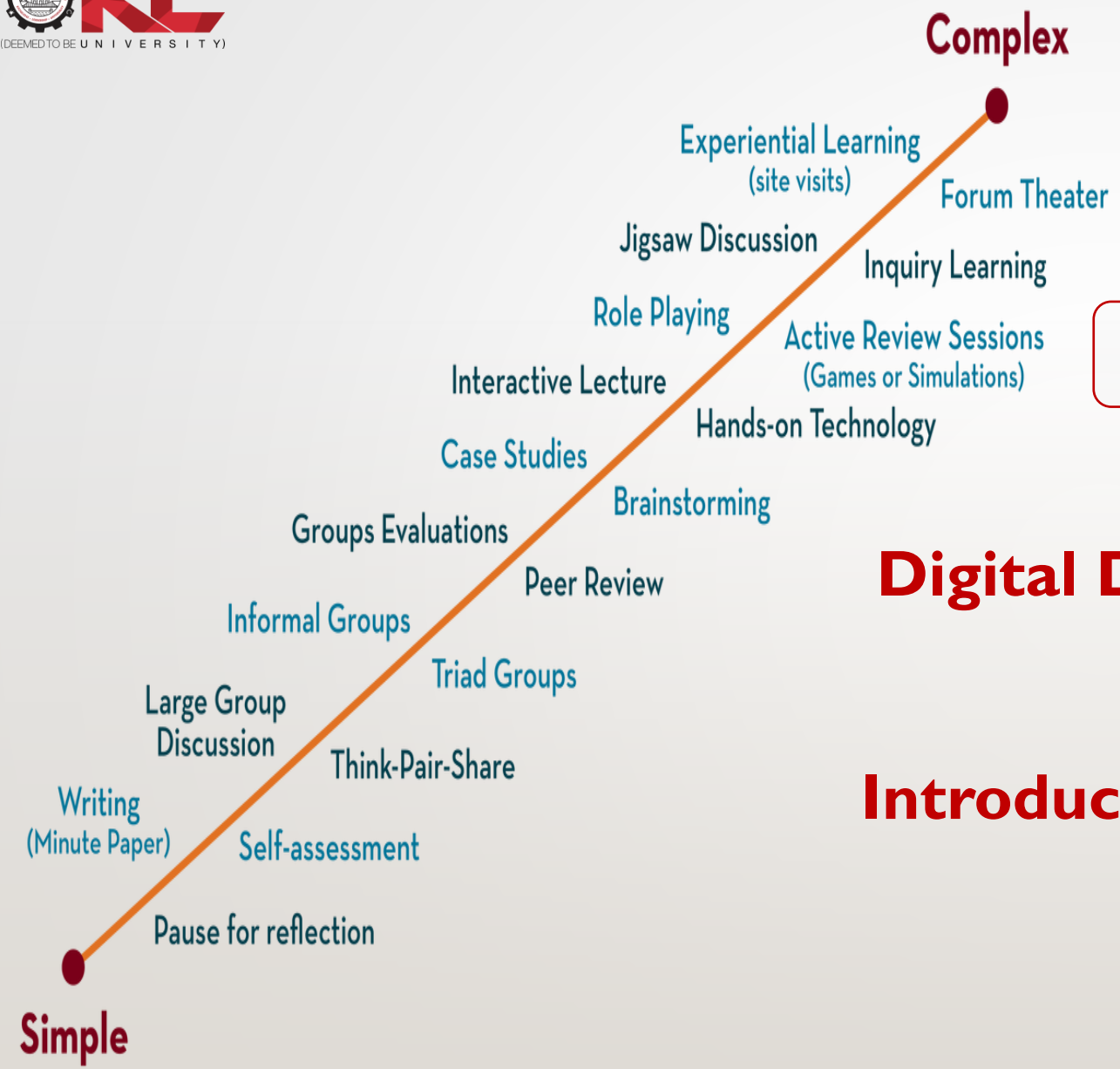


Department of BES-II

Digital Design and Computer Architecture
23EC1202

Topic:

Introduction to Sequential Circuits, Latches and Flip-Flops

Session No: 12 & 13

AIM OF THE SESSION

To familiarize students with the basic concept of Sequential Circuits, Latches and Flip-Flops.

INSTRUCTIONAL OBJECTIVES

This Session is designed to:

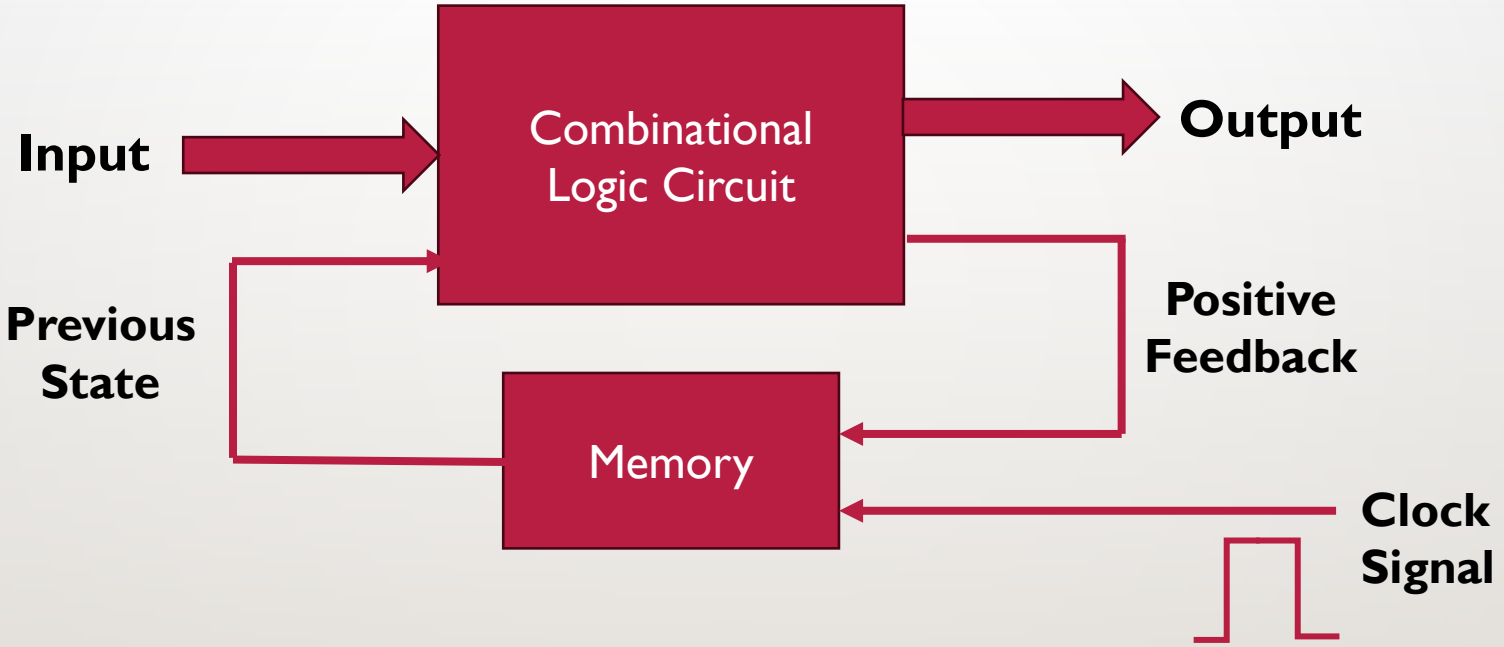
1. Demonstrate the Concept of Sequential Circuits.
2. Describe the Functionality & Characteristics of Latches.
3. Describe the the Role of Flip-Flops.

LEARNING OUTCOMES

At the end of this session, you should be able to:

1. Define the concept of sequential circuits and their role in digital systems.
2. Describe detailed descriptions of the functioning of sequential circuits, emphasizing their ability to retain and process information over time.
3. Summarize the key characteristics of latches, encapsulating their advantages, disadvantages, and applications in a succinct manner.

Combinational Vs Sequential Logic Circuits



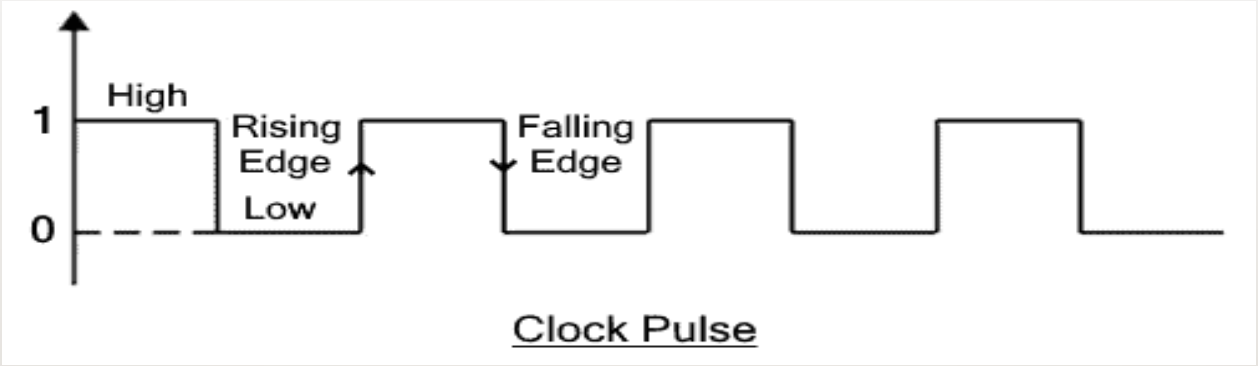
- Sequential circuits, in contrast to combinational circuits, have memory.
- They consider both the current inputs and the history of past inputs (the previous states) to determine their outputs.

Combinational Vs Sequential Logic Circuits

Feature	Combinational Circuits	Sequential Circuits
Dependency on Inputs	Output depends only on current inputs.	Output depends on both current inputs and past states.
Memory Elements	No memory elements.	Contains memory elements (e.g., flip-flops).
Output Determination	Determined instantly based on current inputs.	Determined by both current inputs and past states.
Feedback	No feedback from output to input.	May have feedback from output to input, allowing the circuit to store information.
Timing	No clock signal required.	Synchronized by a clock signal, operates in discrete clock cycles.
Examples	Logic gates, adders, multiplexers.	Flip-flops, registers, counters.
Speed	Typically faster as there is no reliance on clock cycles.	Speed can be limited by clock frequency and cycle time.

NEED OF TRIGGERING

- A synchronous circuit can change its output state only in the presence of a clock signal.
- A clock pulse activates the circuit and then it changes its state based on the input and previous output.



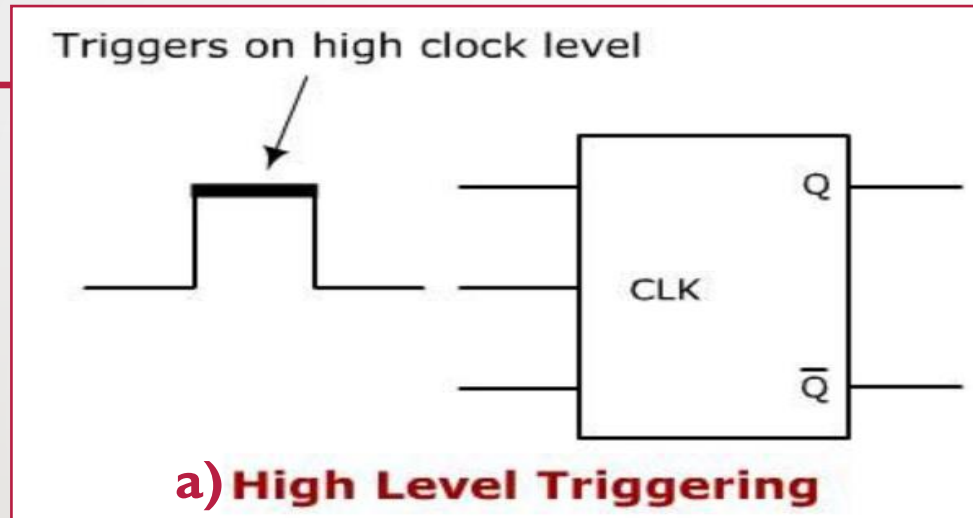
- Triggering ensures precise timing and synchronization of state changes, which is crucial for reliable circuit operation.

Sequential Circuit: Types of Triggering

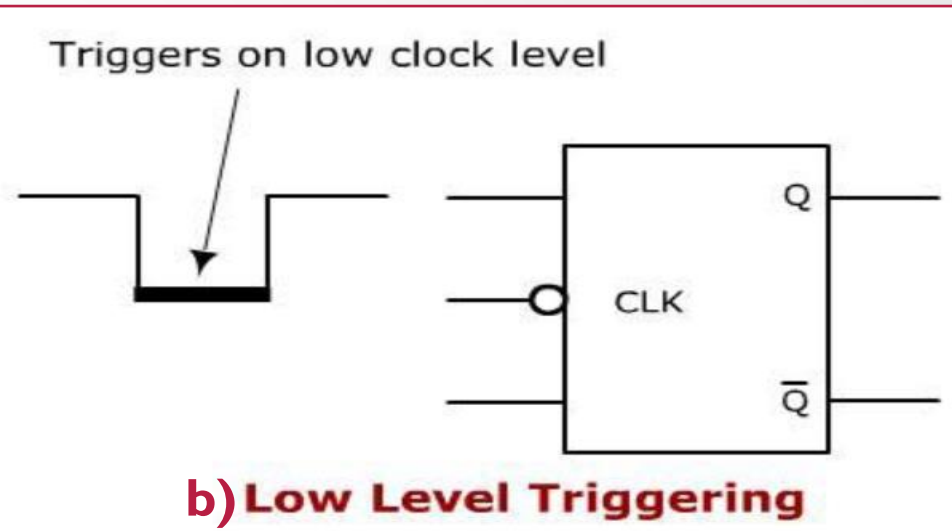
There are two types of triggering/activation in the memory element devices.

i. Pulse-triggered ii. Edge-triggered

i. Pulse Triggered

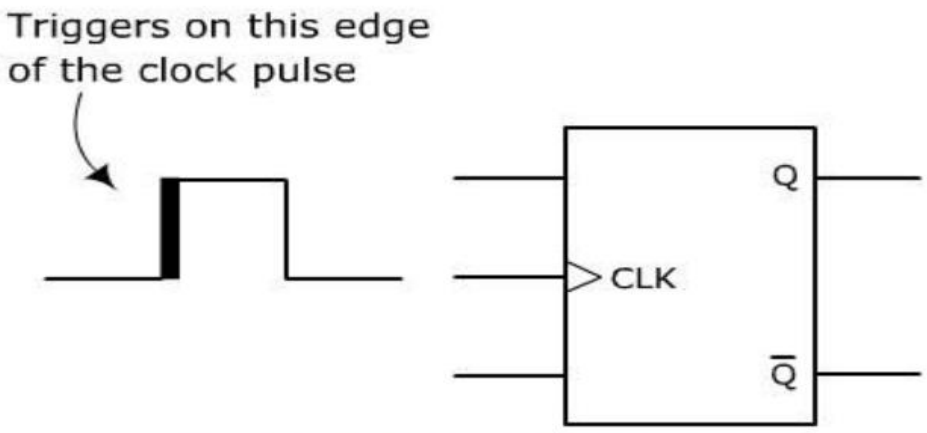


a) High Level Triggering

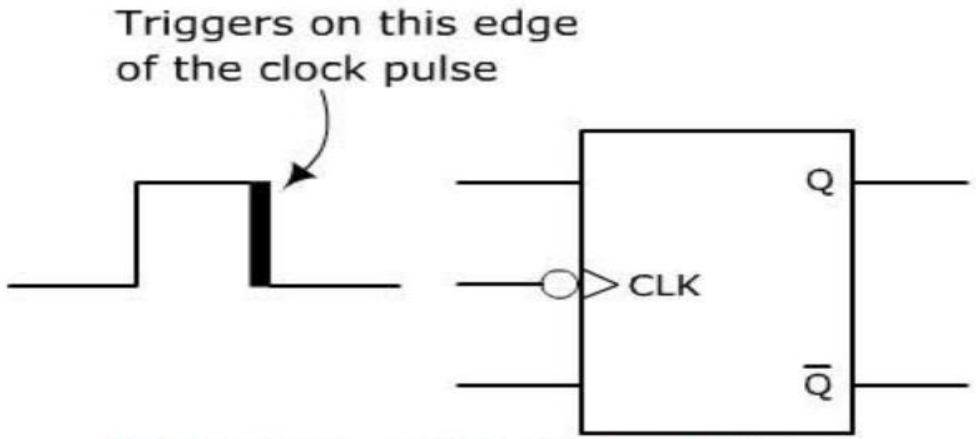


b) Low Level Triggering

ii. Edge Triggered



a) Positive Edge Triggering



b) Negative Edge Triggering

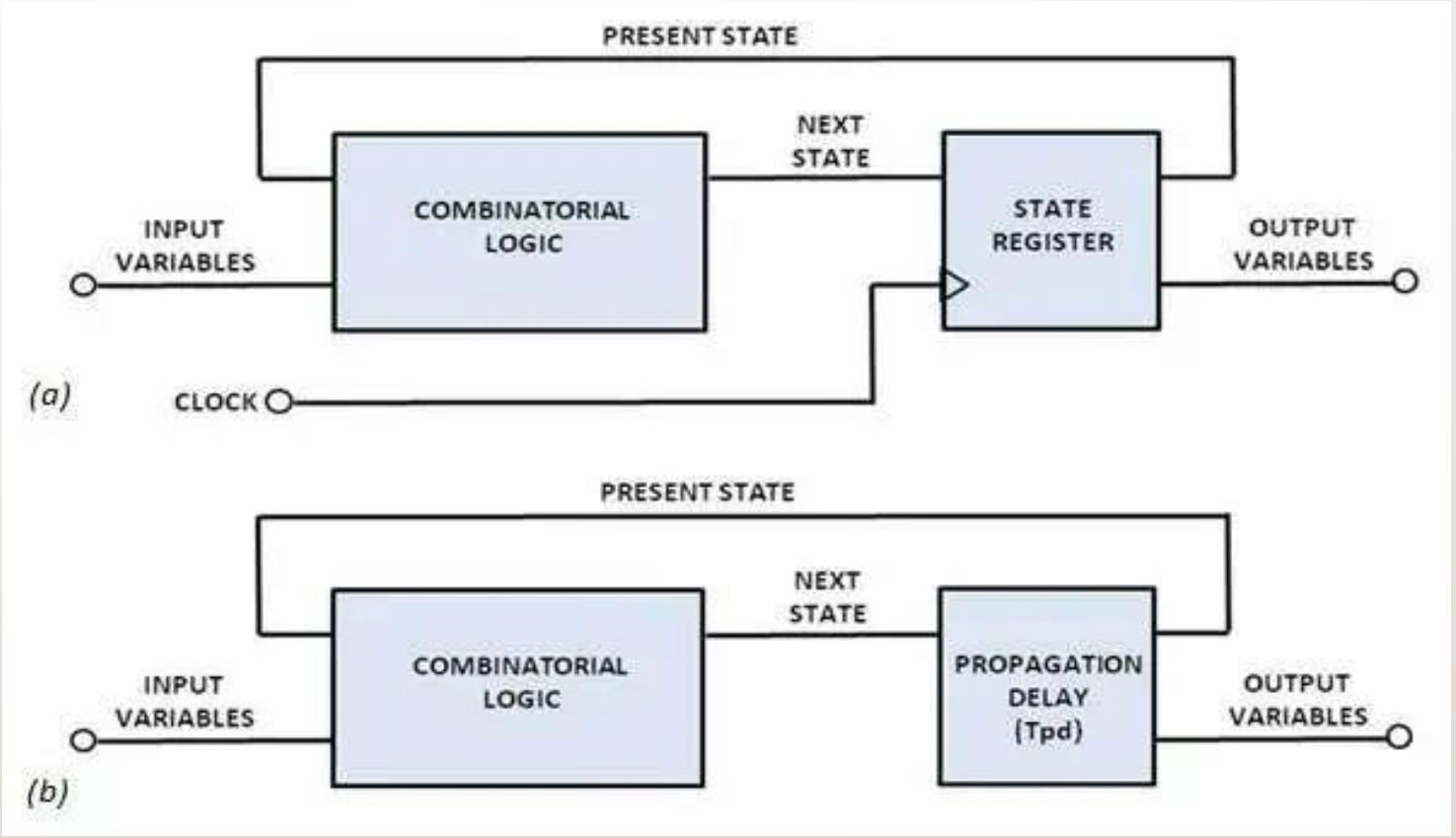
APPLICATIONS OF TRIGGERING

- Level-triggered circuits are commonly used in asynchronous systems where signals are not synchronized to a global clock.
- Edge triggering is frequently used in synchronous circuits, such as counters and flip-flops.

Types of Sequential Circuits

Synchronous sequential circuit

Asynchronous sequential circuit



Synchronous Vs Asynchronous Sequential Circuits

Synchronous sequential circuits	Asynchronous sequential circuits
Change their state only at specific intervals, dictated by a clock signal.	Do not rely on a clock signal for their operation, they change states immediately in response to changes in input.
Memory elements are clocked flip-flops	Memory elements are unclocked flip-flops or time delay elements.
Easier to design and Clock-Dependent Delay	More difficult to design & responds immediately to changes in input

Latches & Flip-flops

Both (Latches & Flip-flops) are building blocks of sequential circuits.

Latches	Flip-flops
Continuously checks its inputs and changes output accordingly.	Continuously checks its inputs and changes output at times determined by the clock signal.
Level Triggered	Edge Triggered
Requires Enable signal to function	Requires clock to function
Made up of Logic gate blocks	Made up of Latches and Logic gates

ASYNCHRONOUS INPUTS TO FLIP-FLOPS

- Some Flip-Flops have asynchronous inputs that are used to force the Flip-Flop to particular state independent of the clock. The inputs that sets the Flip-Flop to 1 is called **PRESET** or **direct set.**
- The input that clears Flip-Flop to 0 is called **clear or direct reset.**.

The usual designations of the inputs are $\overline{PRE}$ and $\overline{CLR}$.

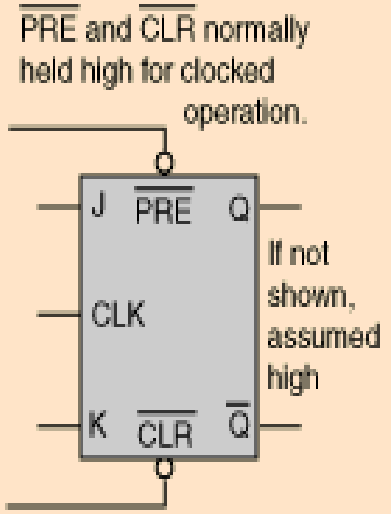
The actions of these inputs are as follows:

$\overline{PRE} = \overline{CLR} = 1$: Inputs inactive so that normal synchronous inputs and clock determine state.

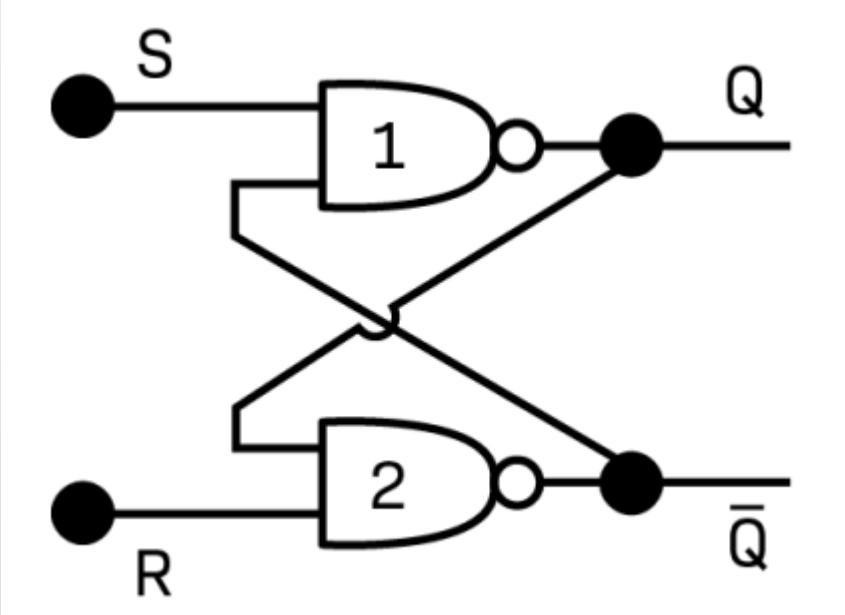
$\overline{PRE} = 0$, $\overline{CLR} = 1$: Q=1 set, unaffected by clock, J, K.

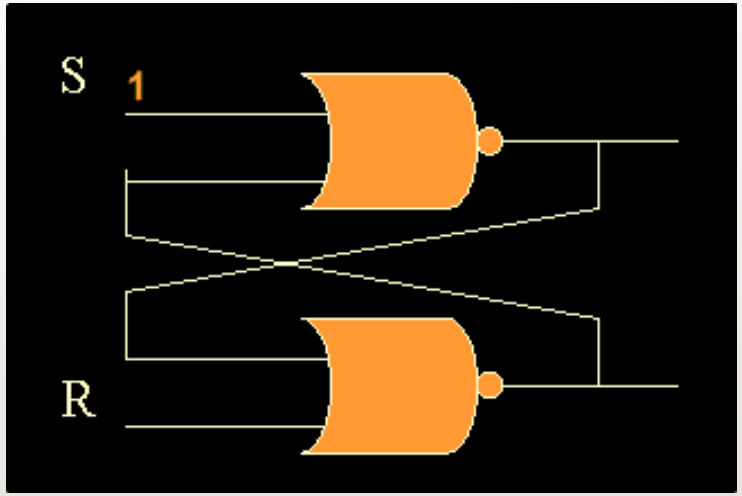
$\overline{PRE} = 1$, $\overline{CLR} = 0$: Q=0, cleared regardless of other inputs.

$\overline{PRE} = \overline{CLR} = 0$: Ambiguous state, to be avoided.



SR LATCH



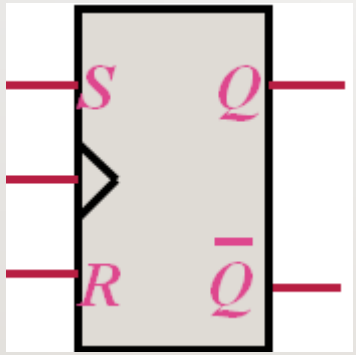


Truth Table

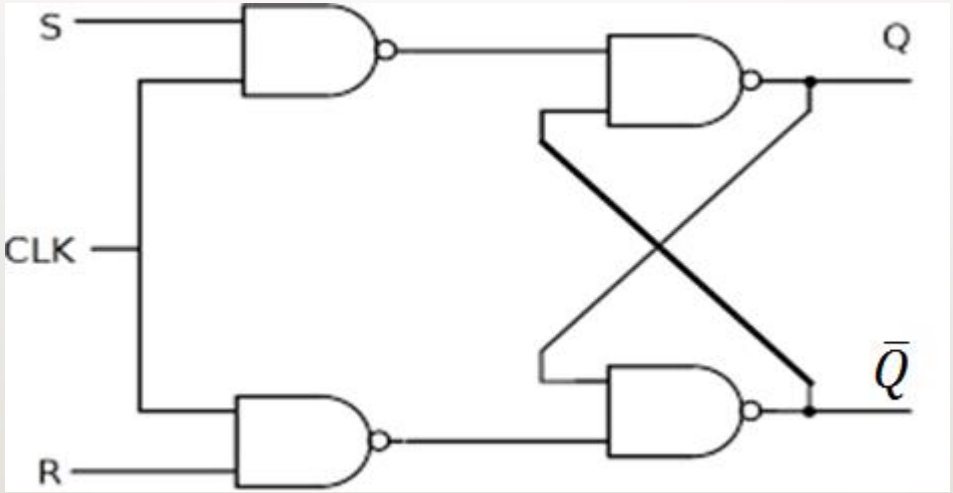
S	R	Q	$\bar{Q}$
0	0	NOT USED	
0	1	1	0
1	0	0	1
* 1	1	NO CHANGE	

SR Flip-flop

Logic Symbol:



SR Flip-flop using NAND Gates:



Truth Table:

S	R	Q (t+1)
0	0	Q (t)
0	1	0
1	0	1
1	1	Invalid

SR Flip-flop

Characteristic Table:

S	R	Q(t)	Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	Invalid
1	1	1	Invalid

Characteristic Equation:

$$Q(t+1) = S + \bar{R}\,Q(t)$$

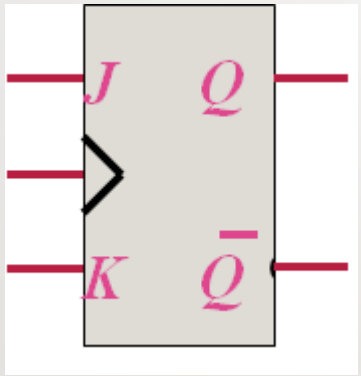
Excitation Table:

Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

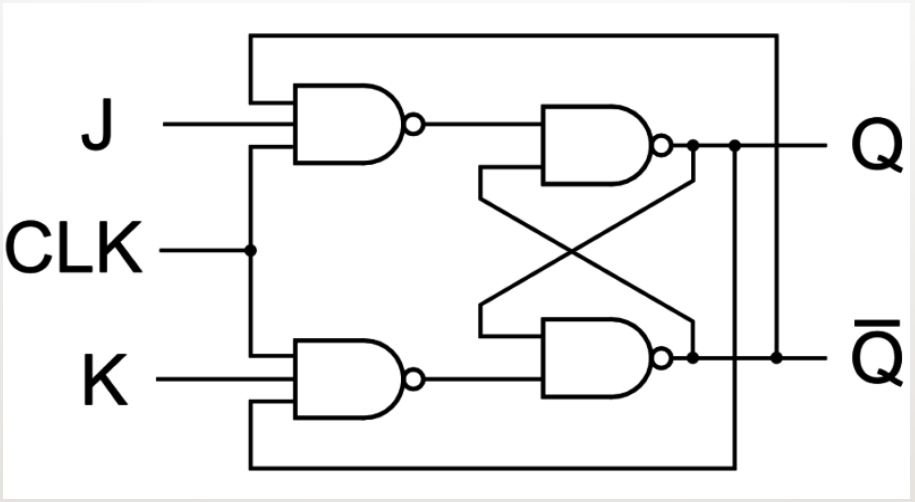
JK Flip-flop

Logic Symbol:

Clk



JK Flip-flop using NAND Gates:



Truth Table:

J	K	Q (t+1)
0	0	Q (t)
0	1	0
1	0	1
1	1	$\overline{Q(t)}$

$Q(t)$

JK Flip-flop

Characteristic Table:

J	K	Q(t)	Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Characteristic Equation:

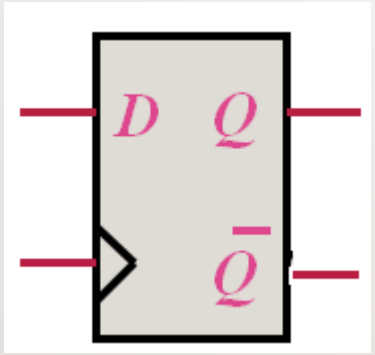
$$Q(t+1) = J\overline{Q(t)} + \overline{K}Q(t)$$

Excitation Table:

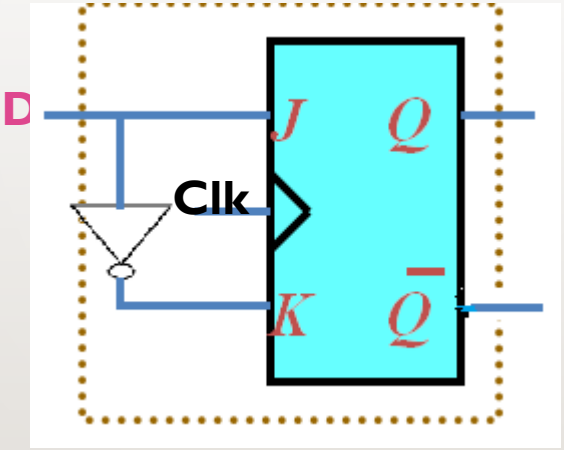
Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

D Flip-flop

Logic Symbol:



D Flip-flop using JK flip-flop:



Truth Table:

D	Q(t+1)
0	0
1	1

- D flip-flop is known as Data or Delay Flip-flop, used in registers to store information.

D Flip-flop

Characteristic Table:

D	Q(t)	Q(t+1)
0	0	0
0	1	0
1	0	1
1	1	1

Characteristic Equation:

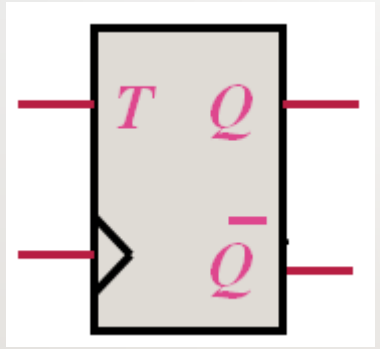
$$Q(t+1) = D$$

Excitation Table:

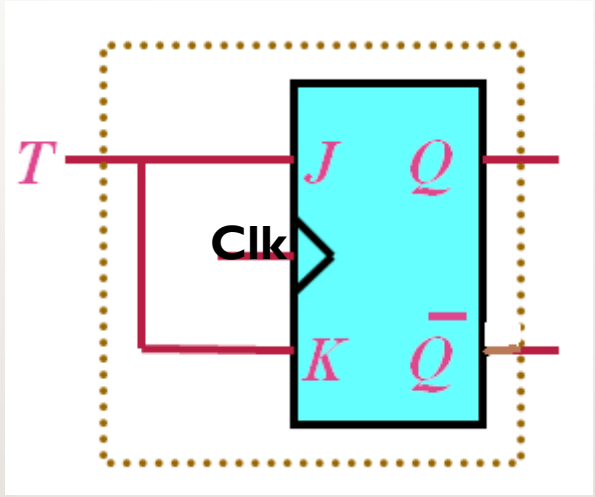
Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

T Flip-flop

Logic Symbol:



T Flip-flop using JK flip-flop:



Truth Table:

T	Q(t+1)
0	Q(t)
1	$\overline{Q(t)}$

- T flip-flop is known as Toggle Flip-flop, used in counters.

T Flip-flop

Characteristic Table:

T	Q(t)	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Characteristic Equation:

$$Q(t+1) = T \oplus Q(t)$$

Excitation Table:

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

SUMMARY

- Sequential circuits are complex digital systems where the output depends not only on the current inputs but also on the history of inputs

- Latches are basic memory components used in sequential circuits, operating on a level-triggering mechanism.

- Flip-flops, a more sophisticated type of memory element than latches, function on an edge-triggering mechanism, changing state at specific moments (e.g., the edges of a clock pulse).

SELF-ASSESSMENT QUESTIONS

1. Latches in digital circuits are used for:

A. Converting digital signals to analog
B. Storing data temporarily based on the level of input signals
C. Generating clock signals
D. Reducing noise in digital signals

2. What is the primary advantage of using a JK flip-flop over an SR flip-flop?

A. Simplicity of design
B. Absence of an invalid state
C. Lower power consumption
D. Faster operation

SELF-ASSESSMENT QUESTIONS

3. What is the primary function of the T (Toggle) input in a T flip-flop?

A. Sets the flip-flop to a high state
B. Resets the flip-flop to a low state
C. Toggles the flip-flop's output state
D. Disables the clock signal

4. What happens when both inputs (J and K) are set to 1 in a JK flip-flop?

A. It enters an invalid state
B. The flip-flop is cleared
C. It toggles its output state
D. The flip-flop is set

TERMINAL QUESTIONS

Short answer questions:

1. Compare and contrast a Latch and Flip-flop in controlling the logic of the system.
2. Describe the need of clocking in flip-flops.
3. Outline the drawback of a JK flip-flop.
4. Draw the block diagram of a sequential circuit.

Long answer questions:

1. Identify and categorize the various types of triggering mechanisms utilized in digital circuits.
2. Develop an SR flip-flop logic diagram and describe the operation using truth table.
3. Develop the SR flip-flop characteristics table and excitation table.

TERMINAL QUESTIONS

Long answer questions:

4. Illustrate the difference between a latch and a flip-flop.
5. Develop the T flip-flop, D flip-flop characteristics table and excitation table.
6. Develop the JK flip-flop characteristics table and excitation table.

REFERENCES FOR FURTHER LEARNING OF THE SESSION

Reference Books:

1. Computer System Architecture by M. Moris Mano
2. Fundamentals of Digital Logic with Verilog HDL by Stephen Brown and ZvonkoVranesic

Sites and Web links:

1. https://www.tutorialspoint.com/computer_logical_organization/sequential_circuits.html
2. https://dept-info.labri.fr/~strandh/Teaching/AMP/Common/Strandh-Tutorial/flip-flops.html

THANK YOU

(DEEMED TO BE UNIVERSITY)

Team – Digital Design & Computer Architecture