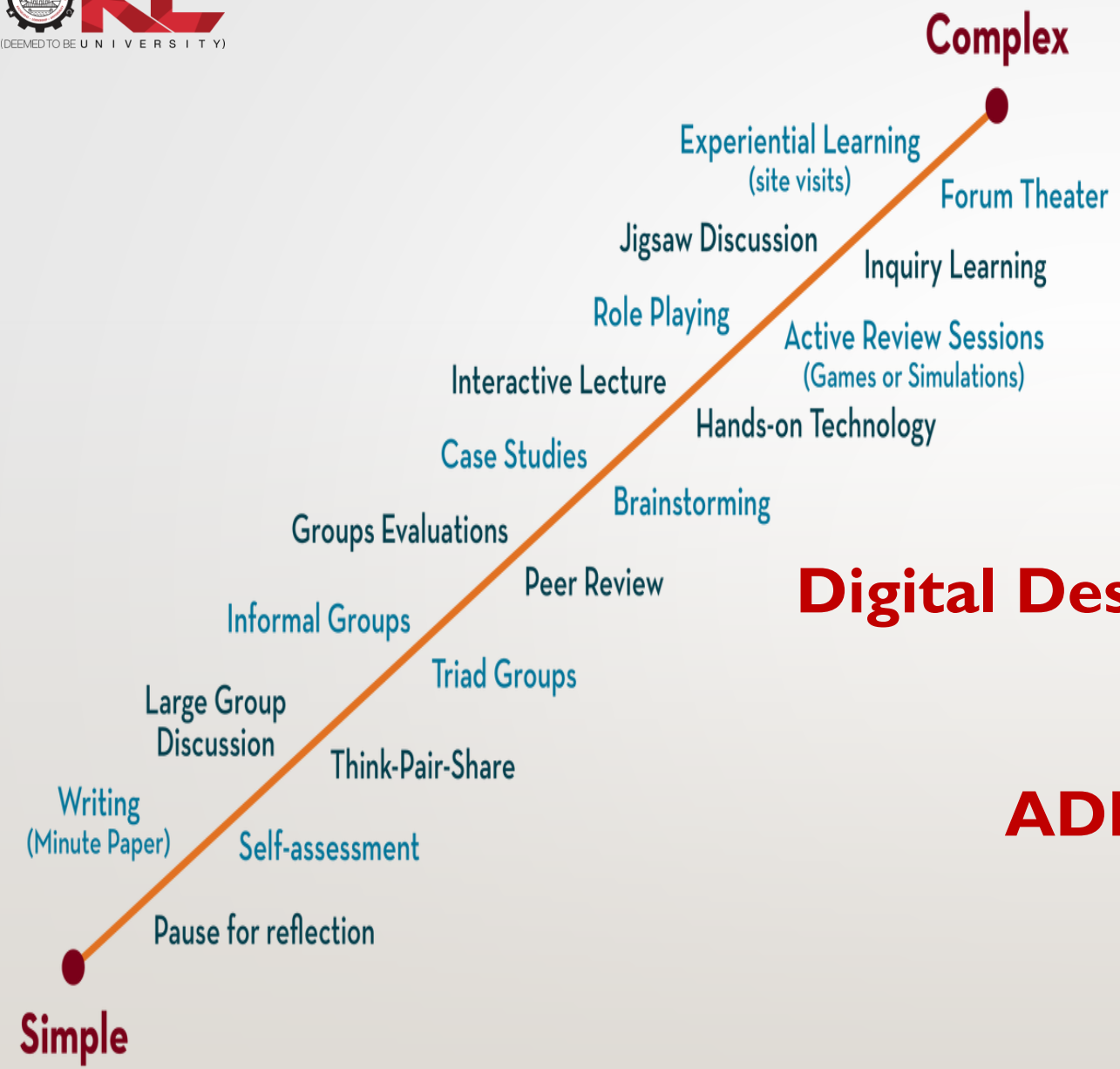


Department of BES-II

Digital Design and Computer Architecture

23EC1202

Topic:

ADDERS & SUBTRACTORS

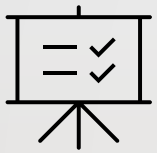
Session No: 04

(DEEMED TO BE UNIVERSITY)

AIM OF THE SESSION

To familiarize students with the basic design concept of Adders & Subtractors

INSTRUCTIONAL OBJECTIVES



This Session is designed to:

1. Demonstrate the logic design of Adders & sub tractors
2. Describe working functions of logic adders and sub tractors using Truth tables
3. List out the uses of adders and sub tractors in real time
4. Describe the design of parallel adders and subtractors

LEARNING OUTCOMES

At the end of this session, you should be able to:

1. Define Half adders and full adders
2. Describe truth tables for logic circuits
3. Summarize design of adders and subtractors

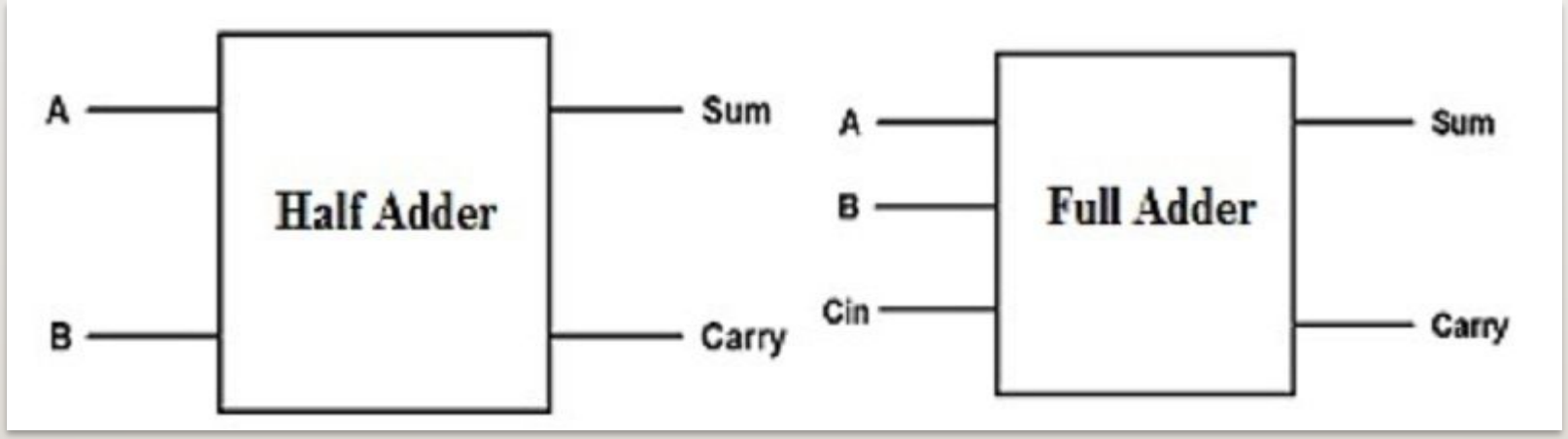
SESSION INTRODUCTION

HALF ADDER:

- It adds two bits of data and generate sum and carry.
- It has 2 inputs and 2 outputs

FULL ADDER:

- It adds three bits of data and generate sum and carry.
- It has 3 inputs and 2 outputs



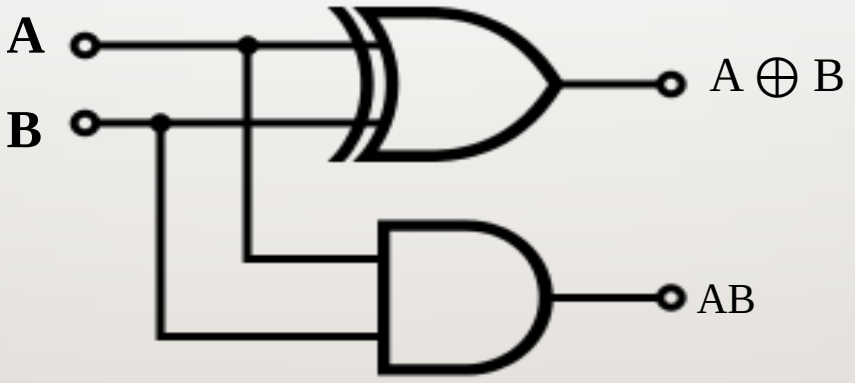
HALF ADDER

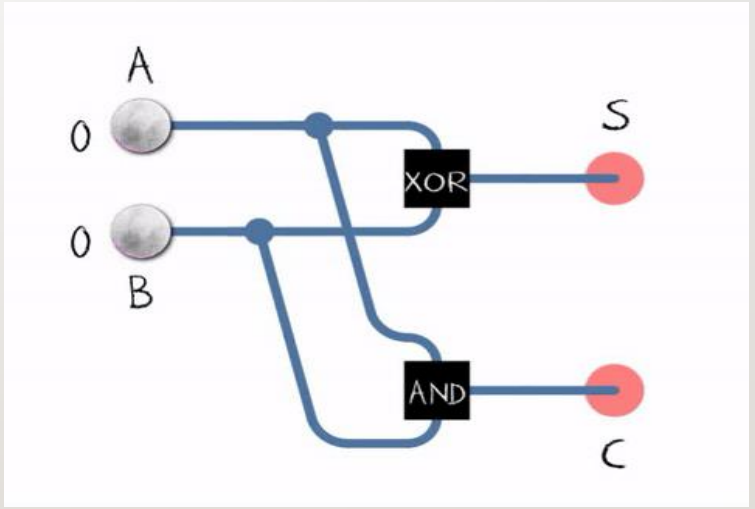
- Recall basic rules for binary addition: 0+0=0, 0+1=1, 1+0=1, 1+1=10
- The operations are performed by logic circuit is called Half adder.

Truth Table:

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Logic Diagram:





Output Expressions: Sum = A'B+AB'=A ⊕ B Carry = AB

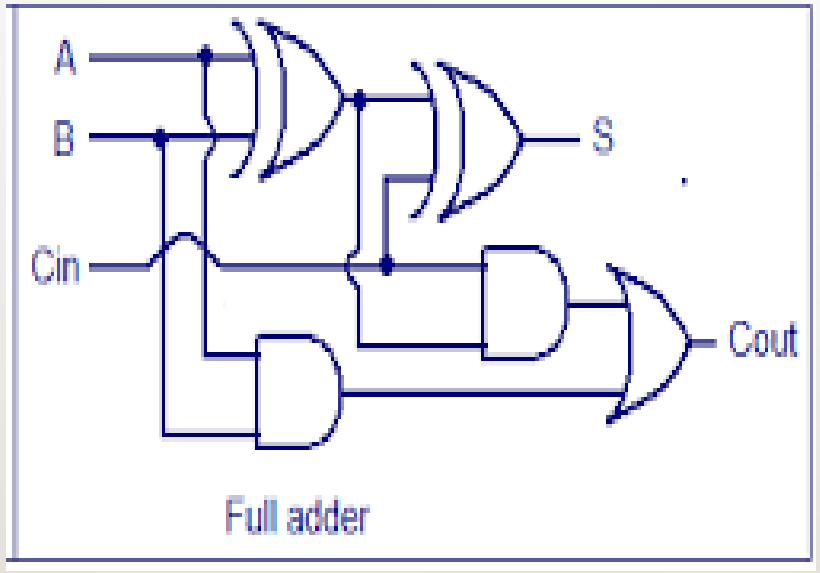
FULL ADDER

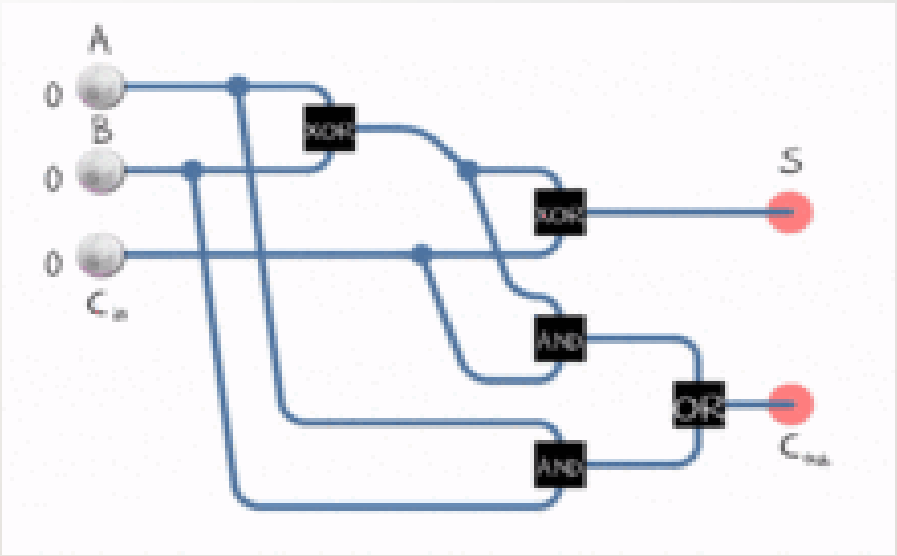
- Full adder accepts two inputs bits and one input carry and generates a sum output and output carry
- The basic difference between Half adder and Full adder is that the full adder accepts input carry

Truth Table:

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Logic Diagram:





Output Expressions:

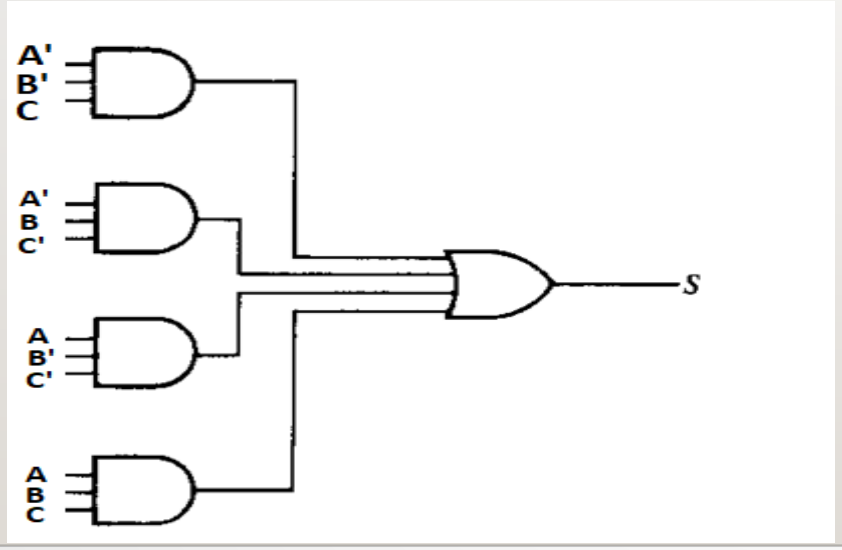
SUM = $\sum m(1,2,4,7)$
= A'.B'.C+A'.B.C'+A.B'.C'+A.B.C

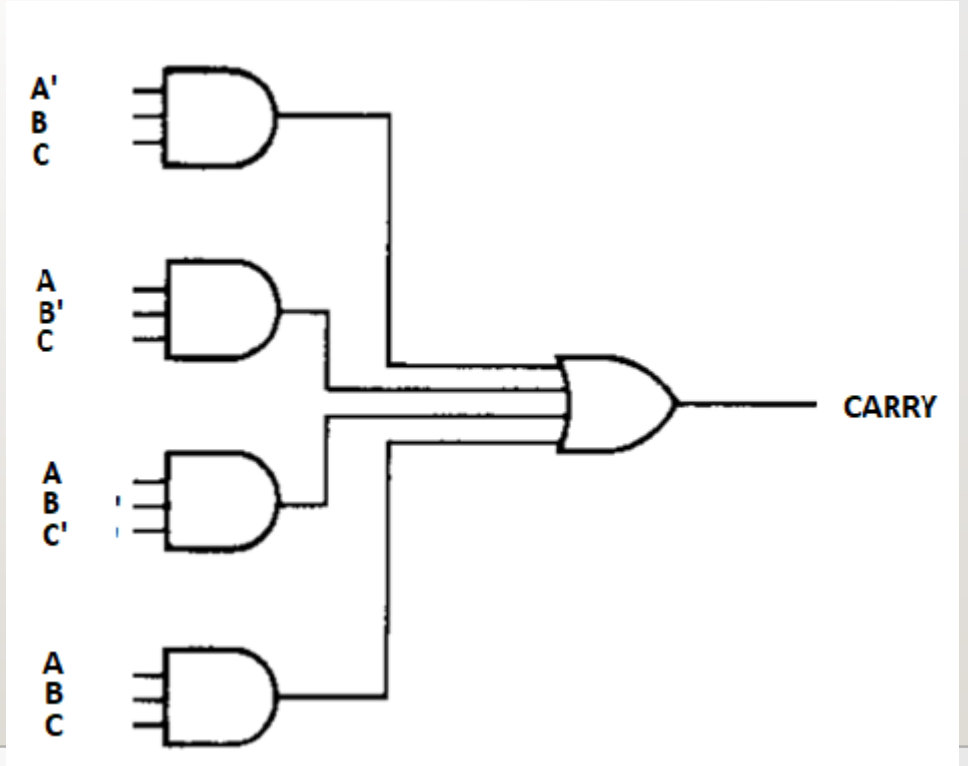
CARRY= $\sum m(3,5,6,7)$
= A'.B.C+A.B'.C+A.B.C'+A.B.C

REALIZATION OF FULL ADDER

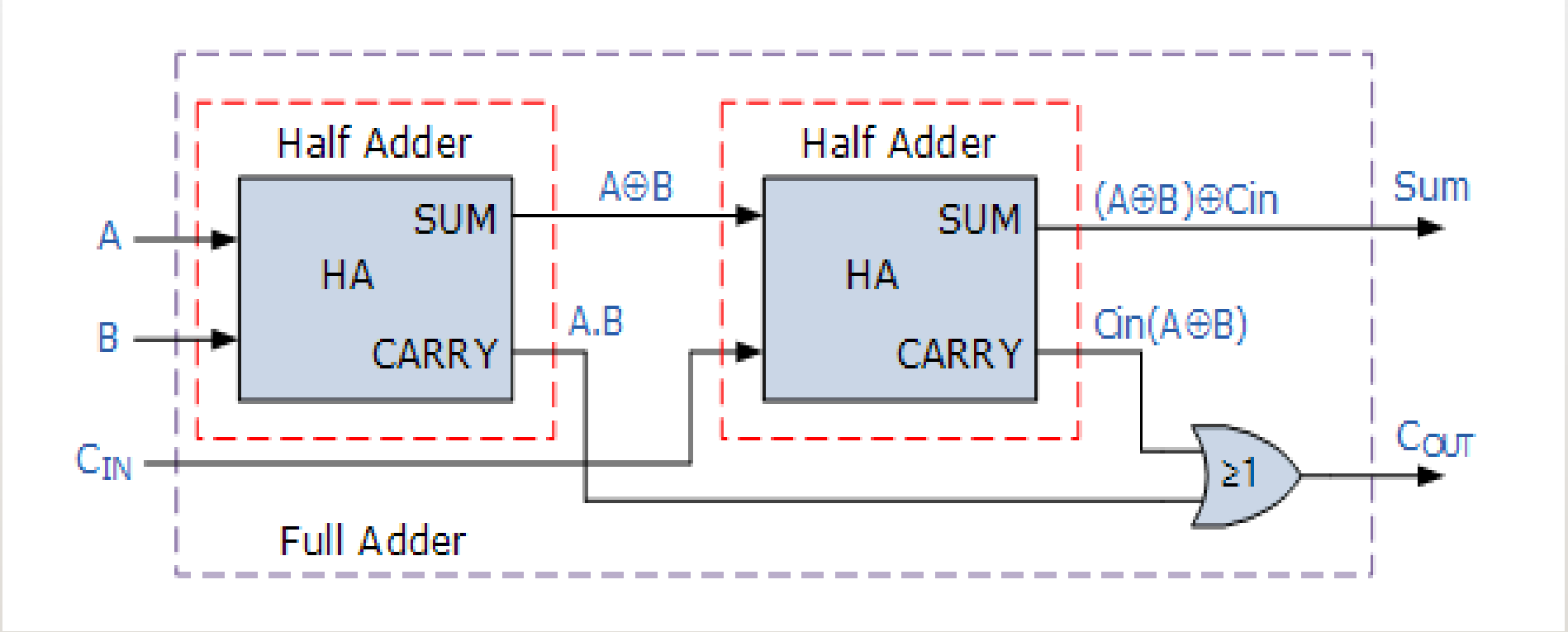
Logic Diagram:

- SUM = A'.B'.C+A'.B.C'+A.B'.C'+A.B.C
- CARRY = A'.B.C+A.B'.C+A.B.C'+A.B.C



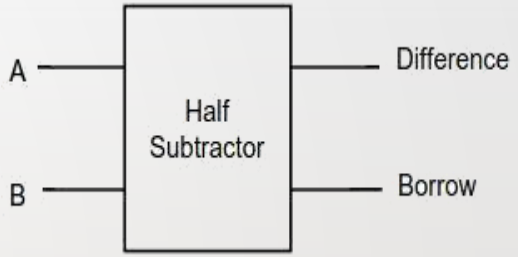


Full adder using two Half adders



Half Subtractor

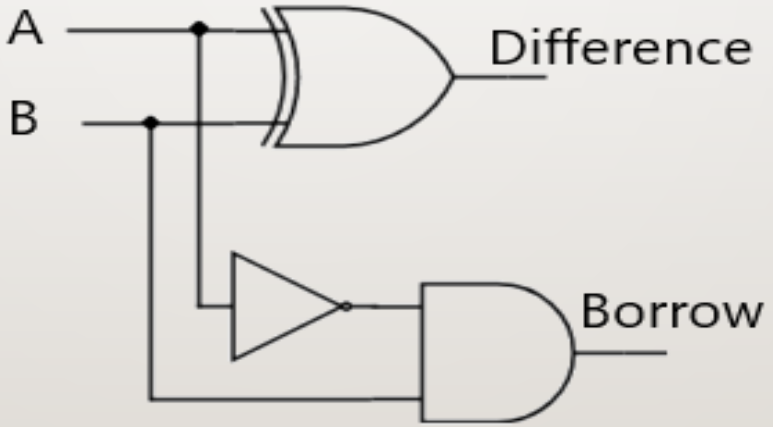
- The half-subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, A (minuend) and B (subtrahend) and two outputs Difference and Borrow.



Truth Table:

Inputs		Outputs	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Logic Diagram:



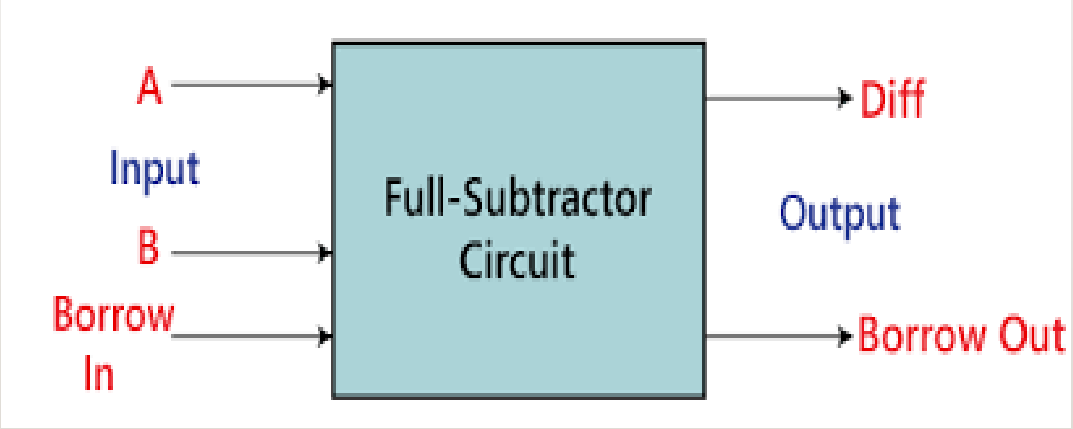
Output Expressions:

Difference = A ⊕ B

Borrow = A' B

FULL SUBTRACTOR

- A full subtractor is a combinational circuit that performs subtraction involving three bits, namely A (minuend), B (subtrahend), and Bin (borrow-in) .
- It accepts three inputs: A (minuend), B (subtrahend) and a Bin (borrow bit) and it produces two outputs: D (difference) and Bout (borrow out).

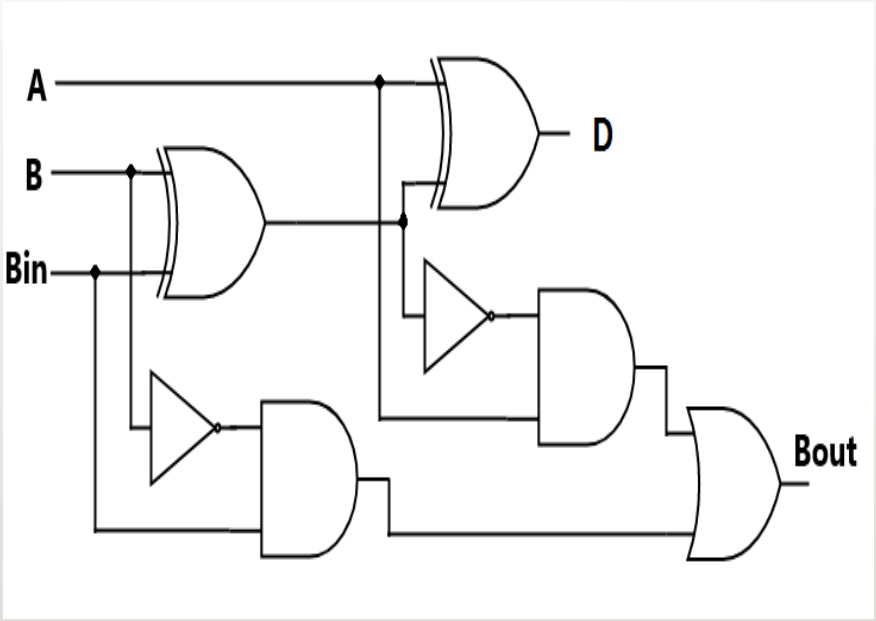


FULL SUBTRACTOR

Truth Table:

A	B	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Logic Diagram:



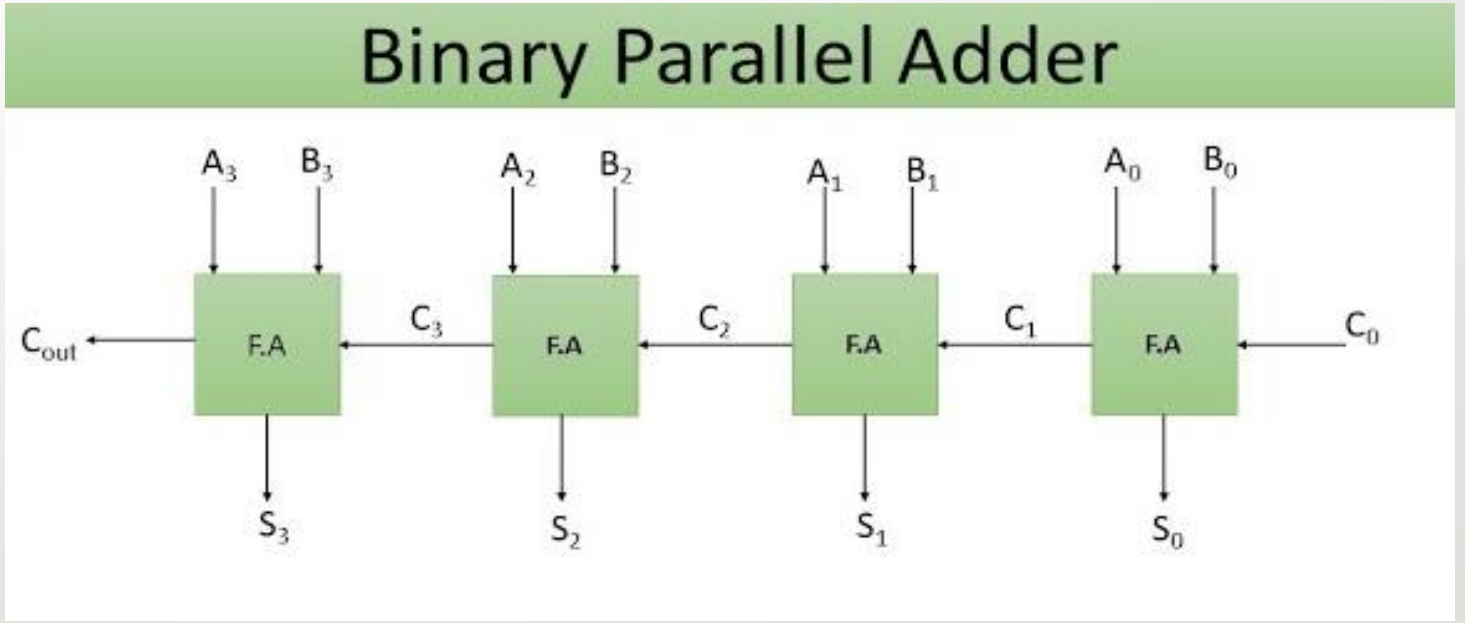
Output Expressions:

D = A ⊕ B ⊕ Bin

Bout = A' Bin + A' B + B Bin

PARALLEL ADDER

It consists of **full adders connected in a chain** where the output carry from each full adder is connected to the carry input of the next higher order full adder in the chain.



Advantages of PARALLEL ADDER

Advantages of parallel Adder/Subtractor –

- The parallel adder/subtractor performs the addition operation faster as compared to serial adder/subtractor.
- Time required for addition does not depend on the number of bits.
- The output is in parallel form i.e all the bits are added/subtracted at the same time.
- It is less costly.

ACTIVITIES/ CASE STUDIES/ IMPORTANT FACTS RELATED TO THE SESSION

ACTIVITIES

Half subtractor:

1. Deducing the truth table for Half subtractor
2. Derive the relation between inputs and outputs from truth table
3. Minimizing output Boolean expressions using optimization techniques
4. Draw logic diagram using logic gates

Full subtractor:

1. Deducing the truth table for Half subtractor
2. Derive the relation between inputs and outputs from truth table
3. Minimizing output Boolean expressions using optimization techniques
4. Draw logic diagram using logic gates

SUMMARY

Half Adder:

- **Purpose:** A half adder is a digital circuit that adds two binary digits (bits) and produces a sum bit (S) and a carry bit (C).
- **Inputs:** Takes two input bits, usually labeled as A and B.
- Outputs:
- **Sum (S):** Represents the addition result of A and B.
- **Carry (C):** Indicates if there is a carry-out from the addition.

Full Adder:

- **Purpose:** A full adder is an extension of the half adder that takes into account an additional carry input, allowing it to add three binary digits.
- **Inputs:** Takes three input bits - A, B, and an incoming carry bit (Cin).
- Outputs:
- **Sum (S):** Represents the addition result of A, B, and the incoming carry.
- **Carry-out (Cout):** Indicates if there is a carry-out from the addition, which can be used as the carry-in for the next stage.

SELF-ASSESSMENT QUESTIONS

1. In which operation carry is obtained?

(a) Subtraction

(b) Addition

(c) Multiplication

(d) Both addition and subtraction

2. The difference between half adder and full adder is.

(a) Half adder has two inputs while full adder has four inputs

(b) Half adder has one output while full adder has two outputs

(c) Half adder has two inputs while full adder has three inputs

(d) All of above

SELF-ASSESSMENT QUESTIONS

3. Half subtractor is used to perform subtraction of _____

(a) 2 bits

(b) 3 bits

(c) 4 bits

(d) 5 bits

4. How many outputs are required for the implementation of a subtractor?

(a) 1

(b) 3

(c) 2

(d) 4

TERMINAL QUESTIONS

Short answer questions:

1. Draw a half subtractor principle with input and output and truth table.
2. Design a full adder using two half adders.

Long answer questions:

1. Describe the full adder using a block diagram, list its truth table and output equations.
2. Describe the full subtractor using logic diagram, truth table and output equations.
3. Realize the full adder using two half adders.
4. Realize the output functional equations of Full adder using required logic gates.

REFERENCES FOR FURTHER LEARNING OF THE SESSION

Reference Books:

1. Computer System Architecture by M. Moris Mano
2. Fundamentals of Digital Logic with Verilog HDL by Stephen Brown and ZvonkoVranesic

Sites and Web links:

1. https://www.tutorialspoint.com/adders-and-subtractors-in-digital-electronics
2. https://technobyte.org/half-adder-full-adder-half-subtractor-full-subtractor/

THANK YOU

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Team – Digital Design & Computer Architecture