List of Important Questions - CO1

1. Formulate a comprehensive solution for realizing a full subtractor circuit using Decoder and OR gates.

2. Illustrate the construction of an Arithmetic Logic Unit (ALU) using an 8-to-1 Multiplexer.

3. Simplify the Boolean function F(a,b,c) = a'c + a'b + ab'c + bc) using a Karnaugh map (K-map).

4. Construct the full adder outputs using a Programmable Read-Only Memory (PROM) and an appropriate decoder.

5. Simplify the expression F(A,B,C) = A.B'.C + A' + A.C.B') using Boolean algebraic laws.

6. Explain DeMorgan's laws and their significance in logic simplifications.

7. Justify why universal logic gates (NAND and NOR) are named so.

8. Convert the decimal number ($278)_{10}$ into both binary and octal number systems.

9. Outline the truth tables for 2-input NAND and EX-NOR gates.

10. Highlight the key features of a Programmable Logic Array (PLA) and differentiate it from a Programmable Array Logic (PAL), with a supporting diagram.

11. Demonstrate the construction of a Full Adder circuit using an appropriate decoder and OR gates.

12. Realize the Boolean function (Y(a,b,c) = abc + b'c + ac') using logic gates.

13. Simplify the Boolean function (F(a,b,c) = abc + a'b'c + a'bc + a'b'c' + ab'c') using a 3-variable Karnaugh map (K-map).

14. Construct a full adder using two half adders.

15. Compare Complex Programmable Logic Devices (CPLDs) and Field-Programmable Gate Arrays (FPGAs), focusing on their distinctive characteristics.

16. Illustrate how a Programmable Logic Array (PLA) can be used to generate the output of a full adder circuit.

17. Demonstrate the working principle of a full subtractor, including its truth table, output equations, and logic diagram.

18. Provide a concise classification of Programmable Logic Devices (PLDs).

19. Convert the function (F(A,B,C) = AB’ + AC + BC) into canonical form.

20. Illustrate the block diagram of a 1:2 demultiplexer and provide its corresponding truth table.

21. Explain the operation of a half adder with its block diagram and truth table.

22. Explain the construction of Configurable Logic Blocks (CLBs) with the help of a diagram.

23. Implement the function $F(A,B,C) = \sum m(0,1,2,6,7)$ using a 4-to-1 Multiplexer (MUX) with "A" as the input line and "B" and "C" as selection lines.

24. Design the function $F = x_1\ x_3\ x_6' + x_1\ x_4\ x_5\ x_6' + x_2\ x_3'\ x_7 + x_2'\ x_4\ x_5'\ x_7$ using CPLD and flip-flops.

25. Simplify the Boolean function $F(w,x,y,z) = \sum m(0,1,8,9,10,11,12,13,14,15)$ using a Karnaugh map (K-map).

26. Develop the design and functionality of an 8-to-3 encoder, including input & output lines and its truth table.

27. Simplify the Boolean function $F(A, B, C, D) = \sum m(0,1,4,5,6,7,10,13) + d(2,3)$ using a Karnaugh map (K-map).