Improving the phase delay capacitive interface circuit technique using MOSFET switches

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Improving the Phase Delay Capacitive Interface Circuit Technique using MOSFET Switches

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Abstract. Measuring the phase delay of an RC network with a known resistance and an unknown capacitance is a simple technique to determine the value of capacitance. In this technique, the state of an input square wave signal is buffered by CMOS inverters and delayed by an RC network which yields a pulse width modulated (PWM) signal according to the phase delay at the output. The duty cycle of the PWM signal is proportional to the unknown capacitance when the resistance is fixed. However, the response of this method becomes severely nonlinear if the phase delay is larger than approximately 45° due to incomplete charging and discharging processes of the unknown capacitor. A novel MOSFET interface circuit with a PMOS FET to charge the unknown capacitor and an NMOS FET to discharge it during each measurement cycle is presented. This method, which expands the range of linear operation, is demonstrated in simulation and experimentally validated using a fringing field capacitive sensor to measure the mass of added water. The novel circuit expands the linear operation to a phase delay of 140.04°, over which the R^2 value achieves 0.9989.

Keywords: capacitance measurement, sensor interface circuit, RC phase delay

1. Introduction

Capacitance measurement is necessary for successfully interfacing to a large variety of sensors, including many types of accelerometers (Jono et al., 1995), gyroscopes (Xie and Fedder, 2002), pressure sensors (Ko and Wang, 1999), stress/strain sensors (Shkel and Ferrier, 2003), humidity sensors (Aziz et al., 2011; Weremczuk et al., 2011), soil water content sensors (Dean et al., 2012), and tomography sensors (Yang and Peng, 2002; Yang, 2010), etc. It is considerably more complicated to measure an unknown capacitance than an unknown resistance, and researchers have therefore developed numerous techniques to interface to capacitive sensors. Examples of these techniques include, relative phase delay (Dean et al., 2009), capacitively controlled

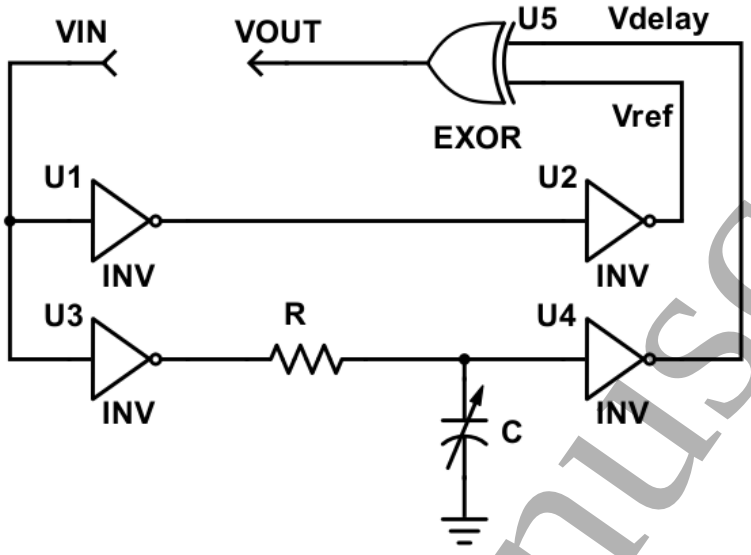

Figure 1: Schematic diagram of the basic phase delay technique.

oscillators (Gasulla et al., 2005), RC discharge (Hagiwara and Saegusa, 1983), phase-locked loops (PLLs) (Sell et al., 2011), frequency-locked loops (FLLs) (Dean and Rane, 2013), capacitive ratio current modulation (Sheu et al., 2012), chopper modulation (Nizza et al., 2013), delta-sigma modulation (Jung et al., 2017), CMOS current-mode interface (Scotti et al., 2014), and mixed-signal interface (Kraver et al., 2001), etc.

The relative phase delay technique (Dean et al., 2009) is a straight forward technique for measuring an unknown capacitance. It is based on delaying the state change of a square wave through a passive RC low-pass filter where R is known and C is the unknown capacitance. The circuit's output signal is a pulse width modulated (PWM) signal with the pulse width proportional to the unknown capacitance. This technique's usefulness is limited to a small range due to severe nonlinear distortion outside of this range. However, this technique can be modified to significantly increase the linear operating range. The remainder of this manuscript presents this technique.

In the relative phase delay technique (Dean et al., 2009) the unknown capacitance, C, is connected with a known resistance, R, to form a single pole passive low-pass filter network. The filter is buffered on both sides by CMOS inverters. The purpose of this buffered filter network is to delay an input square wave, V_{IN}, of known fundamental frequency. If the fundamental frequency of V_{IN} is sufficiently low such that C almost fully charges or discharges between state changes, then the RC subcircuit will delay the square wave by τ which is given by (1):

$$\tau = 0.693R(C + C_{INV}) \tag{1}$$

where C_{INV} represents the capacitance looking into the output CMOS inverter. The propagation delay through the buffering inverters is not considered, because a reference

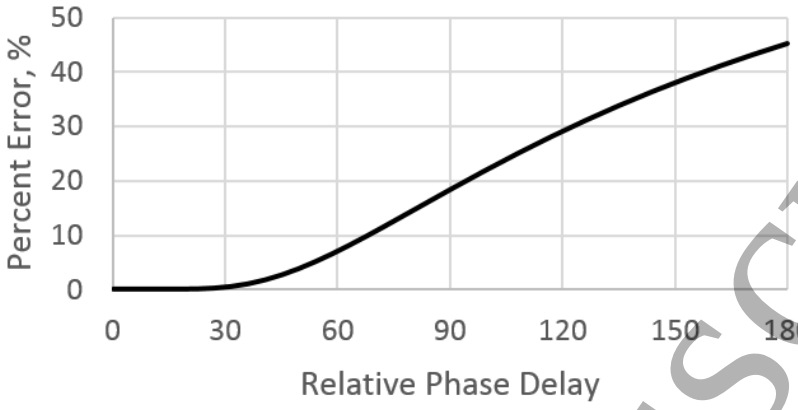

Figure 2: A plot of percent error as a function of relative phase delay between V_{ref} and V_{delay}.

delayed square wave is produced by feeding V_{IN} through two additional CMOS inverters, as shown in figure 1. The operation of this circuit assumes that all four CMOS inverters are identical and possess a trip voltage equal to one half of the power supply voltage, V_{DD}. Also, the input square wave fluctuates between 0 V (logic level 0) and V_{DD} (logic level 1).

V_{ref} is the reference square wave and V_{delay} is the square wave delayed due to the unknown capacitance. The relative delay between V_{ref} and V_{delay} is measured using an Exclusive OR (XOR) logic gate. XOR gates are commonly used as phase detectors in PLLs (Van Nieuwenhuyse et al., 2014) and possess an 180º monotonic operating range between the two input square waves. To minimize jitter, the XOR phase detector operates best around a 90º phase difference between the two input square waves (Maneatis, 1996). The XOR gate outputs a PWM signal (V_{OUT} in figure 1) with the duty cycle proportional to the unknown capacitance. A DC signal proportional to C can be obtained by low pass filtering V_{OUT}.

When the frequency of V_{IN} is sufficiently low such that C almost fully charges or discharges between state changes, the duty cycle of V_{OUT} is approximately linearly proportional to C. As the fundamental frequency of V_{IN} is increased, the amount of duty cycle change over the full range of C also increases. However, the approximation that C fully charges or discharges between state changes becomes less and less valid. This results in the duty cycle of V_{OUT} being a nonlinear function of C. To analyze the cause of the nonlinearity, let V_C represent the magnitude of the nonzero voltage remaining across C as V_{IN} changes states. As a consequence, the phase delay between V_{ref} and V_{delay} becomes

$$\tau = -R(C + C_{INV}) \ln\left(\frac{0.5V_{DD}}{V_{DD} - V_C}\right) \tag{2}$$

and the relative phase delay is no longer a linear function of C since V_C increases as C increases. The previously published work determined that in order to limit the nonlinearity to 2.6%, the maximum phase delay could not exceed 45º, which is 25%

of each half V_{ref} cycle (Dean et al., 2009). This is illustrated in figure 2 in a plot of percent error, as a function of relative phase delay between V_{ref} and V_{delay}. Observe that the percent error is very low, below approximately 30°. Recalling that the XOR phase detector has a monotonic and therefore useful range of 180°, the nonlinearity in unknown capacitance measurement limits the useful range to only 1/4 of the possible phase detector range. This is equivalent to a maximum duty cycle change of only approximately 25%.

A previously published technique proposed to expand the range of linear operation by using an analog switch to lower the resistance, R, as soon as V_C reached the trip voltage of the inverter (Meng and Dean, 2016). Therefore, by temporarily reducing the time constant in the charging and discharging circuit, the otherwise error inducing charge remaining on C is quickly discharged, without adversely affecting the sensing function of the interface circuit. To achieve this, the previous design used two dissimilar value, discrete resistors for R, and a discrete bidirectional analog switch in parallel with the larger resistor, so that it could be shorted to significantly reduce the RC time constant after the state change occurred. In this paper, an improved circuit design is presented, which further expands the linear operating range to 140.04°. This new design uses a single resistor for R, and two discrete MOSFETs instead of a complex analog switch IC to pull C up to V_{DD} or down to ground after a state change has occurred. As a result, the circuit operates over a wider range of input frequencies, and also achieves a more symmetric PWM signal by using two control loops that have approximately identical reaction times.

2. Theoretical Development

2.1. Circuit Design

As previously discussed, the linear relationship between the PWM signal duty cycle and the capacitance C has a very small range limited by C not being fully charged and discharged each cycle. Therefore, in order to expand the range of linear operation, the charging and discharging processes needs to be accelerated as soon as V_C reaches the trip voltage.

An improved method can be realized by adding a p-channel MOSFET (PMOS) as a switch to pull the V_C node up to V_{DD} (5 V typically) and an n-channel MOSFET (NMOS) as a switch to pull it down to ground after the inverter trip voltage has been reached, as shown in the schematic diagram in figure 3. Specifically, when V_{ref} (approximately the same as V_{IN} due to the low propagation delay of the inverters) and V_{delay} are both in the low state, these two signals are fed into a NOR/inverter gate combination to set the gate-source voltage, V_{GS}, of the PMOS to be low, thus turning it on and quickly pulling the V_C node up to 5 V. Likewise, when V_{ref} and V_{delay} are both in the high state, these two signals are fed into a NAND/inverter combination to set the gate-source voltage of the NMOS to be high, thus switching on the NMOS to

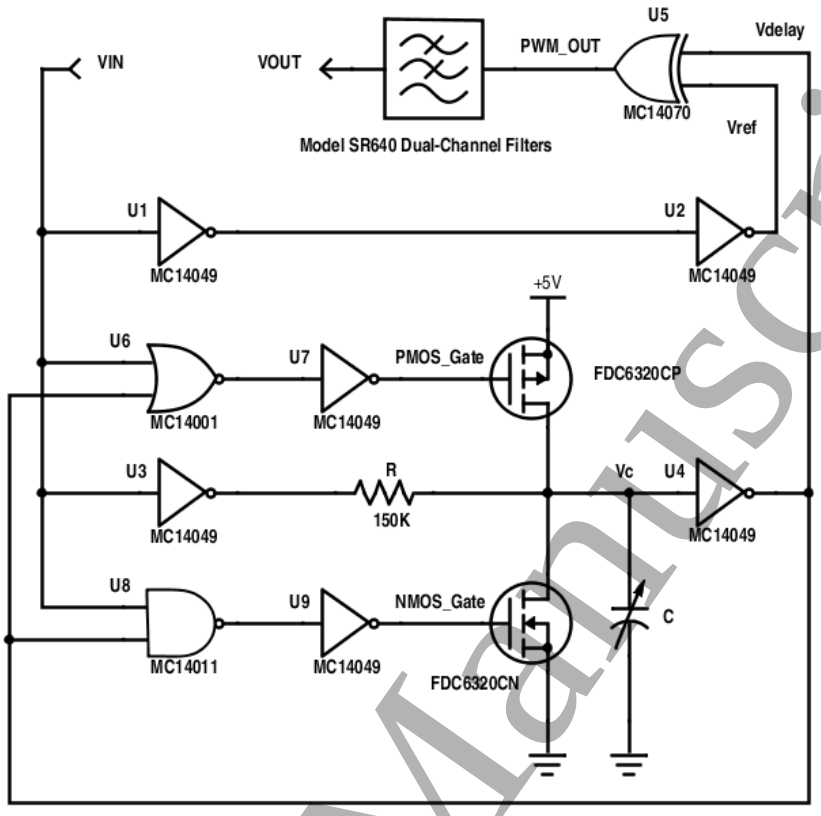

Figure 3: A schematic diagram of the MOSFET switching technique.

quickly pull the V_C node down to 0 V.

It is important to notice that, according to the logic function of the NOR and NAND gates, at the same time when the PMOS is switched on, the NMOS is off, and vice-versa. And both transistors are switched off when C is being charged or discharged to the trip voltage of 2.5 V. This leaves the effective charging and discharging period unaffected, and thus the linear relationship between the PWM duty cycle and sensed capacitance undisturbed.

Consequently, the maximum phase delay for a linear operation is able to reach beyond 45° or 25% of each half V_{ref} cycle. Although the specific increase in the maximum phase delay also depends on the range of the measured variable capacitance and the frequency of the input square wave, it can theoretically be very close to the maximum useful range of 180° when needed. In practice, however, due to increased phase jitter near the 180° limit, avoiding operation close to this limit may make the measurement more accurate.

The output PWM signal can be low-pass filtered to convert the output to a DC voltage proportional to the sensor capacitance, if desired. As shown in figure 3, a programmable model SR640 dual-channel low-pass filter was used to convert the PWM signal to a DC voltage for measurement purposes.

Table 1: Primary parameters of the selected MOSFETs.

Type	Parameter	Conditions	Min	Typ	Max	Units
p-channel	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250 μA	-0.65	-1	-1.5	V
	Static Drain-Source On-Resistance	V_{GS}= -2.7V, I_D=-0.05A		10.6	13	Ω
	Output Capacitance	V_{DS}=-5V, V_{GS}=0V, f=1MHz		9		pF
n-channel	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	0.65	0.85	1.5	V
	Static Drain-Source On-Resistance	V_{GS}=2.7V, I_D=0.2A		3.8	5	Ω
	Output Capacitance	V_{DS}=5V, V_{GS}=0V, f=1MHz		7.8		pF

2.2. MOSFETs Selection

Trade-offs need to be made when selecting proper MOSFETs to yield the most accurate results for the application of small capacitance measurement, which is often below 100 pF. The MOSFETs in use are the PMOS and NMOS on a dual p and n channel MOSFET model of FDC6320C by ON Semiconductor (*FDC6320C Dual N and P Channel Digital FET.*, 1997). The primary parameters of the two MOSFETs are listed in table 1. The transistors have low dynamic output capacitances of 9 pF for the p-channel FET at V_{DS}=-5 V and 7.8 pF for the n-channel FET at V_{DS}=5 V, along with low drain-source on-resistances of 10.6 Ω for the p-channel FET at V_{GS}=-2.7 V and 3.8 Ω for the n-channel FET at V_{GS}=2.7 V, which suits this application well. Specifically, using the low on-resistances to pull the V_C up to V_{DD} or down to ground, instead of switching to a smaller R of 10 $k\Omega$ as used in the previous work (Meng and Dean, 2016), enables a relatively high operating frequency of the entire circuit.

Observe that smaller on-resistance usually means larger gate capacitance, while on the other hand, larger on-resistance usually means smaller gate capacitance. This is due to device fabrication structures and, generally speaking, the resistance decreases as the area of the channel increases; however, the gate capacitance increases. In this application, it is easy to make a choice of selection based on the gate capacitance since

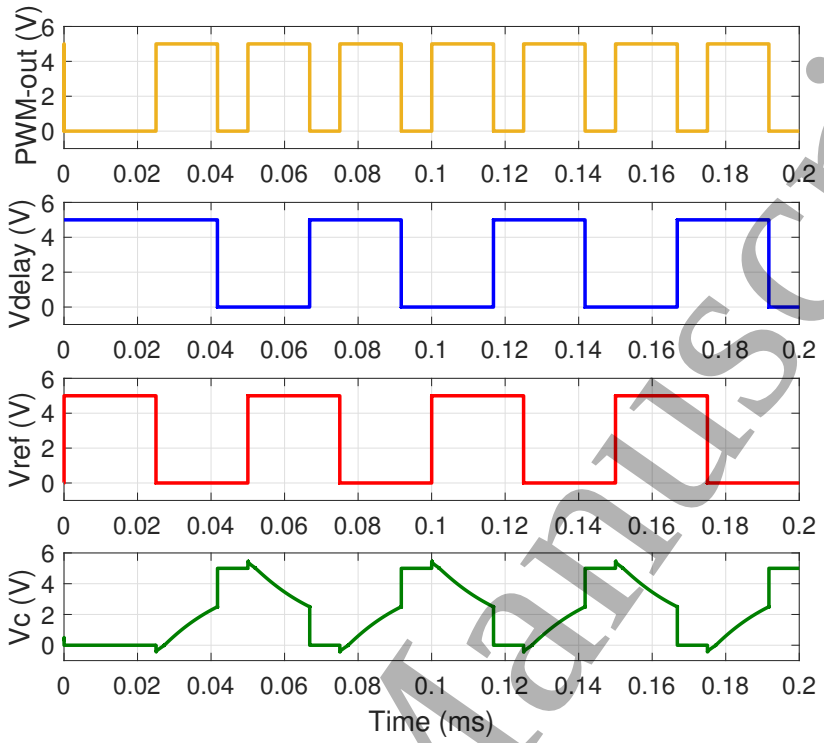

Figure 4: Simulation results of the MOSFET switching circuit with $C = 61.27$ pF at the frequency of 20 kHz.

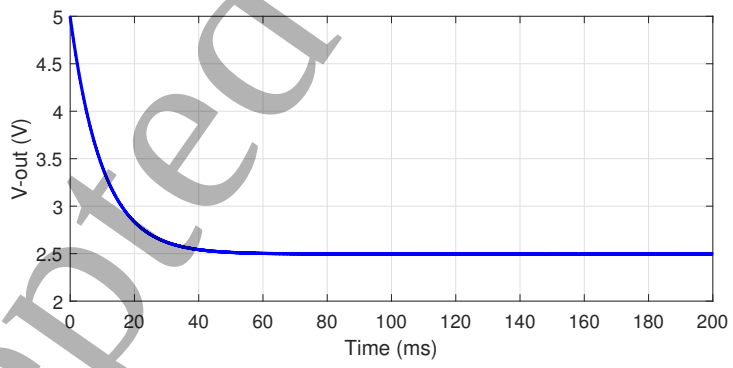

Figure 5: An example simulation plot of the PWM signal converted to a DC voltage with $C = 61.27$ pF at the frequency of 20 kHz.

the system is much more sensitive to the gate capacitance than to the on-resistance.

3. Simulation

Figure 4 depicts the LTSpice simulation results of the novel MOSFET interface circuit with an R of 150 kΩ as shown in figure 3, and a sensor capacitance of 61.27 pF with the input square wave frequency of 20 kHz, as an example. Spice models of

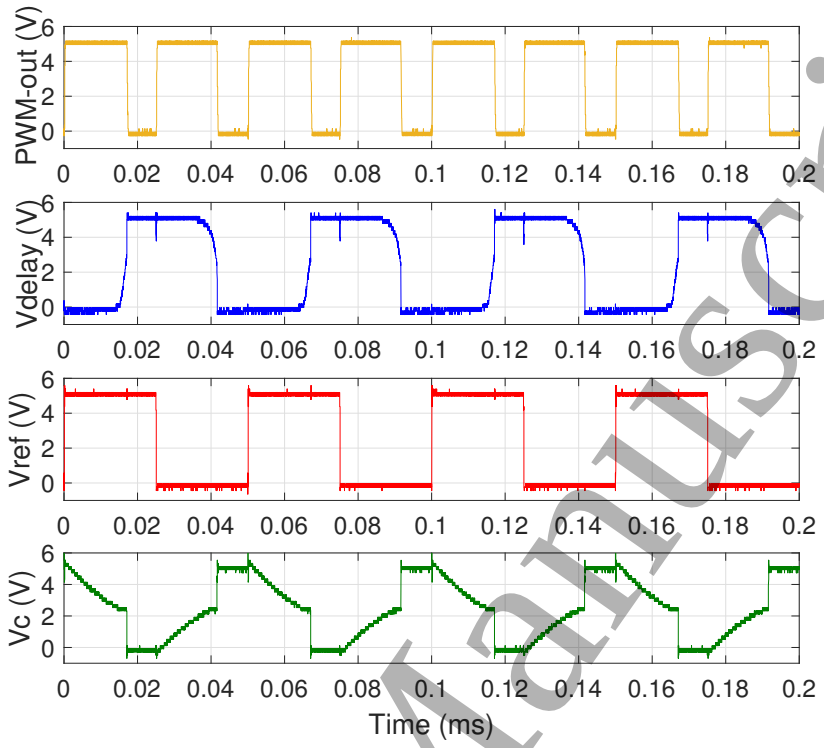

Figure 6: Plots of oscilloscope records of the tested MOSFET switching circuit with C = 61.27 pF at the frequency of 20 kHz.

FDC6320CP, FDC6320CN, MC14049, MC14001, MC14011, MC14070, correspondingly to the p-channel MOSFET, the n-channel MOSFET, the inverters/NOT gates, the NOR gate, the NAND gate and the XOR gate were used (figure 3). Electronic parts of these models were used in the prototype circuit in the next section as well.

The output of the LTSpice simulation with a C of 61.27 pF and an input frequency of 20 kHz is presented in figure 4. The top waveform is the output PWM signal. The upper middle and lower middle waveforms are the output voltages from the phase delay subcircuits, V_{delay} and V_{ref}, respectively. The phase delay caused by the RC network and the function of the XOR gate are obviously reflected in these first three plots. The bottom waveform is the voltage across the sensor capacitance, V_C, from which the acceleration of charging and discharging processes are clearly observable. Notice that V_C has sharp fully charging and fully discharging characteristics every time it reaches the trip voltage, which leaves great potential for expanding the effective phase delay toward the approximately 180° linear range instead of only about 25% of it. Figure 5 shows the DC voltage output, V_{OUT}, converted from the PWM signal by the low-pass filter. According to the simulation results, the MOSFET switch technique improved the RC phase delay interface circuit as designed.

4. Experimental Verification

To evaluate the performance of the proposed interface circuit experimentally, a prototype of the 5-V MOSFET interface circuit was built on a breadboard and a capacitive sensor of known characteristics was integrated into the prototype circuit. An Agilent E3631A DC power supply was used to provide the 5 V DC voltage for the entire MOSFET interface circuit. An Agilent 33220A 20 MHz function generator generated square waves with a 5 V amplitude and 50% duty cycle at selected frequencies for the V_{IN} signal. An Agilent MSO-X 2004A 70-MHz 4-channel oscilloscope was used to capture the waveforms at PWM-out (top waveform in figure 6), V_{delay} (upper middle waveform) and V_{ref} (lower middle waveform). The voltage across the sensor capacitance, V_C, is represented by the bottom waveform in figure 6, from which the charging and discharging procedures are shown in detail. Notice that the V_C is pulled up to 5 V or down to 0 V almost immediately upon reaching the trip voltage of 2.5 V. The plots of simulated signals in figure 4 and experimental signals in figure 6 show good agreement. The PWM signal was fed into the 8-pole programmable dual channel filter of the Stanford Research Systems model SR640 which was used as a low-pass filter to convert the PWM to a DC voltage. Also, a GW Instek LCR-821 LCR meter was used to measure the capacitances of the capacitive sensor to obtain the standard values for the testing.

4.1. Fringing Field Capacitive Sensor

A fringing field capacitive sensor (Yunus and Mukhopadhyay, 2011) (Mizuguchi et al., 2015) was used as the C in figure 3 to validate the circuit design. This sensor was designed and implemented in a printed circuit board (PCB). The output capacitance of this type of sensor was previously demonstrated to increase linearly in proportion to the mass of a drop of water on the active sensing area (Dean et al., 2012). The sensor was selected to verify this design of interface circuit due to its large range of variable capacitance. This kind of capacitive sensor was fabricated with two planar interdigitated electrodes on the top layer of the Cu foil on the PCB and covered by a solid layer of solder mask (figure 7). The bottom layer of the PCB, directly behind the electrode array, had an electrically floating Cu pad covered by solder mask as well. The sensor PCB had the dimensions of 76.5 mm by 29.8 mm in size and the electrode array was 23.0 mm by 21.2 mm. Each of the two electrodes on the top had 35 interdigitated teeth (i.e. 35 electrode pairs) and each of the teeth was overlapped to adjacent teeth by a length of 22.4 mm. The gap between two opposing teeth was 152.4 μm. The Cu pad on the back had the same dimensions and planar position with the electrode array.

In the tests, an eye dropper was used to add drops of distilled water to the surface of the solder mask over the electrode array within the effective sensing area, starting from the center area. As water was added, a single large drop was maintained due to the nearly hydrophobic characteristic of the solder mask. The water interacted with the fringing fields in the volume above the PCB surface. Since the dielectric constant of water is approximately 80 times that of air, the capacitance between the electrodes

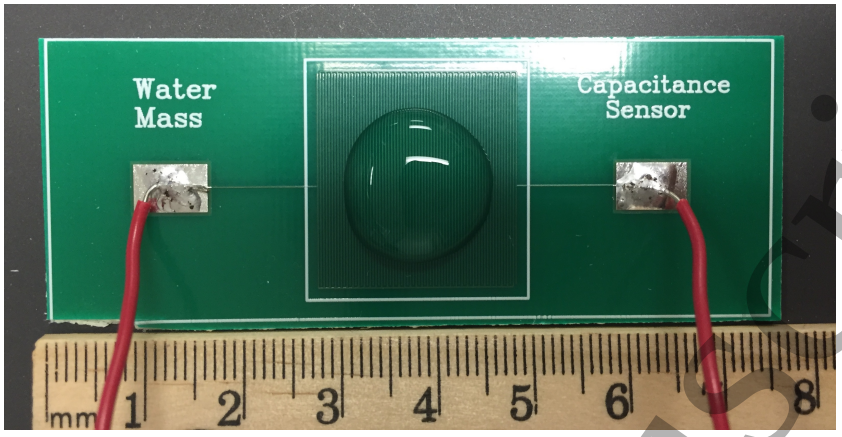

Figure 7: A photograph of 523 mg of distilled water on a fringing field capacitive sensor.

was significantly increased by the beaded up water. For instance, the capacitance of the sensor was 61.27 pF in air and 300 pF when submerged in distilled water. The area on the sensing surface covered by water increased with each additional drop of water being added. The capacitance tends to be linearly proportional with the mass of the drop of water (R^2=0.9982 as reported in (Dean et al., 2012) and R^2=0.99 in (Mizuguchi et al., 2015)). Figure 7 shows a photograph of the sensor with a 523 mg drop of distilled water on the sensing area. The sensor bearing the composite water drop was located on a balanced electronic scale so that the mass of water was weighed after each new drop was added.

4.2. Testing and Results

Testing was performed at room temperature. Data, including the mass of the composite water drop, the sensor capacitance measured by the LCR meter, and the output DC voltage, were collected every time a new drop of water was added. A switch was added to the circuit to disable the function of the MOSFET interface circuit to convert it back to the traditional RC phase delay circuit so that data of V_{OUT} from both circuits could be recorded and compared with the same water drop. Two frequencies of 12 kHz and 20 kHz for the input square wave were used in the testing. The input frequency of 12 kHz was chosen due to the fact that the traditional RC phase delay technique starts to loose linearity at this frequency while the new design still offers a linear response. 20 kHz was found as the maximum input frequency before the new design loses linearity and the composite water drop reaches the edge of the sensing area at the same time. Thus the lower bound and the higher bound of the input frequency range can be much lower than 12 kHz and higher than 20 kHz respectively, depending on the application i.e. the combination of effective capacitance and resistance.

In this testing, specifically, 18 drops of distilled water were added sequentially within the sensing area on the sensor's surface until the edge of the water bead reached close to the limit of the active area. Along with the reference data collected without water

Table 2: Averages of the recorded data with maximum percentage errors at the input frequency of 12 kHz at 23°C

Number of Drop	Mass of DI water (mg)	Sensor Cap. (pF)	DC Voltage (V)		Time Delay (μs)	
			MOSFET Interface Circuit	Traditional RC Circuit	MOSFET Interface Circuit	Traditional RC Circuit
1	0	63.08	1.32	1.32	15.7	11.5
2	38	70.42	1.39	1.38	16.4	12.0
3	72	75.33	1.43	1.41	16.9	12.3
4	109	80.48	1.48	1.44	17.5	12.6
5	140	84.70	1.52	1.45	18.0	12.8
6	174	88.38	1.55	1.46	18.4	13.0
7	211	93.27	1.59	1.48	18.9	13.2
8	244	96.96	1.62	1.49	19.2	13.3
9	274	101.30	1.65	1.50	19.6	13.5
10	308	106.00	1.71	1.51	20.2	13.7
11	341	110.05	1.73	1.52	20.6	13.9
12	376	114.29	1.78	1.54	21.2	14.1
13	410	119.67	1.82	1.55	21.6	14.3
14	454	124.89	1.87	1.57	22.2	14.5
15	492	131.24	1.92	1.58	22.8	14.6
16	523	135.22	1.96	1.59	23.2	14.7
17	557	139.97	2.00	1.61	23.6	14.8
18	593	143.60	2.04	1.62	24.1	15.0
19	629	147.51	2.07	1.63	24.5	15.1
Maximum Error (%)	16	7.78	1.52	2.27	2.9	1.7

on the sensor, 19 output DC voltage levels were recorded from the MOSFET interface circuit and for the traditional RC phase delay circuit. Such testing was repeated for five times for each frequency, resulting in ten sets of data to study the uncertainty and repeatability. Based on the five sets of data acquired under the input frequency of 12 kHz, averaged values including mass of DI water, sensor capacitance, output DC voltages and time delays from the new design and traditional RC circuit are listed in table 2. The maximum percent errors for each value were also listed. Each value was tested for five times and all the percent errors were smaller than 10% except for the mass, which indicates a good repeatability of the testing. The 16% error of the mass resulted from the difficulty in having evenly distributed amounts of water for each droplet. However, since the linear relationship was studied between the output versus mass/capacitance instead of the output versus the number of drops, reasonable variations between drop

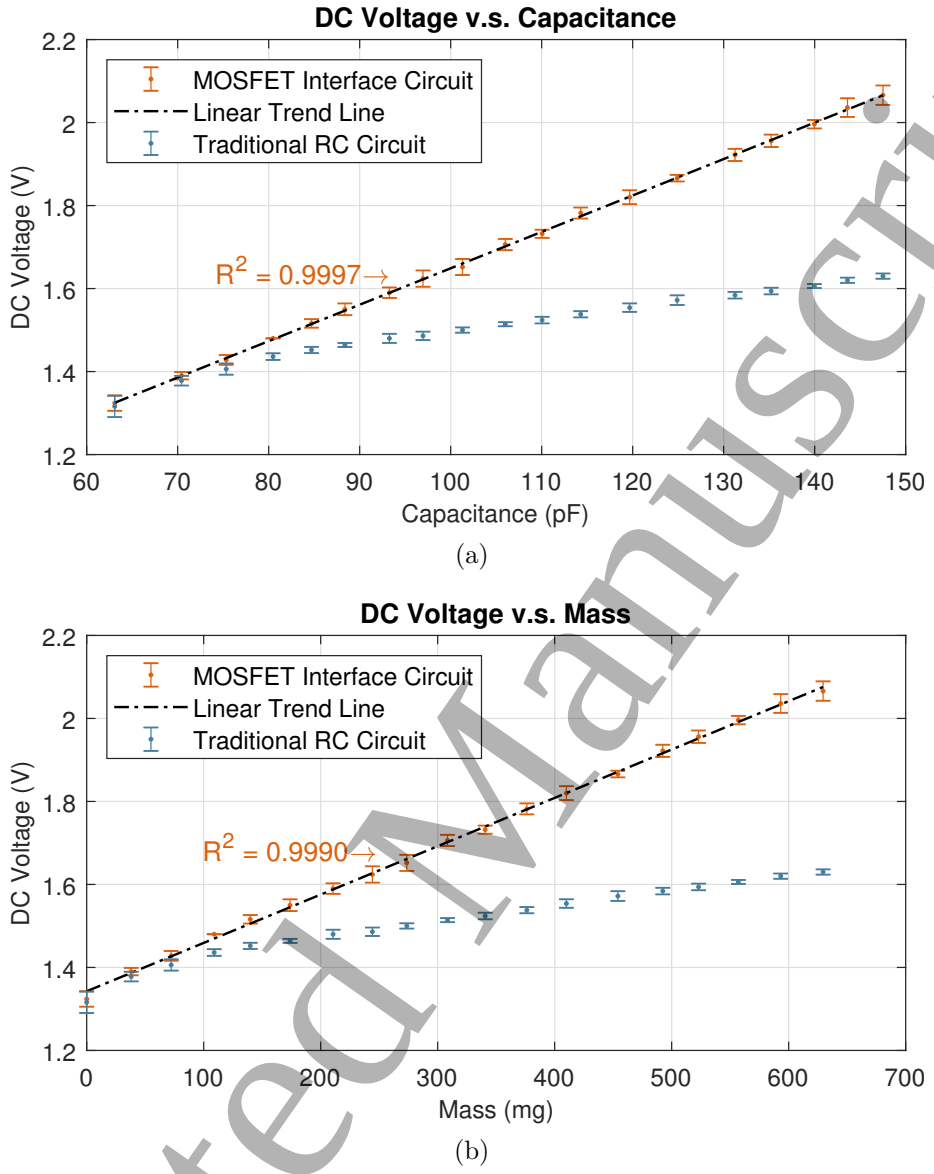

Figure 8: Plots of average output DC voltage versus measured (a) average capacitance and (b) average mass of water with error bars of standard deviations at the frequency of 12 kHz.

sizes would not have a significant affect on the results.

The relationship between the averaged output DC voltage versus the averaged sensor capacitance is presented in figure 8a, in which the orange dots with error bars represent the MOSFET interface circuit and the blue dots with error bars represent the traditional RC circuit. A least-squares fit was used to study how the data fitted the linear regression models (Myers and Myers, 1990). Statistical model fitting coefficients, such as coefficients of determination (R^2's) and probability values (p-values), were calculated to evaluate the fit (Glantz and Slinker, 1990). A linear trend dash-dotted line in black shows a nearly linear relationship with an R^2 value of 0.9997. Along with a p-value

Table 3: Linear regression model fit coefficients.

Frequency	Test Number	DC Voltage v.s. Capacitance		DC Voltage v.s. Mass	
		R^2	p-value	R^2	p-value
12 kHz	1	0.9989	1.03E-21	0.9941	8.12E-29
	2	0.9991	5.74E-25	0.9958	6.32E-30
	3	0.9989	2.67E-26	0.9956	5.42E-30
	4	0.9990	5.21E-25	0.9976	2.88E-32
	5	0.9994	1.05E-28	0.9984	8.72E-34
	Fit of the Averages	0.9997	4.42E-30	0.9990	3.08E-35
20 kHz	1	0.9989	2.49E-23	0.9920	2.26E-28
	2	0.9990	3.66E-25	0.9963	6.00E-31
	3	0.9991	2.30E-25	0.9831	3.20E-25
	4	0.9991	2.43E-25	0.9952	3.20E-30
	5	0.9993	2.77E-26	0.9948	5.90E-30
	Fit of the Averages	0.9997	4.82E-29	0.9956	2.13E-30

of 4.42×10^{-30} ($\ll 0.05$, listed in table 3) under the number of observations of 19 and degree of freedom of 17, the result is considered as statistically significant since the null hypothesis is rejected (Fisz, 2018). Therefore, a conclusion can be made that there is a linear association between the averaged output DC voltage and the averaged capacitance. Observe, however, the trend of the traditional circuit starts to deviate from the linear trend and rolls off when the capacitance increases to a point near 75 pF. As discussed previously, this is due to the sensor capacitor not being nearly fully charged and discharged when the RC phase delay increases larger than 45° or 25% of each half cycle.

The same characteristics can be observed in figure 8b, where the averaged DC voltage is plotted versus the averaged mass of the water accumulated on the effective sensing area. The linearity for the MOSFET interface circuit (R^2 is 0.9990), however, is not quite as good as the linearity between the averaged DC voltage and the averaged capacitance. This is a result of the sensing mechanism employed by the sensor, not the interface circuit. Yet the improvement of the novel MOSFET interface circuit compared with the traditional circuit is still clear.

As expected, the nonlinearity of the traditional circuit was more severe when the phase delay increased beyond 45° or 25% of each half cycle. It is interesting to explore the limitation of the MOSFET interface circuit by increasing the input frequency. The

Table 4: Averages of the recorded data with standard deviations at the input frequency of 20 kHz at 23°C

Number of Drop	Mass of DI water (mg)	Sensor Cap. (pF)	DC Voltage (V)		Time Delay (μs)	
			MOSFET Interface Circuit	Traditional RC Circuit	MOSFET Interface Circuit	Traditional RC Circuit
1	0	60.59	2.50	1.83	15.5	9.4
2	48	71.26	2.69	1.88	16.5	9.5
3	89	76.52	2.79	1.90	17.0	9.6
4	132	81.49	2.87	1.92	17.5	9.8
5	163	85.27	2.94	1.94	17.9	9.8
6	186	88.11	3.00	1.95	18.2	9.9
7	219	91.72	3.08	1.97	18.6	10.0
8	248	95.39	3.13	1.99	18.9	10.0
9	283	98.85	3.20	2.00	19.2	10.1
10	315	101.70	3.26	2.02	19.7	10.2
11	356	106.10	3.33	2.04	20.0	10.2
12	392	110.38	3.42	2.05	20.5	10.2
13	431	114.87	3.50	2.07	20.8	10.3
14	467	119.02	3.56	2.08	21.2	10.3
15	498	123.03	3.63	2.09	21.5	10.4
16	525	126.14	3.68	2.10	21.8	10.4
17	557	129.55	3.74	2.11	22.1	10.5
18	590	132.63	3.80	2.12	22.4	10.6
19	619	135.09	3.85	2.13	22.6	10.6
Maximum Error (%)	17	6.30	2.40	1.98	1.3	1.1

maximum input frequency turned out to be 20 kHz, from which the averaged data were recorded in table 4 from both circuits being tested and plotted in figure 9. In those plots, the traditional circuit failed to give a linear response from the beginning, while the MOSFET interface circuit still worked as designed.

In the fitted models of averaged data, instead of being limited to 45° or 25% of each half cycle, the linear range of the new phase delay circuit was expanded to 138.60° or 77.0% of each half cycle. In the data set with the lowest R^2 of 0.9989, given by test number 1 (table 3), the linear range achieved 140.04° or 77.8% of each half cycle, which is also greater than that of 133.56° or 74.2% of each half cycle achieved by (Meng and Dean, 2016). Again, since the maximum phase delay also depends on the range of the measured variable capacitance and the frequency of the input square wave, the maximum phase delay can potentially be further extended in other applications. For instance, if

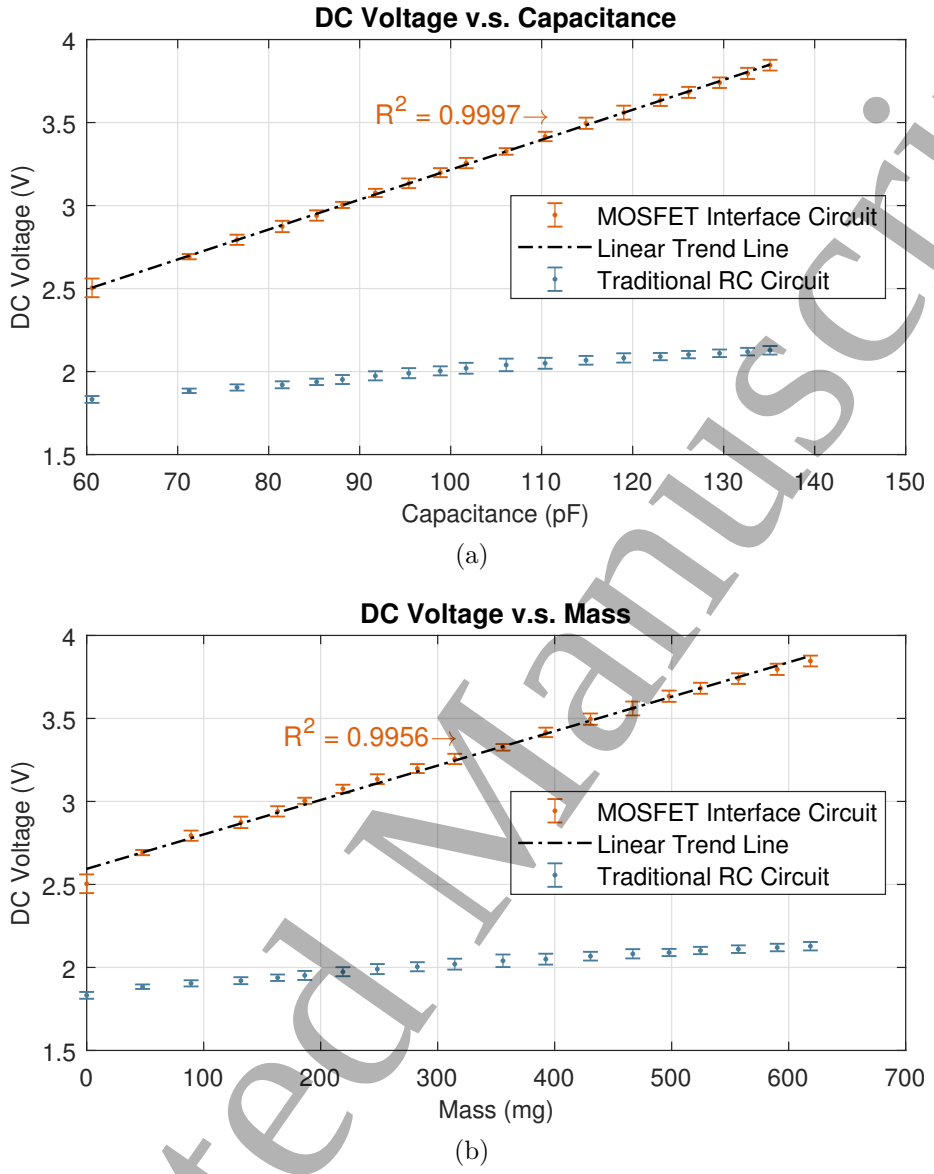

Figure 9: Plots of average output DC voltage versus measured (a) average capacitance and (b) average mass of water with error bars of standard deviations at the frequency of 20 kHz.

the sensing area of the capacitive fringing field sensor increases to hold more water (18 drops of 652 mg is the maximum with this sensor) while the input frequency stays the same without exceeding the maximum frequency of 20 kHz, C will keep increasing to a point where the phase delay is near 180°, though it is not recommended to reach this limit so as to avoid phase jitter as mentioned in section 2.1. Specific applications can find their proper combinations of input frequency, capacitance range and fixed resistance according to (1) to maximize the linear operating range. Although averaged data fit the linear regression model better, single measurements are more typical in practice. The nominal R^2 and linear range of this specific design were thus selected to be 0.9989 and

140.04°/77.8% respectively from a single test which had the lowest R^2.

Main coefficients of linear regression model fitting for all the data sets and their averages are summarized in table 3. Each of the p-values was calculated under the number of observations of 19 and degree of freedom of 17. The result of every test fits a linear regression model well with an R^2 very close to 1 and a p-value much less than 0.05. These experiments not only validated the concept of the MOSFET interface technique, but they also demonstrated a significant improvement compared with the traditional RC phase delay interface circuit.

5. Comparisons with Previous Works

The novel design introduced in this paper is not only a significant improvement of the traditional RC phase delay interface circuit in the linear operation range, i.e. from 133.56° or 74.2% of each half cycle to 140.04° or 77.8% of each half cycle, but also shows merits compared with the previous design in (Meng and Dean, 2016). Comparing the pull-up and pull-down signal patterns in figure 6 with the ones in (Meng and Dean, 2016), the switching is faster in this design: 170 μs and 310 μs for the pull-up and pull-down times respectively for this design, compared with 8.53 ms and 6.65 ms for the pull-up and pull-down times respectively for the previous design (excluding the negligible differences in the switching times of the MOSFETs and the analog switch used previously: 12/11.4 ns, 9.5/7.2 ns, and 18/12 ns for the switching on/off times of the FDC6320CP, FDC6320CN, and ADG701 in (Meng and Dean, 2016) respectively). This is due to the fact that the previous design used two discrete resistors for R, a larger one of 270 kΩ and a smaller one of 10 kΩ, and a discrete bidirectional analog switch in parallel with the larger resistor, so that the larger resistor could be shorted to significantly reduce the RC time constant after the state change occurred. This resulted in a relatively larger RC time constant than the one in this new design, causing the pull-up and pull-down process to be slower when the 270 kΩ resistor was shorted to decrease the overall resistance.

Studying the slopes of linear trend lines gives us insights about higher sensitivities achieved by the novel design compared with previous works. For the linear trend line of the MOSFET interface circuit in figure 8a, the slope is 0.0088 V/pF and the intercept is 0.77 V, while the slope is 0.0012 V/mg and the intercept is 1.34 V for the plot in figure 8b. For the linear trend line of the MOSFET interface circuit in figure 9a, the slope is 0.0181 V/pF and the intercept is 1.41 V, while the slope is 0.0021 V/mg and the intercept is 2.59 V for the plot in figure 9b. While the outputs maintained good linearity when the input frequency increased from 12 kHz to 20 kHz, the sensitivity of the sensing system increased as well, specifically from 8.8 mV/pF to 18.1 mV/pF. In the experiments for the previous design, however, the sensitivities were 5.5 mV/pF for 2.5 kHz and 12.5 mV/pF for 6.25 kHz.

In this paper, the technique described provides the desired behavior with a simpler design and expands the linear operating range to 140.04°. The use of a single resistor

for R, and two discrete MOSFETs allows the circuit to operate over a wider range of input frequencies: 12 kHz to 20 kHz compared to 2.5 kHz to 6.25 kHz, which enables the circuit to be used in more capacitance measurement applications while providing greater accuracy. This technique also achieves a more symmetric PWM signal by using two control loops that have approximately identical reaction times.

6. Limits of Capacitance Measurements

The useful limits for capacitance measurement can be examined through determining the fastest operating speed for this capacitance measurement circuit. Assuming that the full range of 140.04° is employed around 90°, in order to optimize the use of the EXOR gate phase detector, the phase delay can be approximated using

$$\tau = 0.693R(C + C_{INV} + C_N + C_P) \tag{3}$$

where R is the series resistor used in the circuit, C is the unknown capacitance, C_{INV} is the input capacitance of the CMOS inverter, and C_N and C_P are the output capacitances for the NMOS and PMOS MOSFETS, respectively. C_{INV} is nominally 10 pF (Meng and Dean, 2016), and C_N and C_P are nominally 7.8 pF and 9 pF, respectively. Since the on-resistances for the NMOS and PMOS transistors are nominally 3.8 Ω and 10.6 Ω, and the on-resistances should be much less than R, the minimum value for R is assumed to 1000 Ω. Using these values with a minimum C value of 0 pF, (3) can be used to calculate a minimum value for τ of 18.57 ns. This value for τ corresponds to a switching frequency of 2.988 MHz, which is less that the maximum switching frequency for the CMOS inverters of 6.25 MHz (Meng and Dean, 2016). Equation (3) can then be used with the maximum phase delay to determine the maximum value for C, 402.48 pF. Therefore, the maximum capacitance range that can be supported with the interface circuit at its fastest operating speed is 0-402.48 pF at 2.988 MHz. With a 0-5V output voltage range, the resolution is 80.50 pF/V. For this capacitance range and detection speed, the detection limit would be determined by the thermal noise floor:

$$v_n = \sqrt{4KTRB} \tag{4}$$

where K is the Boltzmann's constant (1.38×10^{-23} J/K), T is the absolute temperature, R is series resistance in the circuit, and B is bandwidth. At 300 K, with an R of 1000 Ω, and a B of 2.988 MHz, the thermal noise floor is 7.034 μV, which corresponds to a detection limit of 0.566 fF.

7. Conclusions

RC phase delay is a straight forward technique for measuring an unknown capacitance. However, its linear range is severely limited by the incomplete charging and discharging of the unknown capacitance each half cycle. A novel MOSFET switching technique has been proposed to improve the performance of the RC phase delay interface circuit, to achieve a much wider linear range of operation. The proposed technique was successfully

simulated and experimentally validated using a PCB capacitive fringing field sensor as the unknown capacitance. The new technique achieved an R^2 value of 0.9989 over a range of 140.04° or 77.8% of each half cycle, compared to the linear range limitation of 45° or 25% of each half cycle for the traditional RC phase delay technique.

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