# A Technique for Improving the Linear Operating Range for a Relative Phase Delay Capacitive Sensor Interface Circuit

Yuan Meng and Robert Neal Dean, *Senior Member, IEEE*

***Abstract*— One technique for measuring an unknown sensor capacitance is using the phase delay of an *RC* network with a resistor and the sensor capacitor. By buffering the *RC* network with CMOS inverters, a square wave signal can be delayed through the circuit in proportion to the unknown capacitance. An EXOR gate can be used to compare the delayed square wave with a reference square wave to produce a pulsewidth-modulated signal where the pulsewidth is proportional to the unknown capacitance. This technique has a nearly linear response when the phase delay is small compared with the period of the square wave. However, this technique becomes severely nonlinear if the phase delay is larger than approximately one eighth of the period (45°), as the capacitor does not get fully charged or discharged every half period. To mitigate this nonlinearity, a novel resistance switching *RC* phase delay network is used to expand the linear range of the phase delay by accelerating the charging and discharging processes of the sensor capacitor. This approach is demonstrated using a fringing field capacitive sensor to measure the mass of added water and expands the linear operation to a phase delay to 133.56°.**

***Index Terms*— Capacitance measurement, interface circuit, *RC* phase delay.**

## I. Introduction

SENSORS that convert a measurand into a capacitance are widely used. Examples include sensors for measuring or detecting motion [1], touch [2], soil moisture content [3], moisture content of vegetation [4], moisture content of agricultural products [5], electrical properties of materials [6], fluidic pressure [7], and rain [8]. Many techniques have been developed to interface to capacitive sensors, including relative phase delay [9], relaxation oscillators [10], capacitance to duty cycle conversion [11], switched-capacitor dual-slope capacitance-to-digital conversion [12], resonant drive [13], bridge circuits [14], frequency locked loops [15], phase-locked loops [16], and the use of extreme learning machines [17].

Relative phase delay [9] is a simple technique for converting an unknown capacitance into a pulsewidth-modulated (PWM) signal. The capacitance to PWM conversion is linear over only a small operating range, which limits the usefulness of the technique. A small change to the technique, however, greatly improves the linear range of operation for this technique. The remainder of this paper presents that technique.

Manuscript received June 10, 2015; revised October 16, 2015; accepted October 18, 2015. Date of current version February 5, 2016. The Associate Editor coordinating the review process was Dr. Huang-Chen Lee.

The authors are with the Department of Electrical and Computer Engineering, Auburn University, Auburn, AL 36849 USA (e-mail: deanron@auburn.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIM.2015.2507698

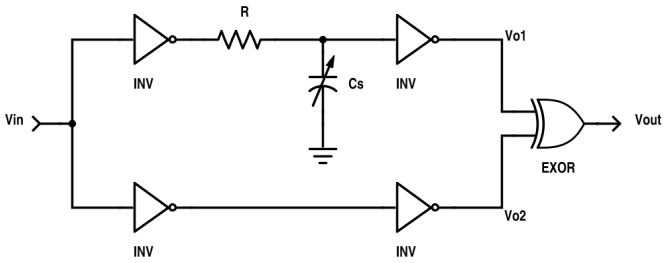


Fig. 1. Schematic of the original relative phase delay technique.

## II. Background

The relative phase delay technique [9] for measuring an unknown capacitance is based on periodic charging and discharging the unknown capacitance through a fixed resistor, where the *RC* pair is buffered on both sides by CMOS inverters. The resulting *RC* low-pass filter stage phase delays the square wave through the circuit. Simultaneously, the square wave is also passed through a parallel two-CMOS inverter circuit without the *RC* network. The outputs from both subcircuits are fed into an EXOR gate that serves as a phase detector for the two resulting square waves. The output signal from the EXOR gate is a PWM signal where the duty cycle is proportional to the unknown capacitance. This circuit is shown in Fig. 1, where $V_{\text{in}}$ is the input square wave to the circuit and $V_{\text{out}}$ is the output PWM signal.

The operation of the circuit assumes that the CMOS inverters have identical propagation delays and their trip voltage is equal to half the power supply voltage. If the fundamental frequency of the $V_{\text{in}}$ square wave is sufficiently low such that $C_s$ nearly fully charges or discharges between state changes, then the relative phase delay between $V_{o1}$ and $V_{o2}$, $t_{0.5}$, is approximately

$$t_{0.5} = 0.693R(C_s + C_g) \tag{1}$$

where $C_g$ is the input capacitance to a CMOS inverter. If a dc voltage proportional to $C_s$ is desired, it can be obtained by low-pass filtering $V_{\text{out}}$, the output PWM signal. Since the EXOR gate phase detector has a 180° monotonic phase

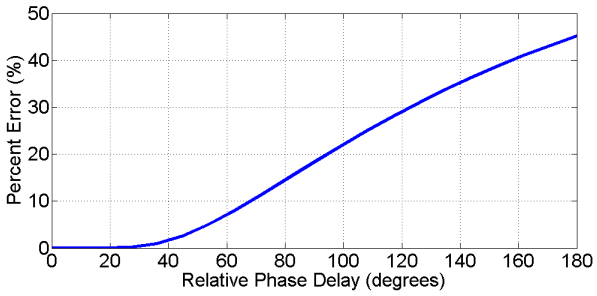


Fig. 2. Plot of percent error as a function of relative phase delay.

comparison range and it operates best around 90° to minimize phase jitter, additional inverter pairs can be added to the $V_{o1}$ or the $V_{o2}$ subcircuit to optimize the use of the phase detector.

When the frequency of $V_{\text{in}}$ is low enough so that $C_s$ nearly fully charges or discharges between state changes, the output PWM duty cycle is approximately linearly proportional to $C_s$. By increasing the frequency of $V_{\text{in}}$, the amount of duty cycle change over the full range of $C_s$ increases. But the approximation of $C_s$ fully charging or discharging between state changes is no longer valid, which results in the duty cycle being a nonlinear function of $C_s$. To understand the cause of the nonlinearity, let $V_c$ represent the magnitude of the nonzero voltage remaining across $C_s$ when $V_{\text{in}}$ changes states. As a consequence, the phase delay between $V_{01}$ and $V_{02}$ becomes

$$t_{0.5} = -R(C_s + C_g)\ln\left(\frac{0.5V_{\text{dd}}}{V_{\text{dd}} - V_c}\right) \tag{2}$$

where $V_{\text{dd}}$ is the power supply voltage and the relative phase delay is no longer a linear function of $C_s$ since $V_c$ increases as $C_s$ increases. The previous work determined that in order to limit the nonlinearity to 2.6%, the maximum phase delay could not exceed 45° or 25% of each half cycle [9]. This is shown in Fig. 2 in a plot of percent error, as a function of relative phase delay between $V_{o1}$ and $V_{o2}$ for a normalized case where the $RC$ time constant varies between 0s and 1s, while the square wave period is 2s (180° corresponds to 1s). The percent error is very low below approximately 30°. Recalling that the EXOR gate phase detector has a maximum useful range of 180°, the nonlinearity in capacitance measurement limits the useful range to only one-fourth of the possible range or a maximum duty cycle change of approximately 25%.

## III. Theoretical Development

Since the limitation for the maximum phase delay is due to the measured capacitor $C_s$ not being fully charged or discharged between each state change, the key to expanding the range of linear response is to accelerate the charging and discharging processes as soon as $V_c$ reaches the trip voltage. Referring to (2), if $V_{\text{dd}}$, $V_c$, $C_g$, and the range of $C_s$ are fixed, a relatively large $R$ dominates as the coefficient of the variable $C_s$. Therefore, when a relatively large $R$ is used corresponding to the value of $C_s$ and the input frequency, acceleration can be achieved by manipulating the resistance value at the time the trip voltage is reached.

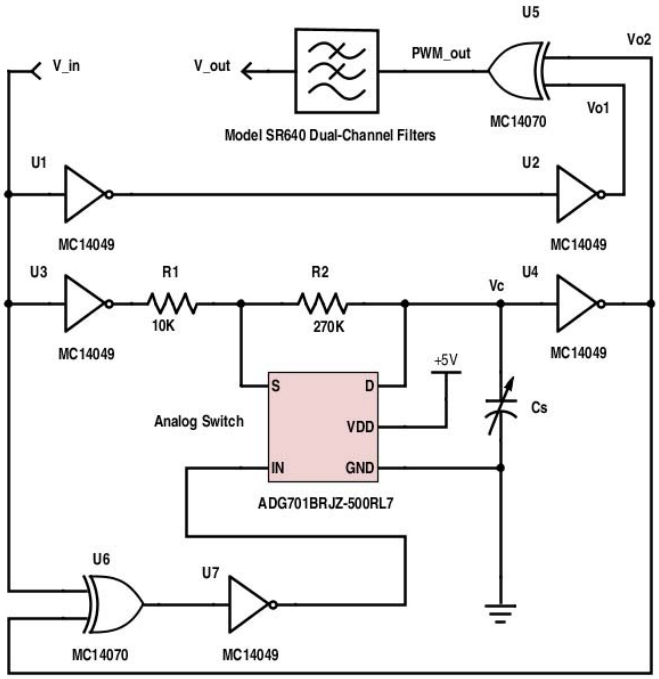


Fig. 3. Schematic of the resistance switching technique.

A novel resistance switching interface circuit is introduced in Fig. 3. In this circuit, the resistor $R$ from Fig. 1 is replaced by two resistors $R1$ and $R2$ in series, where $R2$ is much larger than $R1$. A commercial CMOS low-voltage 2-Ω analog switch (Analog Devices ADG701) is applied to short the larger resistor $R2$ by turning the analog switch ON when acceleration of charging and discharging is needed. This technique must be applied when $C_s$ is charging and discharging.

The analog switch is controlled by a logic circuit consisting of an EXOR gate connected to an inverter, which outputs a high voltage level to switch ON the analog switch when both $V_{o1}$ and $V_{o2}$ are at the same state and to switch OFF the analog switch otherwise. Therefore, the time for the unknown capacitor to be charged from 0 V up to the trip voltage or discharged from $V_{\text{dd}}$ down to the trip voltage is not affected, which is the phase delay time that determines the duty cycle of the output PWM signal. The time for charging from the trip voltage up to $V_{\text{dd}}$ or discharging from the trip voltage down to 0 V is greatly shortened using this technique.

Consequently, the maximum phase delay for a linear relationship between the output PWM duty cycle and the sensor capacitance is able to reach beyond 45° or 25% of each half cycle. Although the specific increase in the maximum phase delay also depends on the range of the measured variable capacitance and the frequency of the input square wave, it can theoretically be very close to the maximum useful range of 180° when needed. In practice, however, due to increased phase jitter near the 180° limit, avoiding reaching very close to this limit may make the measurement more accurate.

The output PWM signal can be low pass filtered to convert the output to a dc voltage proportional to the sensor capacitance. This technique has multiple benefits: a dc voltage is much easier to be measured compared with a PWM signal and

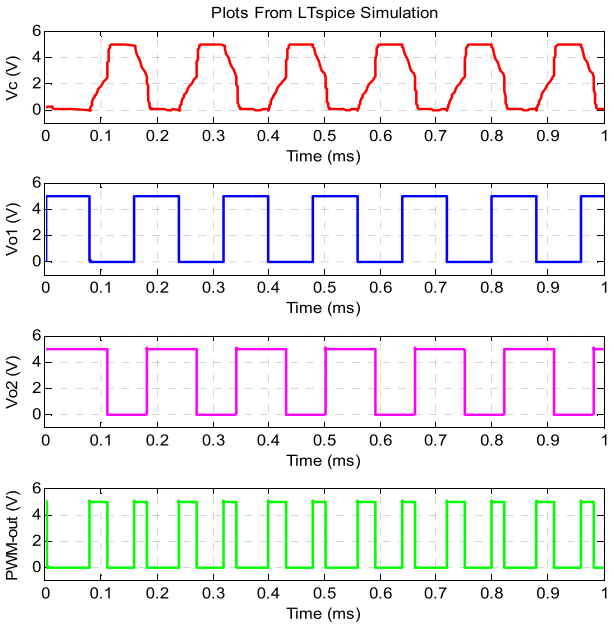


Fig. 4. Simulation results of the resistance switching *RC* phase delay interface circuit with $C_s = 82.78$ pF at 6.25 kHz.

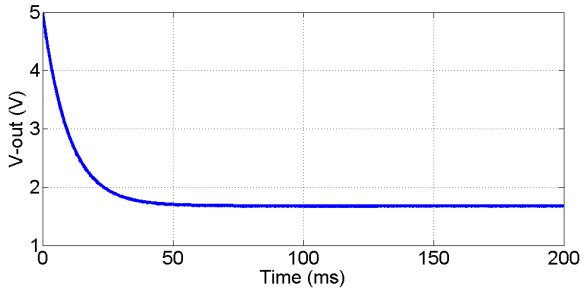


Fig. 5. Example simulation result of the PWM signal converted to a dc voltage with $C_s = 82.78$ pF at 6.25 kHz.

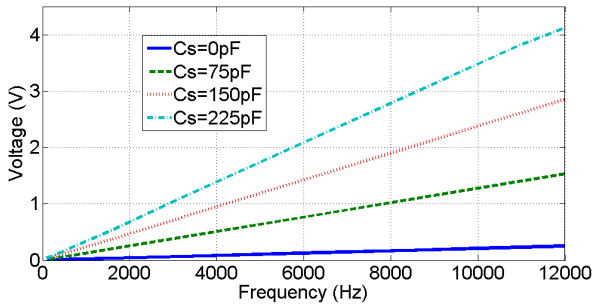


Fig. 6. Simulation results showing the dc output voltage for various values of $C_s$ for a 100 Hz to 12 kHz input square wave.

an asymmetrical PWM signal will be averaged by low-pass filtering so that the resulting dc voltage is still approximately proportional to the measured capacitance if the asymmetry is small. As shown in Fig. 3, a programmable model SR640 dual-channel low-pass filter was used to convert the PWM signal to a dc voltage. For the PWM output, the conversion rate is the frequency of the input square wave used. If a dc signal is desired by low-pass filtering the PWM signal, then the characteristics of the low-pass filter will determine the conversion rate.

## IV. Simulation

Fig. 4 shows the LTSpice simulation results of the novel resistance switching interface circuit with $R1$ of 10 kΩ and $R2$ of 270 kΩ as shown in Fig. 3, and a sensor capacitance of 82.78 pF with an input frequency of 6.25 kHz, as an example. SPICE models for the MC14049 and the MC14070, corresponding to the CMOS inverters and the EXOR gates, were used (Fig. 3). The electronic parts of these models were used in the prototype circuit in the next section as well.

The output of the LTSpice simulation with $C_s$ of 82.78 pF and an input frequency of 6.25 kHz is presented in Fig. 4. The top waveform is the voltage across the sensor capacitance, $V_c$, from which the charging and discharging processes are clearly observable. The upper middle and lower middle waveforms are the output voltages from the phase delay subcircuits, $V_{o1}$ and $V_{o2}$, respectively. The bottom waveform is the output PWM signal. Note that $V_c$ has sharp fully charging and fully discharging characteristics every time it reaches the trip voltage, which leaves a great potential for expanding the effective phase delay toward the approximately 180° linear range instead of only about 25% of it. Primarily due to the characteristics of the LTSpice models, which are verified by the experimental testing results shown in Fig. 7, the PWM signal (bottom waveform) is not perfectly symmetric. Although the extra gate capacitance of the logic gates and the output capacitance of the analog switch contribute to this phenomenon as well, the asymmetry is later averaged by the low-pass filter while being converted to a dc voltage (Fig. 5). According to the simulation results, the resistance switching improved the *RC* phase delay interface circuit as theorized.

A set of LTSpice simulations was run to evaluate the effects of varying the input square-wave frequency on the dc output voltage for $C_s$ values of 0, 75, 150, and 225 pF, respectively, using the circuit model from Fig. 3. For a $C_s$ value of 0 pF, only the CMOS input capacitance $C_g$ was in the circuit. An input square-wave frequency range of 100 Hz to 12 kHz was evaluated. Above 12 kHz, the phase delay exceeded the linear operating range of the circuit for a $C_s$ of 150 pF. The results shown in Fig. 6 show the linear response of the circuit.

## V. Experimental Verification

To experimentally evaluate the performance of the proposed interface circuit, a prototype was constructed and a capacitive sensor of known characteristics was integrated into the prototype circuit. An Agilent E3631A dc power supply was used to provide the 5 V dc supply voltage for the entire circuit. An Agilent 33220A 20 MHz function generator generated square waves with a 50% duty cycle and 5 V amplitude at selected frequencies for the $V_{\text{in}}$ signal. An Agilent MSO-X 2004A 70-MHz four-channel oscilloscope was used to capture the waveforms at $V_c$ (top waveform in Fig. 7), $V_{o1}$ (lower middle waveform), and $V_{o2}$ (upper middle waveform), and $\text{PWM}_{\text{out}}$ (bottom waveform). A GW Instek LCR-821 *LCR*

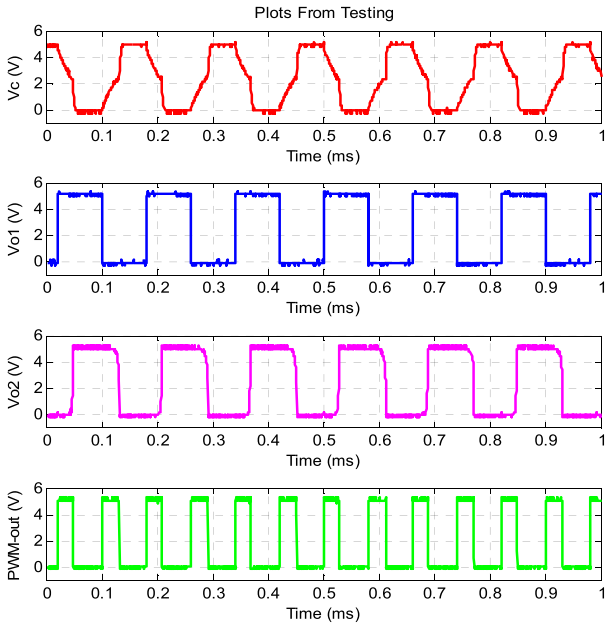


Fig. 7. Plots of oscilloscope records of the tested resistance switching circuit with $C_s = 82.78$ pF at 6.25 kHz.

meter was used to measure the capacitances of the capacitive sensor as the standard values for the testing. The PWM signal was low pass filtered using a Stanford Research Systems model SR640 programmable filter to convert the PWM output signal to a dc voltage.

### A. Fringing Field Capacitive Sensor

The capacitive sensor used to validate the design, as the $C_s$ in Fig. 3, was a fringing field capacitive sensor [18], [19] previously designed and implemented in printed circuit board (PCB) technology, whose output capacitance was previously demonstrated to linearly increase in proportion to the mass of a water drop on the active sensing area [3]. This kind of capacitive sensor was fabricated with two planar interdigitated electrodes on one side of the Cu foil on the PCB and covered by a solid layer of solder mask. The backside of the PCB, directly behind the electrode array, had an electrically floating Cu pad covered by solder mask as well. A photograph of the sensor is shown in Fig. 8. The sensor was 83.8 mm $\times$ 26.7 mm in size and the electrode array was approximately 10 mm $\times$ 8.5 mm. Each of the electrodes had 35 teeth and each of the teeth was overlapped to adjacent teeth by 9.7 mm. The gap between two opposing teeth was 152.4 $\mu$m.

Tap water was added to the surface of the solder mask over the electrode array within the effective sensing area drop by drop with an eye dropper. A single drop was maintained due to the nearly hydrophobic characteristic of the solder mask. The water interacted with the fringing fields in the volume above the PCB surface, and significantly increased the capacitance between the electrodes since the dielectric constant of water is approximately 80 times that of air. For instance, the measured sensor capacitance was 83.1 pF in air and 300 pF submerged in tap water. When an additional drop was added, the area


Fig. 8. Photograph of 359 mg of tap water on a fringing field capacitive sensor.

TABLE I
RECORDED DATA WITH AN INPUT FREQUENCY OF 2.5 kHz AT 22.2 °C AND 39% RELATIVE HUMIDITY

| Number of Testing | Mass of tap water (mg) | Sensor Capacitance (pF) | DC Voltage (V) | |
|---|---|---|---|---|
| | | | Resistance Switching Circuit | Traditional RC Circuit |
| 1 | 0 | 81.86 | 0.767 | 0.744 |
| 2 | 61 | 104.21 | 0.87 | 0.892 |
| 3 | 99 | 116.37 | 0.935 | 0.933 |
| 4 | 137 | 126.21 | 1.011 | 0.992 |
| 5 | 169 | 135.12 | 1.049 | 1.035 |
| 6 | 205 | 144.34 | 1.103 | 1.085 |
| 7 | 245 | 153.66 | 1.141 | 1.119 |
| 8 | 278 | 162.05 | 1.186 | 1.153 |
| 9 | 317 | 170.65 | 1.255 | 1.18 |
| 10 | 360 | 182.17 | 1.31 | 1.197 |
| 11 | 393 | 190.25 | 1.37 | 1.227 |
| 12 | 443 | 203.76 | 1.42 | 1.243 |
| 13 | 470 | 210.48 | 1.47 | 1.264 |
| 14 | 499 | 220.73 | 1.51 | 1.29 |
| 15 | 537 | 231.77 | 1.59 | 1.31 |
| 16 | 571 | 242.01 | 1.65 | 1.33 |

on the surface covered by water increased. According to [16], the capacitance tends to linearly increase with the increase in mass of the drop of water. A photograph of the sensor with a 359-mg drop of water on the sensing area is shown in Fig. 8.

### B. Testing Results

Testing of the circuit in Fig. 3 with the fringing field capacitive sensor was performed at ambient conditions in the laboratory. These conditions are shown in Tables I and II.

TABLE II
RECORDED DATA WITH AN INPUT FREQUENCY OF 6.25 kHz AT 22.8 °C AND 36% RELATIVE HUMIDITY

| Number of Testing | Mass of tap water (mg) | Sensor Capacitance (pF) | DC Voltage (V) | |
|---|---|---|---|---|
| | | | Resistance Switching Circuit | Traditional RC Circuit |
| 1 | 0 | 82.78 | 1.84 | 1.52 |
| 2 | 49 | 103.66 | 2.08 | 1.59 |
| 3 | 92 | 115.52 | 2.23 | 1.67 |
| 4 | 131 | 126.67 | 2.38 | 1.74 |
| 5 | 172 | 137.39 | 2.52 | 1.77 |
| 6 | 203 | 148.33 | 2.64 | 1.78 |
| 7 | 240 | 156.36 | 2.76 | 1.8 |
| 8 | 275 | 167.43 | 2.9 | 1.84 |
| 9 | 312 | 174.16 | 2.98 | 1.88 |
| 10 | 355 | 184.03 | 3.11 | 1.91 |
| 11 | 382 | 195.21 | 3.22 | 1.94 |
| 12 | 413 | 199.65 | 3.31 | 1.94 |
| 13 | 445 | 210.95 | 3.45 | 1.95 |
| 14 | 478 | 219.96 | 3.55 | 1.96 |
| 15 | 508 | 226.7 | 3.67 | 1.96 |
| 16 | 530 | 232.02 | 3.71 | 1.96 |

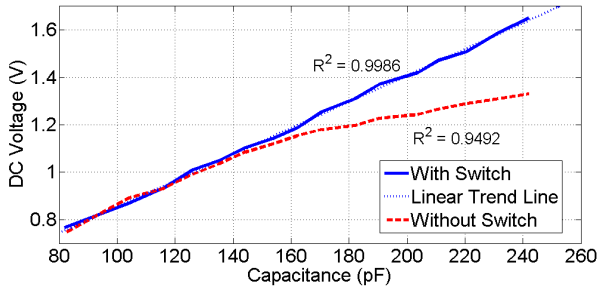


Fig. 9. Plot of dc voltage versus sensor capacitance at the frequency of 2.5 kHz.

The output dc voltage, the sensor capacitance measured by the *LCR* meter, and the mass of the composite water drop were collected every time a new drop of water was added. A switch was added to the circuit to disable the function of the resistance switching circuit to convert it back to the traditional *RC* phase delay circuit so that data of both circuits could be recorded and compared with an identical water drop. Using a 2.5 kHz input square wave, the data were recorded in Table I.

For this testing, 15 drops of tap water were added within the sensing area on the sensor's surface until the edge of the water bead reached close to the limit of its active area. In addition, the data were collected without water on the sensor. Therefore, 16 output dc voltage levels were recorded from the resistance switching interface circuit and the traditional *RC* phase delay circuit. The relationship between the dc voltage versus the sensor capacitance is presented in Fig. 9, in which the solid line represents the resistance switching circuit and the dashed line represents the traditional circuit. Along with a linear trend dotted line, the solid line shows a nearly linear relationship with an $R^2$ value of 0.9986. Observe, however, the dashed line from the traditional circuit starts to deviate from the linear trend and bends down when the

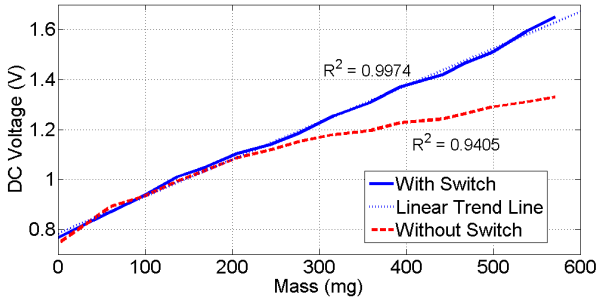


Fig. 10. Plot of dc voltage versus measured mass of water at the frequency of 2.5 kHz.

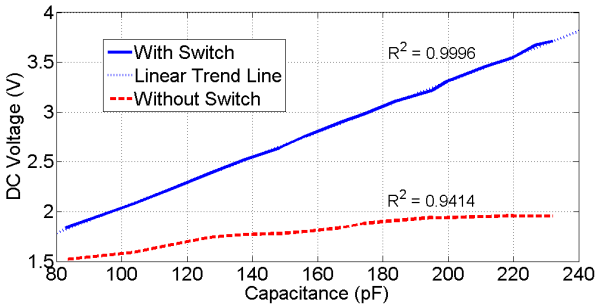


Fig. 11. Plot of dc voltage versus sensor capacitance at the frequency of 6.25 kHz.

capacitance increases to a point near 140 pF. This is due to the sensor capacitor not being nearly fully charged and discharged when the *RC* phase delay increases larger than 45° or 25% of each half cycle, as discussed previously.

The same characteristics can be observed in Fig. 10, where dc voltage is plotted versus the mass of the water drop. The linearity for the resistance switching circuit ($R^2$ is 0.9974), however, is not quite as good as the linearity between the dc voltage and the capacitance. This is a result of the sensing mechanism employed by the sensor, not the interface circuit. Yet the improvement compared with the traditional circuit is still clear.

As it was expected that the nonlinearity of the traditional circuit response would be more severe when the phase delay keeps increasing beyond 45° or 25% of each half cycle, it is interesting to explore the limitation of the resistance switching circuit by increasing the input frequency. The maximum input frequency turned out to be 6.25 kHz. The data were recorded in Table II from both circuits being tested at this frequency and plotted in Figs. 11 and 12. In those plots, the traditional circuit failed to give a linear response, while the resistance switching circuit still worked as designed. Instead of being limited to 45° or 25% of each half cycle, the linear range of the new phase delay circuit was expanded to 133.56° or 74.2% of each half cycle. Testing not only validated the concept of the resistance switching technique, but it also demonstrated a significant improvement compared with the traditional *RC* phase delay interface circuit. Observe that the test data in Fig. 11 at 82.78 pF closely matches the simulation results in Fig. 5. However, at the larger $C_s$ values, the experimental circuit had a larger conversion gain than the

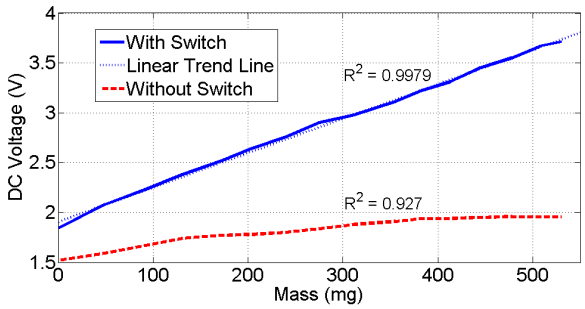


Fig. 12. Plot of dc voltage versus measured mass of water at the frequency of 6.25 kHz.

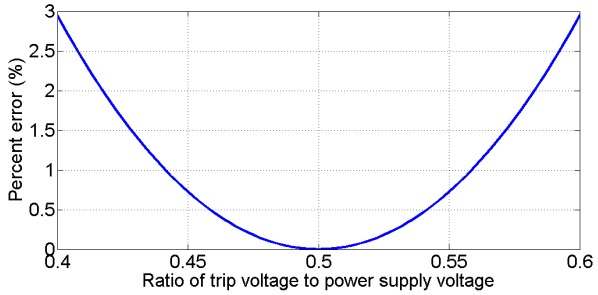


Fig. 13. Plot of percent error in the capacitance to pulse width conversion versus the ratio of the CMOS inverter trip voltage to the power supply voltage.

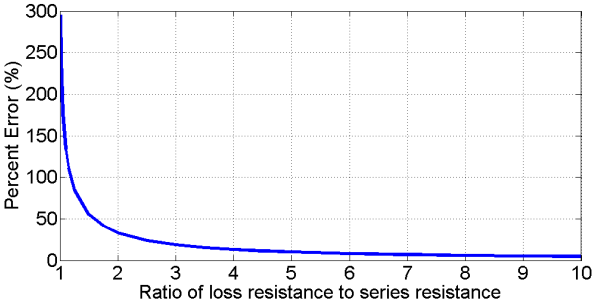


Fig. 14. Plot of percent error versus the ratio of the parallel resistance to the series resistance.

simulated circuit. The LTSpice simulation used manufactures' device models, and it is believed that these models were closer to worst case performance specifications than the devices used in the experimental prototype.

## VI. Practical Implications

### A. Performance Limitations

Noise in the system will obviously affect the minimum resolution, resulting in phase jitter in the width of the PWM pulses. Therefore, standard good engineering practices should be used to minimize electrical noise in the system. The achievable resolution will also be impacted by the characteristics of the low-pass filter used to convert the PWM signal to a dc signal proportional to the unknown capacitance.

The high frequency limit of the input square wave will either be determined by the *RC* time constant of the delay stage or by the switching speed of the CMOS inverter. The MC14049 has a maximum switching speed of approximately 6.25 MHz using a 5 V supply voltage. This inverter has a 10-pF typical gate capacitance, while the ADG701 has a 2 Ω ON-resistance. Using these values for $R$ and $C$ and allowing the capacitor to charge up to 99% of 5 V, the maximum frequency limit would be 5.42 GHz. Therefore, the CMOS inverter speed is the limiting factor for the highest possible frequency input square wave that can be used, regardless of the value of the capacitance being measured.

### B. Imperfect CMOS Inverter

Ideally, the trip voltage of a CMOS inverter is equal to the supply voltage divided by two. In reality, the trip voltage differs from this value due to manufacturing tolerances [20]. When the trip voltage is not ideal, the pulsewidth for the capacitor charging and discharging cycles are unequal. However, due to the logarithmic relationship between trip voltage and charging/discharging time, as illustrated in (2), the resulting pulses will also be proportionally unequal in length, resulting in an error in measurement. For a reasonably good CMOS inverter, with a trip voltage being between 40% and 60% of the supply voltage, the worst case error is approximately 3%, as shown in Fig. 13 in a plot of percent error in the capacitance to pulsewidth conversion versus the trip voltage to the power supply voltage ratio.

### C. Capacitance Measurement in a Lossy Material

In many applications, the capacitance being measured uses a lossy dielectric that can be discretely modeled as a resistance in parallel with the unknown capacitance. Referring back to Fig. 1, the parallel resistance forms a voltage divider circuit with the series resistor $R$, with a delayed response due to $C_s$ and both resistors. This results in capacitance measurement errors that increase significantly as the ratio of the loss resistance in parallel with the capacitance to the series resistance in the circuit approaches unity. A series of LTSpice simulations were run to evaluate this effect, with the results shown in Fig. 14. For this simulation, a series resistance of 100 kΩ and a 100-pF capacitor were used, while the parallel resistance was varied between 101 and 1000 kΩ, while the resulting pulsewidth after a CMOS inverter was measured and compared with the pulsewidth with an infinite parallel resistance. The resulting measurement error varied from 3.56% with a resistance ratio of 10 to 295.68% with a resistance ratio of 1.01.

For the fringing field sensor used in Section V, the sensor architecture results in a dc blocking capacitor in series with the parallel loss resistance term due to the solder mask coating over the electrodes [3], which greatly reduces the measurement error compared with Fig. 14, resulting in a nearly linear sensor response as shown in Figs. 9–12.

## VII. Conclusion

*RC* phase delay is a simple technique for measuring an unknown capacitance. However, its linear range is severely limited due to incomplete charging and discharging of the unknown capacitance in each half cycle. A resistance

switching technique has been proposed to improve the performance of the *RC* phase delay interface circuit, to achieve a much wider linear range of operation. The proposed technique was successfully simulated and experimentally validated using a PCB capacitive fringing field sensor with an output capacitance range of approximately 80 pF to 245 pF. This technique achieved an $R^2$ value of 0.9996 over a relative phase delay range of 133.56°, compared with the linear range limitation of 45° for the traditional *RC* phase delay technique. This capacitive sensor interface technique is particularly useful for sensors that have relatively large capacitance ranges, such as fringing field sensors.

## REFERENCES


[1] G. Langfelder, A. F. Longoni, A. Tocchio, and E. Lasalandra, "MEMS motion sensors based on the variations of the fringe capacitances," *IEEE Sensors J.*, vol. 11, no. 4, pp. 1069–1077, Apr. 2011.

[2] S. Tsuji and T. Kohama, "A layered 3D touch screen using capacitance measurement," *IEEE Sensors J.*, vol. 14, no. 9, pp. 3040–3045, Sep. 2014.

[3] R. N. Dean, A. K. Rane, M. E. Baginski, J. Richard, Z. Hartzog, and D. J. Elton, "A capacitive fringing field sensor design for moisture measurement based on printed circuit board technology," *IEEE Trans. Instrum. Meas.*, vol. 61, no. 4, pp. 1105–1112, Apr. 2012.

[4] A. Afzal, S. F. Mousavi, and M. Khademi, "Estimation of leaf moisture content by measuring the capacitance," *J. Agricult. Sci. Technol.*, vol. 12, no. 3, pp. 339–346, 2010.

[5] C. V. K. Kandala, C. L. Butts, and S. O. Nelson, "Capacitance sensor for nondestructive measurement of moisture content in nuts and grain," *IEEE Trans. Instrum. Meas.*, vol. 56, no. 5, pp. 1809–1813, Oct. 2007.

[6] Z. Liu, S. Liu, Y. Luo, J. Wang, and S. Wang, "Permittivity measurement of wood based on an uniplanar capacitance sensor," in *Proc. IEEE Int. Conf. Inf. Autom.*, Harbin, China, Jun. 2010, pp. 912–916.

[7] J. Huang, H. Yuan, Y. Cui, and Z. Zheng, "Nonintrusive pressure measurement with capacitance method based on FLANN," *IEEE Trans. Instrum. Meas.*, vol. 59, no. 11, pp. 2914–2920, Nov. 2010.

[8] I. Bord, P. Tardy, and F. Menil, "Influence of the electrodes configuration on a differential capacitive rain sensor performances," *Sens. Actuators B, Chem.*, vol. 114, no. 2, pp. 640–645, Apr. 2006.

[9] R. Dean, A. Rane, and N. Hyatt, "A capacitive sensor interface circuit based on relative phase delay," in *Proc. 55th Int. Instrum. Symp.*, League City, TX, USA, Jun. 2009, pp.1–12.

[10] Y. Liu, S. Chen, M. Nakayama, and K. Watanabe, "Limitations of a relaxation oscillator in capacitance measurements," *IEEE Trans. Instrum. Meas.*, vol. 49, no. 5, pp. 980–983, Oct. 2000.

[11] Z. Ignjatovic and M. F. Bocko, "An interface circuit for measuring capacitance changes based upon capacitance-to-duty cycle (CDC) converter," *IEEE Sensors J.*, vol. 5, no. 3, pp. 403–410, Jun. 2005.

[12] B. George and V. J. Kumar, "Analysis of the switched-capacitor dual-slope capacitance-to-digital converter," *IEEE Trans. Instrum. Meas.*, vol. 59, no. 5, pp. 997–1006, May 2010.

[13] B. Cagdaser and B. E. Boser, "Resonant drive: Sense and high voltage electrostatic drive using single MEMS capacitor and low voltage electronics," in *Proc. 18th Int. Conf. Micro Electro Mech. Syst.*, Miami Beach, FL, USA, Jan./Feb. 2005, pp. 142–146.

[14] B. Fellmuth, H. Bothe, N. Haft, and J. Melcher, "High-precision capacitance bridge for dielectric-constant gas thermometry," *IEEE Trans. Instrum. Meas.*, vol. 60, no. 7, pp. 2522–2526, Jul. 2011.

[15] R. N. Dean and A. K. Rane, "A digital frequency-locked loop system for capacitance measurement," *IEEE Trans. Instrum. Meas.*, vol. 62, no. 4, pp. 777–784, Apr. 2013.

[16] T. M. Supon, K. Thangarajah, R. Rashidzadeh, and M. Ahmadi, "A PLL based readout and built-in self-test for MEMS sensors," in *Proc. IEEE 54th Int. Midwest Symp. Circuits Syst.*, Seoul, Korea, Aug. 2011, pp. 1–4.

[17] G. Sarkar, A. Chatterjee, A. Rakshit, and K. Bhattacharya, "Hierarchical extreme learning machine-polynomial based low valued capacitance measurement using frequency synthesizer–vector voltmeter," *IEEE Trans. Instrum. Meas.*, vol. 63, no. 9, pp. 2180–2187, Sep. 2014.

[18] J. Mizuguchi, J. C. Piai, J. A. de França, M. B. de Morais França, K. Yamashita, and L. C. Mathias, "Fringing field capacitive sensor for measuring soil water content: Design, manufacture, and testing," *IEEE Trans. Instrum. Meas.*, vol. 64, no. 1, pp. 212–220, Jan. 2015.

[19] M. A. M. Yunus and S. C. Mukhopadhyay, "Development of planar electromagnetic sensors for measurement and monitoring of environmental parameters," *Meas. Sci. Technol.*, vol. 22, no. 2, p. 025107, 2011.

[20] A. Mukherjee, *Introduction to N-Channel Metal-Oxide Semiconductor and Complementary Metal-Oxide Semiconductor Very Large Scale Integration Systems Design*. Englewood Cliffs, NJ, USA: Prentice-Hall, 1986, pp. 30–31.


**Yuan Meng** received the B.S. degree in optical information science and technology from Guizhou University, Guiyang, China, in 2011, and the M.S. degree in electrical engineering from Auburn University, Auburn, AL, USA, in 2015, where he is currently pursuing the Ph.D. degree in electrical engineering.

He is currently a Research Assistant with the Department of Electrical and Computer Engineering, Auburn University. His current research interests include microelectromechanical systems sensors, microelectronic fabrication, and interface electronics.

**Robert Neal Dean** (M'90–SM'10) received the B.E.E., M.S., and Ph.D. degrees from Auburn University, Auburn, AL, USA, in 1988, 1991, and 2006, respectively, all in electrical engineering.

He is currently a McWane Endowed Associate Professor with the Department of Electrical and Computer Engineering, Auburn University. He teaches the undergraduate senior design course and graduate courses in sensors, microelectromechanical systems (MEMS), and photovoltaics. His current research interests include sensors, MEMS, instrumentation electronics, chaos electronics, and power electronics.