NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2015-2016

CE1005/CZ1005 – DIGITAL LOGIC

Nov/Dec 2015 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 6 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. All questions carry equal marks.

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1. (a) Perform the following number conversions. Show all the steps clearly.

(i) Convert 672.15 (in octal) to hexadecimal.

(2 marks)

(ii) Convert C1.FD (in hexadecimal) to decimal. Give your answer in 6 significant digits.

(2 marks)

(iii) Convert 6.48 (in decimal) to binary. Give your answer in 8 significant bits.

(3 marks)

(b) A digital system is used to record the number of people visiting a facility. Assume that the number of visitors in any single day does not exceed three thousand. Determine the number of bits required to represent the total number of visitors in one year (assume 365 days) in unsigned binary. Show each step clearly.

(5 marks)

Note: Question No. 1 continues on Page 2

(c) Simplify the following Boolean expression algebraically. Show each step clearly and give your answer in Sum-of-Product (SOP) form.

$$F(a, b, c, d) = (a' c' + d')(b d + c')' (a' d + (b' c)')' + (c + d')'$$

(7 marks)

(d) A circuit has the following canonical Boolean expression:

$$F^* = (A + B + C^*)(A + B' + C^{*'})(A' + B' + C^*)$$

Draw a logic circuit diagram with suitable symbols and matched bubbles to clearly illustrate the three maxterms that assert the active Low output F*. The inputs A and B are both active High while the input C* is active Low. Do not expand or simplify the expression.

(6 marks)

2. (a) There are four judges in a contest: one chief judge and three assistant judges. All the judges make independent decisions. A contestant is successful when

- all three assistant judges pass him/her, or
- both the chief judge and at least one assistant judge pass him/her.

Otherwise, the contestant is unsuccessful.

A combinational logic circuit takes the four judges' individual decisions as inputs to produce the success status for a contestant.

(i) Construct a truth table for the success status output SU (1 means Successful, 0 means Unsuccessful). Take A, B, C and D as individual decision inputs (1 means Pass, 0 means Fail) from the chief judge and assistant judges.

(6 marks)

(ii) By using a Karnaugh map, find the minimum-cost Sum-of-Product expression for the output SU. Show all the loops clearly.

(5 marks)

Note: Question No. 2 continues on Page 3

(b) (i) Represent each of the following signed decimal values in 8-bit 2's complement format. Show all the steps clearly.

- -72
- +67

(4 marks)

(ii) A circuit produces a logic High output when its input, a signed decimal value falls between the range of -72 and +67 (both values included). Otherwise the output is Low. Assume that the input is represented in 8-bit 2's complement format. Determine the Boolean expression of the circuit output. You are not required to simplify the expression.

(4 marks)

(c) Figure Q2 shows a logic circuit with inputs, EN and A, and output X. Describe how the circuit works and determine its truth table.

(6 marks)

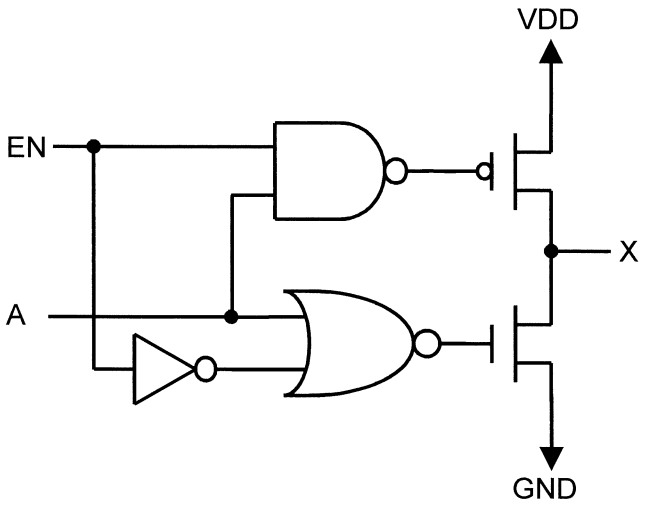

Figure Q2

3. A majority gate is a combinational circuit in which the output is a 1 if the majority of the inputs are 1's, otherwise the output is a 0. A 3-input majority gate has an input bus *A[2:0]* and an output *Z*.

(a) You are required to implement the 3-input majority gate.

(i) Draw a Karnaugh map for the 3-input majority gate and find the minimized SOP (Sum-of-Products) expression.

(5 marks)

(ii) Draw a logic circuit that implements the minimized SOP expression.

(4 marks)

(iii) Write the Verilog module for the logic circuit by using structural gate-level primitives in Verilog.

(5 marks)

(b) The 3-input majority gate can be implemented using a 4-to-1 multiplexer.

(i) Complete the 3-input majority gate in Figure Q3 by indicating the appropriate inputs *A[2:0]* at respective '?'.

(5 marks)

(ii) Write the combinational **always** block in Verilog for the 3-input majority gate in Q3b(i).

(6 marks)

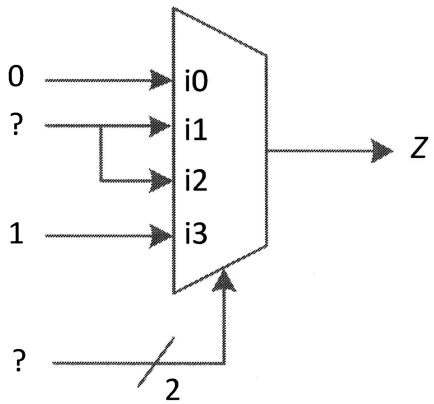

Figure Q3

4. (a) Figure Q4a shows a circuit with two inputs (*Clk* and *Rst*) and one 2-bit output bus (*Q[1:0]*).

(i) Complete the timing diagram shown in Figure Q4b for the circuit in Figure Q4a by drawing the waveforms for *Q[1]* and *Q[0]*. Assume that *Rst = 0*.

(8 marks)

(ii) Write the Verilog module for the circuit in Figure Q4a with synchronous reset.

(8 marks)

(iii) Draw the state transition diagram of the circuit in Figure Q4a. Each state must be labelled with the output *Q[1:0]*.

(4 marks)

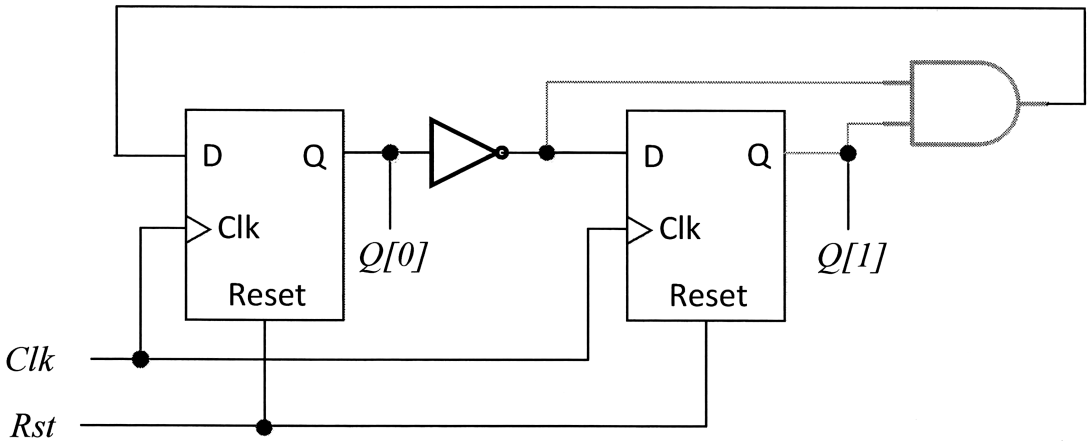

Figure Q4a

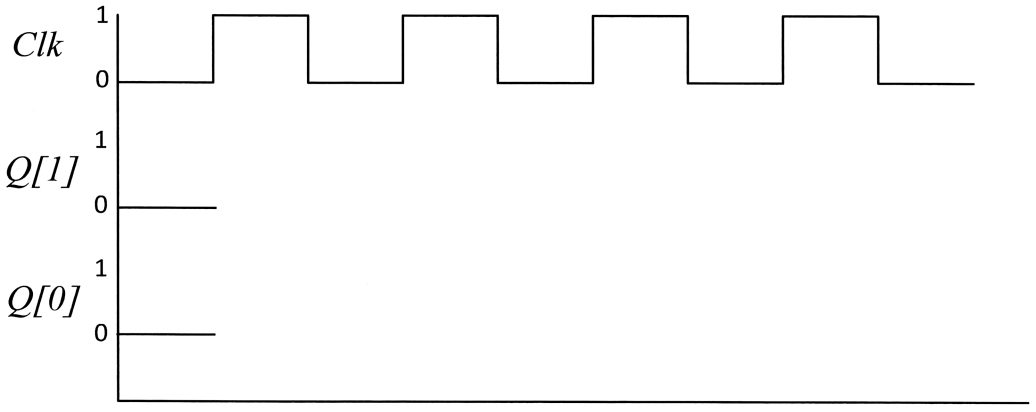

Figure Q4b

Note: Question No. 4 continues on Page 6

(b) A mobile robot detects the presence of obstacles by using front and side sensors, and navigates by traversing along the obstacle walls. The finite state machine (FSM) for the mobile robot should have three active High inputs: *start*, *front_obstacle* and *end_wall*; and one output: *on_buzzer*:

- The FSM starts in the *idle* state.
- In the *idle* state, if *start* is asserted, the FSM moves to the *forward* state.
- In the *forward* state, if *front_obstacle* is asserted, the FSM moves to the *turn_left* state.
- In the *turn_left* state, the *on_buzzer* output is HIGH and the FSM moves to the *follow_wall* state at the rising edge of the clock. The *on_buzzer* output is LOW in other states.
- In the *follow_wall* state, if *end_wall* is asserted, the FSM moves to the *clear_wall* state.
- In the *clear_wall* state, if *front_obstacle* is asserted, the FSM moves to the *turn_left* state. Otherwise, the FSM moves to the *turn_right* state at the rising edge of the clock.
- In the *turn_right* state, the FSM moves to the *forward* state at the rising edge of the clock.

Draw the state transition diagram that captures the above behavior of the robot.

(5 marks)

END OF PAPER

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Please read the following instructions carefully:

1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.