NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 2 EXAMINATION 2014-2015

CE1005/CZ1005 – DIGITAL LOGIC

Apr/May 2015 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 5 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. All questions carry equal marks.

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1. (a) Perform the following number conversions. Show all steps clearly.

   (i) Convert 2A.B (in hexadecimal) to decimal. (2 marks)

   (ii) Convert 745.37 (in octal) to hexadecimal. (2 marks)

   (iii) Convert 1.136 (in decimal) to binary. Give your answer in 8 significant digits. (3 marks)

   (b) Determine the number of bits required to represent an unsigned 15-digit decimal number in each format below. Show all steps clearly.

   (i) BCD (binary coded decimal) (2 marks)

   (ii) Binary (4 marks)

Note: Question No. 1 continues on Page 2

(c) Using algebraic manipulations, obtain the minimum-cost SOP (Sum of Product) expression for the following logic function. Show all steps clearly.

$$F(w, x, y, z) = (x + y' z')' (w' + x' y) (w + x y + y' z)'$$

(6 marks)

(d) Implement the following logic function using a minimum number of 2-input NOR gates only. Illustrate with a clearly labelled circuit diagram.

$$F(a, b, c) = (b + c) (a' + b' + c')$$

(6 marks)

2. (a) (i) Briefly describe the following parameters of a logic device:

- VOL(max)
- VOH(min)
- VIL(max)
- VIH(min)

(4 marks)

(ii) State the relation between the parameters in Q2(a)(i) and the device's noise margin.

(2 marks)

(b) Each operand enclosed within a pair of square brackets is a signed decimal number. Represent each operand in 8-bit 2's complement format and perform the arithmetic operations. Show all steps clearly. State clearly whether or not there is overflow in each case.

(i) [-28] + [101]

(4 marks)

(ii) [-61] – [73]

(4 marks)

Note: Question No. 2 continues on Page 3

(c) (i) A 4-input combinational logic circuit with active low output F* is described by the following canonical expression. Use a Karnaugh map to obtain the minimum-cost POS (Product of Sum) expression for F*. Show all loops clearly on the Karnaugh map.

$$F^*(A, B, C, D) = \prod M(1, 3, 4, 6, 9, 11, 14)$$

(6 marks)

(ii) The inputs A and D are active low. Replace the variable names A and D with A* and D* respectively in the POS expression you have obtained in Q2(c)(i).

(1 mark)

(iii) Using suitable logic symbols with matched bubbles, draw a clearly labelled logic circuit diagram to illustrate the relation between F* and the four inputs A*, B, C and D*.

(4 marks)

3. (a) A full adder performs a single bit addition by taking inputs *a*, *b* and *cin*, and produces outputs *sum* and *cout*.

(i) Write down the truth table for a full adder.

(3 marks)

(ii) Draw a gate-level circuit for the full adder, using only 2-input gates.

(4 marks)

(b) You are provided with a Verilog implementation of the full adder described in Q3(a) with the following module declaration.

```
module full_add(input a, b, cin, output sum, cout);
```

(i) Implement a Verilog module that adds two 3-bit numbers, *x[2:0]* and *y[2:0],* and returns a 3-bit answer *total[2:0]* and an overflow output *oflow*. You are required to use the full_add module in your implementation. There should be no carry in. You can hard-wire a signal by setting it to an appropriate logic value.

(10 marks)

Note: Question No. 3 continues on Page 4

(ii) Briefly describe how you can change the implementation in Q3(b)(i) to realize a 3-bit adder/subtractor. You do not need to implement the full module.

(3 marks)

(iii) Explain why we do not generally build arithmetic circuits in this manner. What is the preferred approach in modern design?

(2 marks)

(c) Briefly describe the functionality of a multiplexer. How can you create a 2-by-1 multiplexer using a single Verilog **assign** statement?

(3 marks)

4. (a) Write a Verilog module of an enabled 5-bit counter. The module should also include an additional *jump* input that, when asserted, increases the counter by 5 rather than increment by 1. Assume all inputs are active high.

(7 marks)

(b) The waveform in Figure Q4a is used to drive the counter. Show the resulting output sequence of the counter.

(4 marks)

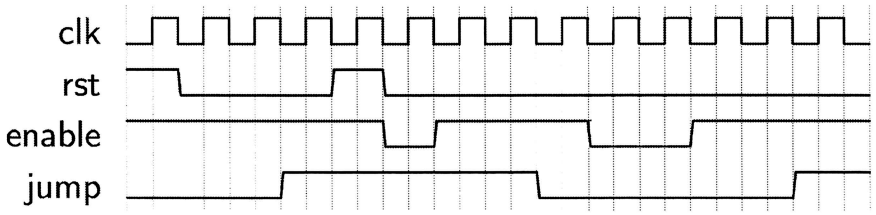

Figure Q4a

(c) Figure Q4b shows a finite state machine (FSM) state transition diagram. Implement the FSM in Verilog using an **always** block for the state transition logic and a separate **always** block for the state register. Assume missing transitions are self-transitions.

(8 marks)

Note: Question No. 4 continues on Page 5

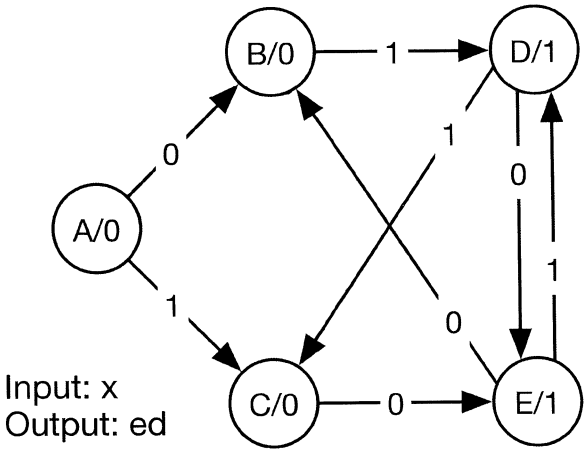

Figure Q4b

(d) Deduce the function of the FSM in Q4(c).

(3 marks)

(e) Briefly explain the difference between a latch and a flip-flop and why one is preferred over the other in modern digital design.

(3 marks)

END OF PAPER

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Please read the following instructions carefully:

1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.