NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 2 EXAMINATION 2012-2013

CE1006/CZ1006 – COMPUTER ORGANIZATION AND ARCHITECTURE

Apr/May 2013 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 7 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. All questions carry equal marks.
5. The VIP Instruction Set Summary Chart is provided in Appendix 1 on page 7.

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1. Figure Q1a shows the hexadecimal contents of several registers in the VIP processor and a section of its memory.

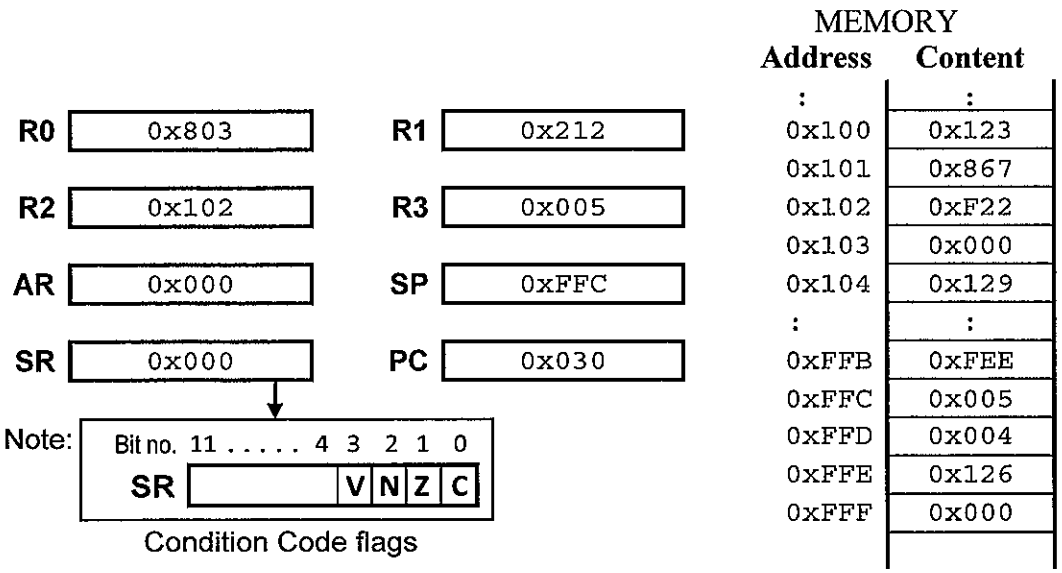

Figure Q1a

Note: Question No. 1 continues on Page 2

(a) Give (*in hexadecimal*) the 12-bit contents in the two registers **R0** and **SR**, *immediately after* the execution of each instruction given below.

Note: Instructions (i) to (vi) are **not consecutive instructions**. You must use the initial conditions shown in Figure Q1a to derive your answer for each of the instructions given below.

(i) `MOV R0,R3`

(ii) `MOV R0,#0xFFF`

(iii) `MOV R0,[R2+1]`

(iv) `RAR R0`

(v) `EOR R0,R1`

(vi) `POPM 3`

(12 marks)

(b) With reference to the VIP assembly language program in Figure Q1b, give (*in hexadecimal*) the 12-bit contents of registers **R0**, **R1** and **R2** **after** the execution of the instruction at the address label **DONE**. Assume execution of the given series of consecutive instructions begins at the label **START**.

Note: The instructions **JGT SKIP** and **JPL LOOP** will be assembled with the appropriate relative offset that will allow each instruction to jump to the respective address labels indicated.

(9 marks)

```
START   MOV   R0,#2
        MOV   R1,#4
        MOV   R2,R0
LOOP    CMP   R1,R0
        JGT   SKIP
        ADD   R2,R2
SKIP    NEG   R1
        DEC   R0
        JPL   LOOP
        DEC   R0
DONE    ADDC  R2,R2
```

Figure Q1b

(c) A VIP instruction with the mnemonic **CALL 0x020** is stored at the starting address of **0x020**. Describe clearly what will happen when this instruction is executed.

(4 marks)

2. (a) A VIP assembly language program and the contents of several registers and memory variables are given in Figure Q2a. Give the mnemonics of (I1), (I2), (I3), (I4) and (I5) that will complete the missing instructions based on their associated comments.

(8 marks)

```
Address
0x000  Main  MOV   SP,#0xFFF   ; Initialize stack pointer
0x002          ?               ; Push value in memory variable VarA to stack   (I1)
0x004          ?               ; Push value in memory variable VarB to stack   (I2)
0x006          ?               ; Push address of memory variable VarC to stack (I3)
0x008        CALL  Sub1        ; Call subroutine Sub1
0x00A          ?               ; Remove stack parameters                       (I4)
                :
                :
                :
0x030  Sub1  PSHM  3           ; Instruction (S1)
                :
                :
                :              ; to be completed
                :              ; as required in
                :              ; question Q2(c)
                :
                :
                :
                ?              ; Return to calling program                     (I5)
```

Address	Contents
VarA 0x200	0x444
VarB 0x201	0x555
VarC 0x202	0x666

R0	0x000	R1	0x111
R2	0x222	R3	0x333

Figure Q2a

(b) Draw a labeled memory map to show all the known contents on the system stack immediately after the execution of the `PSHM 3` instruction at (`S1`). Your diagram must include (*in hexadecimal*) the stack addresses and their respective contents. Assume the program given in Figure Q2a begins execution at the address label `Main`.

(8 marks)

(c) The subroutine `Sub1` implements the C language code given in Figure Q2b. Complete the remaining portion of subroutine `Sub1` based on the way the parameters `VarA`, `VarB` and `VarC` have been passed in Figure Q2a. Based on your solution, state clearly what assumption you have made regarding the nature of the three variables `VarA`, `VarB` and `VarC`.

(9 marks)

```
if (VarA >= VarB)
  VarC = VarA + VarB;
else
  VarC = VarA - VarB;
```

Figure Q2b

3. (a) With reference to computer memory, state the key difference between volatile and non-volatile memory. For each memory device listed below, determine if the device is volatile or non-volatile. Briefly describe the working principle that enables the device to store information.

(i) Magnetic hard-disk

(ii) Compact Flash (CF) card

(iii) Digital Video Disc (DVD)

(11 marks)

(b) Computer systems employ input/output (I/O) control methods that include programmed I/O, interrupt-driven I/O and direct memory access. Among these three I/O control methods, state which is the most suitable to process each of the I/O device listed below. In each case, provide justifications for your choice.

(i) Mouse input device

(ii) Digital Video Disc (DVD) player

(6 marks)

(c) Table Q3a shows a page table for a virtual address space (composed of 8 pages of 512 bytes each) mapped into 2048 bytes of physical address space. Assume all addresses are memory byte addresses starting from zero. For each of the hexadecimal virtual addresses ($\mathbf{00000_{16}}$, $\mathbf{00202_{16}}$, $\mathbf{00640_{16}}$ and $\mathbf{00808_{16}}$), find the corresponding virtual page number and indicate its physical address (*in hexadecimal*), if any. Indicate clearly for cases where a page fault will occur.

(8 marks)

Table Q3a

Virtual Page Number	Valid Bit	Page Frame Number
0	1	3
1	1	2
2	1	1
3	0	-
4	0	-
5	1	0
6	0	-
7	0	-

4. (a) Information may be conveyed from Computer A to Computer B via a communication link as shown in Figure Q4a. Serial and parallel standards have been devised to enable the communication.

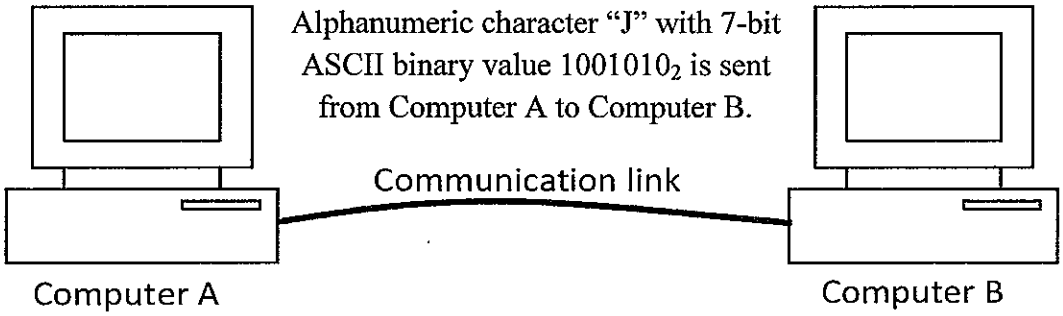

Figure Q4a

(i) Describe an advantage AND a disadvantage of serial data transfer when compared with parallel data transfer.

(4 marks)

(ii) The alphanumeric character "J" (with ASCII binary value 1001010_2) is sent from Computer A to Computer B using RS232 with the following data format:

Bits per second: 4800
Start bit: 1
Data bits: 8
Even Parity: 1
Stop bit: 1
Flow control: None

Determine the maximum transfer rate in characters per second (cps) and draw the expected waveform that will be observed on the transmit line of the RS232 interface on Computer A. Indicate clearly in your diagram the direction of the time axis.

(6 marks)

Note: Question No. 4 continues on Page 6

(b) A VIP assembly language program is shown in Figure Q4b and the initial states of registers `R1` and `R2` are shown in Figure Q4c. Consider a VIP processor organization with 4 pipeline stages: Fetch Instruction (F), Decode (D), Execute (E) and Store (S).

```
MOV   R0,R1        ; Load R0 with R1  (I1)
UMUL  R2           ; R1:R0 = R0 × R2  (I2)
```

Figure Q4b

Figure Q4c

With reference to Figure Q4b and Figure Q4c, answer the following questions.

(i) Data dependency between instructions (`I1`) and (`I2`) can lead to pipeline conflict. Explain what causes this data dependency.

(2 marks)

(ii) Describe one method to resolve the pipeline conflict between instructions (`I1`) and (`I2`). With the help of a pipeline diagram, illustrate how the pipeline conflict is resolved.

(5 marks)

(iii) Instruction (`I2`) in Figure Q4b performs an unsigned multiplication operation. Based on the initial states of registers in Figure Q4c, identify the multiplicand and multiplier values for instruction (`I2`) and their 6-bit binary representation (unsigned integer). Illustrate how the multiplication is achieved with the Booth algorithm.

Note: You must clearly show the intermediate values that are used to derive the result of the multiplication. You only need to illustrate the multiplication for generating the lower order 12-bit result.

(8 marks)

Appendix 1

VIP Instruction Set Summary Chart

VIP Instruction Encoding – Opcode Formats

11	10	9	8	7	6	5	4	3	2	1	0
0-7	Dual operand			d				s			
8	Short Move			d				n			
9-A	Unary/Control			op-code				operand = s, d or n			
B-F	JMP			2's complement -128 to +127 *relative*							

Group 1 – Dual-Operand Instructions (Opcode: 000 to 8FF)

Bits 8-11	Name	Bits 4-7	Bits 0-3	Operation	Flags
0	MOV	d	s	d ← s	NZ
1	AND	d	s	d ← d .AND. s	NZ
2	OR	d	s	d ← d .OR. s	NZ
3	EOR	d	s	d ← d .EOR. s	NZ
4	ADD	d	s	d ← d + s	VNZC
5	ADDC	d	s	d ← d + s + carry	VNZC
6	SUB	d	s	d ← d + (.NOT. s) + 1	VNZC
7	CMP	d	s	d + (.NOT. s) + 1	VNZC
8	MOVS	d	n	d ← n	

Group 2 – Unary and Control Instructions (Opcode: 900 to 9FF)

Bits 4-7	Name	Bit 0-3	Operation	Flags
0	INC	d	d ← d + 1	C
1	DEC	d	d ← d + 0xFFF	NZC
2	ROR	d	Rotate d right : msb ← lsb; and C ← lsb	NZC
3	ROL	d	Rotate d left : lsb ← msb; and C ← msb	NZC
4	RRC	d	Rotate d right including carry	NZC
5	RLC	d	Rotate d left including carry	NZC
6	RAR	d	Rotate d 'arithmetic' right preserving msb	NZC
7	PRSG	d	Left shift lsb from EOR (bits 11,5,3,0)	NZC
8	INV	d	d ← .NOT. d	NZ
9	NEG	d	d ← (.NOT. d) + 1	NZC
A	DADD	s	AR ← AR + s + carry (as 3 BCD digits)	ZC
B	UMUL	s	R1:R0 ← unsigned R0 times unsigned s	Z
C	TST	s	s + 0	NZ
D	EXEC	s	Execute s as an instruction	implied
E	BCSR	n	SR (bits 3-0) ← SR .AND. (.NOT. n)	explicit
F	BSSR	n	SR (bits 3-0) ← SR .OR. n	explicit

Group 3 – Unary and Control Instructions (Opcode: A00 to AFF)

Bits 4-7	Name	Bits 0-3	Operation	Flags
0	PSH	s	SP ← SP-1; (SP) ← s	
1	POP	d	d ← (SP); SP ← SP+1	explicit if d=SR
2	PSHM	3:2:1:0	Push R3:2:1:0 to stack, R3 first	
3	POPM	3:2:1:0	Pop R3:2:1:0 from stack, R3 last	
4	CALL	s	SP ← SP-1; (SP) ← Return Address PC ← Effective address	
5	RET	n	PC ← (SP) + n; SP ← SP+1	
6			See subgroup 3a	
7	RCN	n	Count for next rotate instruction. if n=0 use bits 3:2:1:0 of AR	
8	JDAR	±n	AR ← AR-1, if AR != 0, PC ← PC ± n	
9	JPE	±n	If parity of AR is even, PC ← PC ± n	
A	JPL	±n	If N = 0, PC ← PC ± n	
B	JVC	±n	If V = 0, PC ← PC ± n	
C	JGE	±n	If N = V, PC ← PC ± n	
D	JLT	±n	If N != V, PC ← PC ± n	
E	JGT	±n	If Z = 0 and N = V, PC ← PC ± n	
F	JLE	±n	If Z = 1 or N != V, PC ← PC ± n	

Group 1 – Jump Instructions (8-bit Range) (Opcode: B00 to FFF)

Bits 8-11	Name	n = Bits 0 to 7	Operation
B	JMP = BRA	-128 to +127	PC ← PC ± n
C	JEQ = JZ	-128 to +127	If Z=1, PC ← PC ± n
D	JNE = JNZ	-128 to +127	If Z=0, PC ← PC ± n
E	JHS = JC	-128 to +127	If C=1, PC ← PC ± n
F	JLO = JNC	-128 to +127	If C=0, PC ← PC ± n

Group 3a – Control Instructions (Opcode: A60 to A6F)

Bits 4-7	Name	Bits 0-3	Operation
6	RETI	0	SR ← (SP); SP ← SP+1; PC ← (SP); SP ← SP+1
6	SWI	1	SP ← SP-1; (SP) ← PC; SP ← SP-1; (SP) ← SR; PC ← (0x009)
6	WAIT	2	IE ← 1; Execution resumes after interrupt signal
6	HALT	3	Stop execution. Non-maskable interrupt or hardware reset to exit.
6	STOP	4	Stop execution. Reset to exit.
6	SYNC	8	Pulse SYNC output pin high for 1 clock cycle
6	NOP	9	No operation
6	LOCK	A	Block interrupts and bus sharing
6	UNLK	B	Allow interrupts and bus sharing
6	MSS	C to F	Memory Space Select override

Addressing Modes

Hex	Symbol	Location of Data	Availability
0	R0	Register R0	Both d and s
1	R1	Register R1	Both d and s
2	R2	Register R2	Both d and s
3	R3	Register R3	Both d and s
4	[R0]	Register R0 indirect	Both d and s
5	[R1]	Register R1 indirect	Both d and s
6	[R2+n]	Register R2 with offset indirect	Both d and s
7	[R3+n]	Register R3 with offset indirect	Both d and s
8	AR	Data is in Auxiliary Register	Both d and s
9	SR	Status Register	Both d and s
A	SP	Stack Pointer	Both d and s
B	PC	Program Counter	Both d and s
C	#n	Immediate, (or just n for CALL)	s only
D	[n]	Absolute (code space for CALL)	Both d and s
E	[SP+n]	SP with offset indirect	Both d and s
F	[PC+n]	PC with offset indirect (CALL is relative with PC+n)	Both d and s

Notation: d = destination; s = source

Description of bits in Status Register

SR	F	R	Description
11-8	*	*	Reserved
7-4	*	*	Defined but not described here
3	V	0	Set if 2's complement sign is incorrect
2	N	0	Is most significant bit of result
1	Z	0	1 if result is zero, otherwise 0
0	C	0	1 if carry out, otherwise 0

Notation: SR=Bits in register; F=Name of flag; R=Value after reset

END OF PAPER

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3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.