

NANYANG TECHNOLOGICAL UNIVERSITY**SEMESTER 2 EXAMINATION 2011-2012****CE1006/CZ1006 – COMPUTER ORGANISATION AND ARCHITECTURE**

April/May 2012

Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 6 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. All questions carry equal marks.

1. Computers store numbers in many different ways, including signed and unsigned integers, Q-format (fractional format), and using IEEE754 representation.

- (a) Determine the 6-bit binary result when the two's complement representation of decimal values 5 and -5 are fed into an ALU which is set to perform an AND operation. Note which of the flags N, Z, C and V are set when the operation completes. Repeat for EOR and ADD.

(9 marks)

- (b) Calculate how many bits the 8-bit immediate value 0x7E needs to be rotated right within a 32-bit register to produce the value 0xF800 0001. State why the ARM needs to use this kind of procedure to load a large immediate number (such as the one shown) into a register.

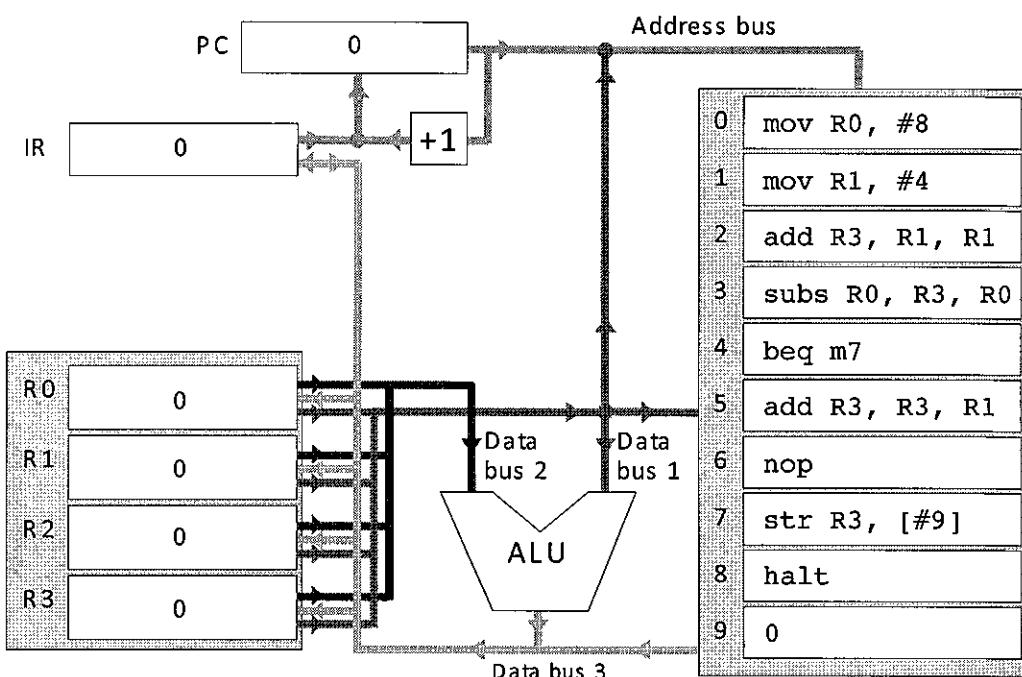
(7 marks)

- (c) IEEE754-1985 defines single and double precision floating point numbers of size 32-bits and 64-bits, respectively. Show how the decimal value 56 can be stored in single precision IEEE754 format.

(9 marks)

2. A simple CPU with ARM-style instructions is shown in Figure Q2a. The #n indicates an immediate value, and [#n] an absolute memory address. The instruction b m5 would branch to the instruction at memory location 5, and 'halt' ends the execution.
- (a) Construct a table as shown in Table Q2b that will trace through the operation of this CPU beginning in the state shown in Figure Q2a. In each row, record the state of the CPU after executing the current instruction. For your convenience, the first row has been completed.

(10 marks)

**Figure Q2a****Table Q2b**

Instruction	PC	R0	R1	R3
mov R0, #8	1	8	0	0

- (b) Briefly explain the purpose of the connection leading from the IR to the PC in Figure Q2a. State during which instruction (if any) it will be active.

(3 marks)

Note: Question No. 2 continues on Page 3

- (c) Does the arrangement of the link discussed in Q2(b) imply that either absolute or PC-relative branching is used? (4 marks)
- (d) By noting the limitations imposed by the direction arrows shown on the various buses in Figure Q2a, state whether this CPU would be able to execute the following instructions in a single clock cycle.
- (i) add R0, [#9], [#8]
 - (ii) sub [#9], R1, R2
 - (iii) mov R0, #10
 - (iv) add R0, R1, #5
- (8 marks)
3. (a) A processor has a pipeline with three stages: fetch instruction (FI), decode instruction (DI) and execute instruction (EI). Assume that each stage will take 1 unit of time and that all instructions go through the three stages.
- (i) With the aid of a timing diagram, determine the minimum units of time required for the processor to complete a sequence of 4 consecutive instructions. State any assumptions made.
- (6 marks)
- (ii) Determine the total units of time required for the processor to complete a sequence of 4 consecutive instructions if the pipeline is disabled.
- (2 marks)
- (b) List two differences in the characteristics between a read-only memory (ROM) and a random-access memory (RAM). Explain why most computer systems would have both these types of memory.
- (4 marks)

Note: Question No. 3 continues on Page 4

- (c) What is the difference between DRAM and SRAM in terms of characteristics such as speed, capacity and cost? (3 marks)
- (d) Table Q3a shows a page table for a logical address space (composed of 8 pages of 1024 bytes each) mapped into 4096 bytes of physical address space. With reference to Table Q3a, answer the following questions assuming that all numbers are decimal, everything is numbered starting from 0 and all addresses are memory byte addresses.
- (i) How many bits are required to store the page frame number for each entry of the page table? (2 marks)
 - (ii) Explain the possible use of the ‘Valid bit’ and the ‘Modify bit’ in the page table. (4 marks)
 - (iii) Complete the table started in Table Q3b to indicate the corresponding physical address, if any, for each of the virtual addresses listed. If necessary, indicate whether a page fault has occurred. (4 marks)

Table Q3a

Virtual Page Number	Valid bit	Modify bit	Page Frame Number
0	1	1	3
1	0	0	-
2	1	0	2
3	0	0	-
4	1	1	1
5	0	0	-
6	1	0	0
7	0	0	-

Table Q3b

Virtual Address	Physical Address
0	
1234	
3001	
6789	

4. (a) Figure Q4a shows a waveform captured from the output of an RS-232 port.

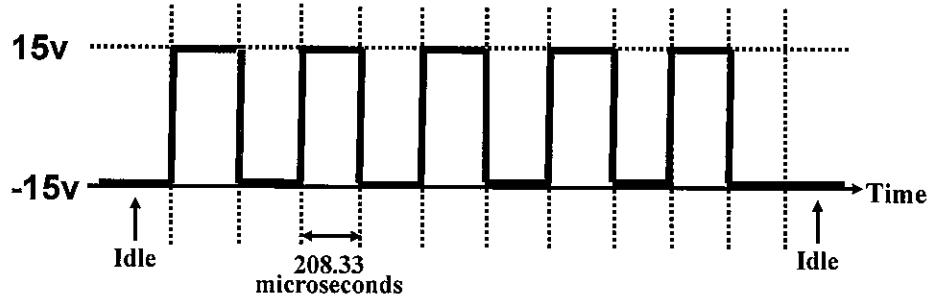


Figure Q4a

Table Q4b

LS \ MS	0	1	2	3	4	5	6	7
0	NUL	DLE	SP	0	@	P	'	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	\$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	'	7	G	W	g	w
8	BS	CAN	(8	H	X	h	x
9	HT	EM)	9	I	Y	i	y
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[k	{
C	FF	FS	/	<	L	\	l	
D	CR	GS	-	=	M]	m	}
E	SO	RS	.	>	N	^	n	
F	SI	US	/	?	O	—	o	DEL

- (i) Assume that one character was received error-free with the parity bit enabled. Specify the asynchronous serial data format and the baud rate used by this RS-232 interface.

(5 marks)

Note: Question No. 4 continues on Page 6

- (ii) Using the ASCII table shown in Table Q4b, state the ASCII character transmitted, assuming that the least-significant bit is transmitted first.

(2 marks)

- (iii) Calculate the data transfer rate of this RS-232 interface in characters per second (cps).

(2 marks)

- (iv) Re-compute Q4(a)(iii) if the parity bit is now disabled. Discuss what has been sacrificed for this gain in transfer rate.

(4 marks)

- (b) A magnetic hard disk has 16 recording surfaces with a total of 12,000 cylinders. There is an average of 300 sectors per track and each sector contains 512 bytes of data. The hard disk operates with a rotational speed of 5400 rpm and has a 6 ms average seek time. The average size of a block being accessed is 32 Kbytes and each data block is stored in consecutive sectors. Answer the following questions regarding this hard disk and show the calculations performed to obtain your answers.

- (i) What is the maximum number of bytes that can be stored on this hard disk?

(2 marks)

- (ii) What is the average data transfer rate (in bytes per second) for accessing consecutive data blocks on the same track?

(2 marks)

- (iii) What is the average percentage of the total time occupied by the seek and rotational delays for accessing a random data block on the hard disk?

(6 marks)

- (iv) Using an additional hard disk with similar properties, which RAID configuration would improve the fault tolerance of the array?

(2 marks)

END OF PAPER

NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2012-2013

CE1006/CZ1006 – COMPUTER ORGANIZATION AND ARCHITECTURE

Nov/Dec 2012

Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 5 pages.
 2. Answer **ALL** questions.
 3. This is a closed-book examination.
 4. All questions carry equal marks.
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1. (a) Consider ARMv5 processor architecture and its instruction set.
 - (i) Why can we not use a 32-bit absolute address in ARMv5 architecture?
 - (ii) Write a single assembly instruction that will set register (*R1*) to zero, without using a MOV or SUB instruction.
 - (iii) What is meant by the term “bus” in the context of the design of a computer architecture and state its purpose?
 - (iv) The 32-bit number H'12345678 is held in (byte addressed) memory using the big Endian method starting at memory location H'00001000. What hexadecimal number is held in memory location H'00001002.
 - (v) What is meant by the term PC-relative addressing? When is this addressing mode used?

(10 marks)

Note: Question No. 1 continues on Page 2

- (b) Identify the addressing mode of each of the following instructions and explain their operations. Assume ARMv5 processor instruction set.
- (i) ADD R1, R1, #100
 - (ii) STR R0, [R5, #5]
 - (iii) ADD R1, R2, R3
 - (iv) BL fn3
 - (v) LDR R0, #0x100
- (15 marks)
2. (a) Find the IEEE754 single precision format representation of the decimal number 10.75. Note that IEEE754-1985 uses 32 bits to represent a single precision number.
(9 marks)
- (b) Which of the following Q-formats - Q1.4 or Q1.7 - represents a decimal number 0.78125 accurately? Provide the bit pattern for both formats.
(6 marks)
- (c) The following machine code 0xE3A00C01 in ARMv5 architecture loads a 32-bit constant in register R0. Identify the decimal value of the constant stored in register R0.
(6 marks)
- (d) Explain Flynn's Taxonomy of computer architecture.
(4 marks)

3. (a) State the advantages and disadvantages of the polled I/O data transfer technique and the interrupt driven I/O data transfer technique.

(6 marks)

- (b) Figure Q3 shows the pin layout of a simple microprocessor (μ P), a SRAM and a PROM chip. All control signals (**RD**, **WR**, **CS**, etc) are active-high. The microprocessor can be configured to support memory access with or without the use of the **CAS/RAS** control signals.

With reference to Figure Q3, answer the following questions.

- (i) What is the total memory space (*in bytes*) supported by the microprocessor if the **CAS/RAS** control signals are NOT used for accessing the memory?

(2 marks)

- (ii) What is the total memory space (*in bytes*) supported by the microprocessor if the **CAS/RAS** control signals are used for accessing the memory?

(2 marks)

- (iii) What is the memory capacity (*in bits*) of the SRAM and PROM chips?

(4 marks)

- (iv) Explain the reason why there is no **WR** control pin on the PROM chip.

(2 marks)

- (v) A microprocessor needs to be configured such that addresses **0x0** to **0x3** are used to store temporary data and addresses **0x4** to **0x7** are used to store program codes. Using the PROM and the SRAM chips, draw a circuit diagram to show the interconnections between the microprocessor and the required memory chips.

(9 marks)

Note: Question No. 3 continues on Page 4

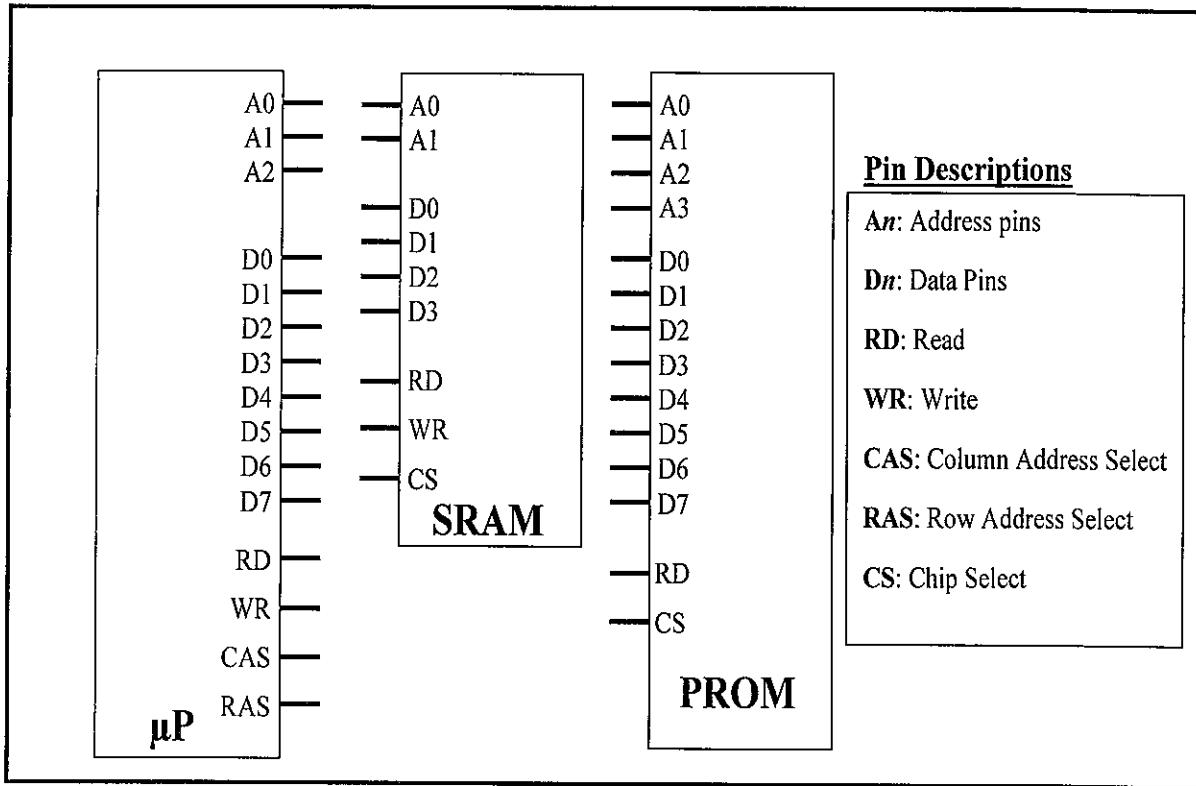


Figure Q3

4. (a) State at least one advantage and one disadvantage of using serial data transfer when compared to using parallel data transfer.
(4 marks)

- (b) An asynchronous RS-232 serial port has a baud of 2400. Assuming that the port is transmitting 7-bit ASCII characters, determine the maximum transfer rate (in characters per second) that is achievable? State the asynchronous serial data format that is used to achieve this.
(4 marks)

- (c) Table Q4 shows the properties of two magnetic hard disks, **HD_A** and **HD_B**, which are used in a computer system. Assume that the average size of a block being accessed is 32 Kbytes and each data block is stored in consecutive sectors.

Note: Question No. 4 continues on Page 5

Table Q4

Specification	HD_A	HD_B
Number of recording surfaces	16	16
Total number of cylinders	6000	6000
Sectors per track	600	300
Bytes per sector	512	512
Rotational Speed (rpm)	4800	5400
Average Seek Time (ms)	6	6

With reference to the specifications stated in Table Q4, answer the following questions regarding the hard disks and show the calculations performed to obtain your answers:

- (i) Calculate the capacities of the hard disks and state which hard disk has the greater capacity? (5 marks)
- (ii) A computer salesman claims that "*a hard disk with a faster rotational speed has a higher average data transfer rate than a hard disk with slower rotational speed*". By comparing HD_A and HD_B, explain if this claim is always true. (6 marks)
- (d) A processor has a pipeline with four stages: fetch instruction (**F**), decode instruction (**D**), compute (**C**) and write result (**W**). Given that each stage will take 1 unit of time and all instructions go through the four stages, determine the minimum units of time required for the processor to complete a sequence of 3 consecutive instructions with the aid of a timing diagram. State any assumptions made. (6 marks)

END OF PAPER

NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 2 EXAMINATION 2012-2013

CE1006/CZ1006 – COMPUTER ORGANIZATION AND ARCHITECTURE

Apr/May 2013

Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 7 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. All questions carry equal marks.
5. The VIP Instruction Set Summary Chart is provided in Appendix 1 on page 7.

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1. Figure Q1a shows the hexadecimal contents of several registers in the VIP processor and a section of its memory.

		MEMORY
Address	Content	
R0	0x803	R1 0x212
R2	0x102	R3 0x005
AR	0x000	SP 0xFFC
SR	0x000	PC 0x030
Note:	Bit no. 11 4 3 2 1 0 SR [] V N Z C	: : 0x100 0x123 0x101 0x867 0x102 0xF22 0x103 0x000 0x104 0x129 : : 0xFFB 0xFEE 0xFFC 0x005 0xFFD 0x004 0FFE 0x126 0FFF 0x000
	Condition Code flags	

Figure Q1a

Note: Question No. 1 continues on Page 2

- (a) Give (*in hexadecimal*) the 12-bit contents in the two registers **R0** and **SR**, *immediately after* the execution of each instruction given below.

Note: Instructions (i) to (vi) are **not consecutive instructions**. You must use the initial conditions shown in Figure Q1a to derive your answer for each of the instructions given below.

- (i) MOV R0, R3
- (ii) MOV R0, #0xFFFF
- (iii) MOV R0, [R2+1]
- (iv) RAR R0
- (v) EOR R0, R1
- (vi) POPM 3

(12 marks)

- (b) With reference to the VIP assembly language program in Figure Q1b, give (*in hexadecimal*) the 12-bit contents of registers **R0**, **R1** and **R2** **after** the execution of the instruction at the address label **DONE**. Assume execution of the given series of consecutive instructions begins at the label **START**.

Note: The instructions **JGT SKIP** and **JPL LOOP** will be assembled with the appropriate relative offset that will allow each instruction to jump to the respective address labels indicated.

(9 marks)

START	MOV	R0, #2
	MOV	R1, #4
	MOV	R2, R0
LOOP	CMP	R1, R0
	JGT	SKIP
	ADD	R2, R2
SKIP	NEG	R1
	DEC	R0
	JPL	LOOP
	DEC	R0
DONE	ADDC	R2, R2

Figure Q1b

- (c) A VIP instruction with the mnemonic **CALL 0x020** is stored at the starting address of **0x020**. Describe clearly what will happen when this instruction is executed.

(4 marks)

2. (a) A VIP assembly language program and the contents of several registers and memory variables are given in Figure Q2a. Give the mnemonics of (I1), (I2), (I3), (I4) and (I5) that will complete the missing instructions based on their associated comments. (8 marks)

Figure Q2a

- (b) Draw a labeled memory map to show all the known contents on the system stack immediately after the execution of the **PSHM 3** instruction at (**S1**). Your diagram must include (*in hexadecimal*) the stack addresses and their respective contents. Assume the program given in Figure Q2a begins execution at the address label **Main**. (8 marks)

(c) The subroutine **Sub1** implements the C language code given in Figure Q2b. Complete the remaining portion of subroutine **Sub1** based on the way the parameters **VarA**, **VarB** and **VarC** have been passed in Figure Q2a. Based on your solution, state clearly what assumption you have made regarding the nature of the three variables **VarA**, **VarB** and **VarC**. (9 marks)

```
if (VarA >= VarB)
    VarC = VarA + VarB;
else
    VarC = VarA - VarB;
```

Figure Q2b

3. (a) With reference to computer memory, state the key difference between volatile and non-volatile memory. For each memory device listed below, determine if the device is volatile or non-volatile. Briefly describe the working principle that enables the device to store information.
- (i) Magnetic hard-disk
(ii) Compact Flash (CF) card
(iii) Digital Video Disc (DVD)
- (11 marks)
- (b) Computer systems employ input/output (I/O) control methods that include programmed I/O, interrupt-driven I/O and direct memory access. Among these three I/O control methods, state which is the most suitable to process each of the I/O device listed below. In each case, provide justifications for your choice.
- (i) Mouse input device
(ii) Digital Video Disc (DVD) player
- (6 marks)
- (c) Table Q3a shows a page table for a virtual address space (composed of 8 pages of 512 bytes each) mapped into 2048 bytes of physical address space. Assume all addresses are memory byte addresses starting from zero. For each of the hexadecimal virtual addresses (00000_{16} , 00202_{16} , 00640_{16} and 00808_{16}), find the corresponding virtual page number and indicate its physical address (*in hexadecimal*), if any. Indicate clearly for cases where a page fault will occur.
- (8 marks)

Table Q3a

Virtual Page Number	Valid Bit	Page Frame Number
0	1	3
1	1	2
2	1	1
3	0	-
4	0	-
5	1	0
6	0	-
7	0	-

4. (a) Information may be conveyed from Computer A to Computer B via a communication link as shown in Figure Q4a. Serial and parallel standards have been devised to enable the communication.

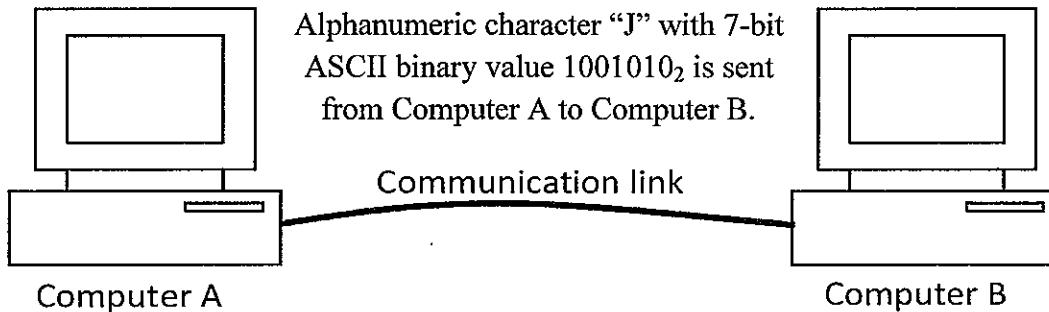


Figure Q4a

- (i) Describe an advantage AND a disadvantage of serial data transfer when compared with parallel data transfer. (4 marks)
- (ii) The alphanumeric character "J" (with ASCII binary value 1001010_2) is sent from Computer A to Computer B using RS232 with the following data format:

Bits per second: 4800

Start bit: 1

Data bits: 8

Even Parity: 1

Stop bit: 1

Flow control: None

Determine the maximum transfer rate in characters per second (cps) and draw the expected waveform that will be observed on the transmit line of the RS232 interface on Computer A. Indicate clearly in your diagram the direction of the time axis. (6 marks)

Note: Question No. 4 continues on Page 6

- (b) A VIP assembly language program is shown in Figure Q4b and the initial states of registers R1 and R2 are shown in Figure Q4c. Consider a VIP processor organization with 4 pipeline stages: Fetch Instruction (F), Decode (D), Execute (E) and Store (S).

MOV R0, R1	; Load R0 with R1 (I1)
UMUL R2	; R1:R0 = R0 × R2 (I2)

Figure Q4b

R1 0x031 R2 0x018

Figure Q4c

With reference to Figure Q4b and Figure Q4c, answer the following questions.

- (i) Data dependency between instructions (I1) and (I2) can lead to pipeline conflict. Explain what causes this data dependency.
(2 marks)
- (ii) Describe one method to resolve the pipeline conflict between instructions (I1) and (I2). With the help of a pipeline diagram, illustrate how the pipeline conflict is resolved.
(5 marks)
- (iii) Instruction (I2) in Figure Q4b performs an unsigned multiplication operation. Based on the initial states of registers in Figure Q4c, identify the multiplicand and multiplier values for instruction (I2) and their 6-bit binary representation (unsigned integer). Illustrate how the multiplication is achieved with the Booth algorithm.

Note: You must clearly show the intermediate values that are used to derive the result of the multiplication. You only need to illustrate the multiplication for generating the lower order 12-bit result.

(8 marks)

NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2013-2014

CE1006/CZ1006 – COMPUTER ORGANIZATION AND ARCHITECTURE

Nov/Dec 2013

Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 7 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. All questions carry equal marks.
5. The VIP Instruction Set Summary Chart is provided in Appendix A.

-
1. Figure Q1a shows the hexadecimal contents of several registers in the VIP processor and a section of its memory.

MEMORY Address	Content
:	:
0x100	0x456
0x101	0x877
0x102	0xF22
0x103	0x889
0x104	0x339
:	:
0xFFB	0xCDE
0xFFC	0x106
0xFFD	0xF44
0xFFE	0x023
0xFFF	0xFF0

R0 0x102 **R1** 0x800

R2 0x801 **R3** 0x005

AR 0x000 **SP** 0xFFFF

SR 0x001 **PC** 0x020

Note: Bit no. 11 4 3 2 1 0

Condition Code flags

SR [] | V | N | Z | C |

Figure Q1a

Note: Question No. 1 continues on Page 2

- (a) Give (*in hexadecimal*) the 12-bit contents in the two registers **R1** and **SR**, *immediately after* the execution of each instruction given below.

Note: Instructions (i) to (vi) are **not consecutive instructions**. You must use the initial conditions shown in Figure Q1a to derive your answer for each of the instruction given below.

- (i) **MOV R1, #0**
- (ii) **MOV R1, [R0]**
- (iii) **ADD R1, R2**
- (iv) **RLC R1**
- (v) **AND R1, [0x103]**
- (vi) **POP R1**

(12 marks)

- (b) Write the equivalent C high-level language program that is represented by the VIP assembly language program given in Figure Q1b. You may assume that your C integer variables **Var0**, **Var1**, **Var2**, **Var3** and **Var4** are represented by the memory addresses given by labels **Var0**, **Var1**, **Var2**, **Var3** and **Var4** respectively in Figure Q1b.

Start	MOV	[Var4], #0
	CMP	[Var2], [Var3]
	JGE	Label_1
	MOV	[Var1], #6
	JMP	Label_2
Label_1	MOV	[Var1], #4
Label_2	MOV	[Var0], #10
Label_3	CMP	[Var0], #0
	JEQ	Label_4
	ADD	[Var4], [Var1]
	DEC	[Var0]
	JMP	Label_3
Label_4	MOV	[Var2], [Var4]

Figure Q1b

(10 marks)

- (c) Give a reason why some instruction set architecture (ISA) designs have adopted the Load-Store architecture?

(3 marks)

2. (a) With reference to the VIP assembly language program shown in Figure Q2, describe whether the parameter for memory variable **Data1** is passed to the subroutine `OddParity` by value or by reference. Give a reason for your answer.

(4 marks)

Address			
0x000	Main	MOV SP, #0xFFFF	; Initialize stack pointer (I1)
0x002		PSH #0x100	; Push parameter to stack (I2)
0x004		CALL OddParity	; Call subroutine to insert odd parity bit (I3)
0x006		?	; Remove stack parameter (I4)
0x008	:		

Address	Contents
Data1 0x100	0x111
0x101	:
0x102	:

Address	Contents
Data1 0x100	0x911
0x101	:
0x102	:

Before Entering Subroutine

After Returning from Subroutine

Figure Q2

- (b) To pass an odd parity error check, the number of binary ones in the 12-bit data word must be odd. To ensure this happens, all occurrences of binary ones in the least significant 11 bits in the word are counted and if the tally is an even number, the most significant bit (MSB) in the word is set to one, otherwise it is cleared to zero.

Write a VIP assembly language subroutine labeled `OddParity` to perform the odd parity encoding to a 12-bit memory variable. Figure Q2 shows how the single parameter is to be passed into the subroutine and the effect of the `OddParity` subroutine upon returning to the calling program. Your solution must ensure the subroutine is transparent.

(16 marks)

- (c) With reference to Figure Q2, give two different VIP mnemonics that can be used to remove the parameter from the stack. Explain clearly which is the preferred choice and why this is so.

(5 marks)

3. (a) Figure Q3a shows a 6-T SRAM cell.

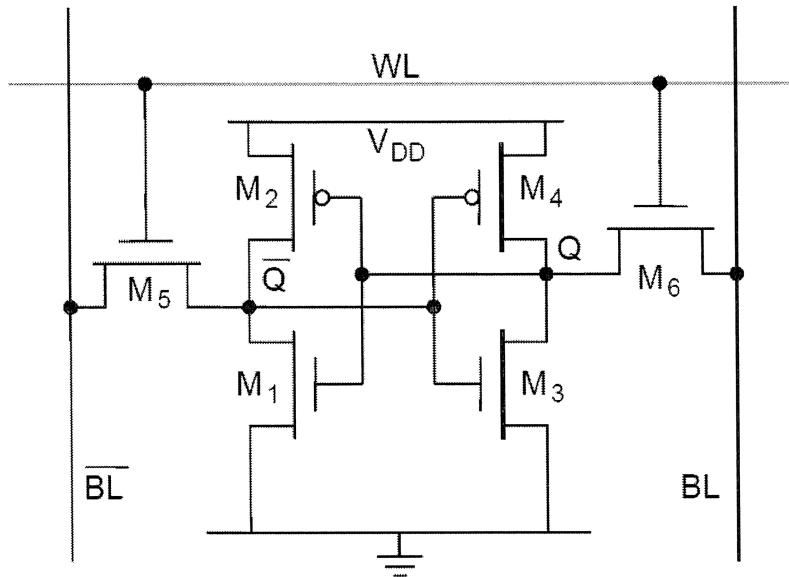


Figure Q3a

- (i) Explain whether the SRAM cell is **volatile** or **non-volatile**. (3 marks)
- (ii) An SRAM device has 20-bit address bus and 16-bit data bus. How many memory locations and SRAM cells are there? (4 marks)
- (iii) Briefly describe the operations of the circuits in Figure Q3a for READ and WRITE access of the SRAM cell. (4 marks)
- (b) SRAM memory is often implemented as **cache memory** in computer systems.
- (i) What is **cache memory** and what are its main purposes? (4 marks)

Note: Question No. 3 continues on Page 5

- (ii) An observation table for several direct-mapped cache memory accesses is shown in Table Q3b. The address reference strings are provided as hexadecimal numbers and the order of memory access starts from **3F8** and ends at **2EA**.

For each of these address reference strings,

- give the value of the binary bits in the Tag, Block and Word fields.
- state whether each cache memory access registers a hit or a miss, and if the cache content is replaced.

Assume the cache memory is initially empty. You may use a table similar to Table Q3b to present your answers.

(10 marks)

Table Q3b

Direct-Mapped Cache Memory					
Address Reference String (Hex)	Main Memory Address			Cache Access (Hit/Miss?)	Cache Replace (Yes/No?)
	Tag (2 bits)	Block (4 bits)	Word (4 bits)		
3F8					
3F3					
3E2					
2E2					
2EA					

4. (a) An engineer would like to transfer data periodically from a data logger to a computer using direct interfacing.
- (i) Should he consider using serial or parallel data transfer? List three key considerations and discuss their respective impact on his decision.

(9 marks)

He eventually decides to use the RS-232 protocol shown in Figure Q4. The clock period used in the data transfer is 1 μ s. With reference to this decision, answer the following questions:

Note: Question No. 4 continues on Page 6

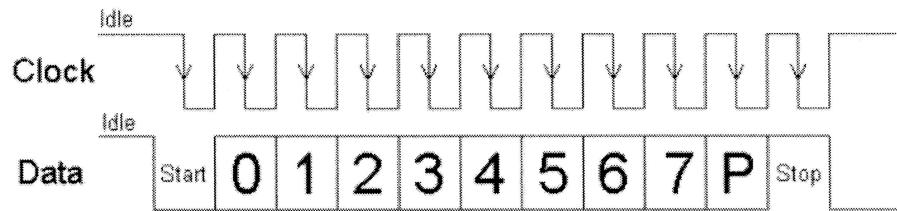


Figure Q4

- (ii) What is the theoretical maximum data transfer rate?
(4 marks)
- (iii) If the data logger needs to send 1 megabyte (MB) of data every 10 ms, discuss whether the engineer has made a correct choice in selecting the RS-232 protocol.
(4 marks)
- (b) Using any of the **Rotate** instructions in the VIP Instruction Set given in Appendix A, write a VIP assembly code segment that will multiply the unsigned content in register **R0** by the constant value 3. Your 12-bit result should reside in register **R0** after the multiplication.
(4 marks)
- (c) It is suggested register **R0** may represent a real number with value 2.611 using fixed floating-point representation where the unsigned integer has 5 bits and the fractional value has 7 bits. Determine the 12-bit hexadecimal value that is stored in register **R0** and the smallest incurred rounding error.
(4 marks)

NANYANG TECHNOLOGICAL UNIVERSITY**SEMESTER 2 EXAMINATION 2013-2014****CE1006/CZ1006 – COMPUTER ORGANIZATION AND ARCHITECTURE**

April/May 2014

Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 7 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. All questions carry equal marks.
5. The VIP Instruction Set Summary Chart is provided in Appendix 1 on page 7.

1. Figure Q1a shows the hexadecimal contents of several registers in the VIP processor and a section of its memory.

		MEMORY	
Address	Content		
R0	0xFFB	R1	0xFEF
R2	0x101	R3	0x000
AR	0x002	SP	0xFFD
SR	0x000	PC	0x000
Note:		Bit no. 11 4 3 2 1 0 SR [] V N Z C Condition Code flags	
		:	:
		0x100	0x000
		0x101	0x777
		0x102	0xE2E
		0x103	0x123
		0x104	0x000
		:	:
		0xFFB	0x81E
		0xFFC	0xFF1
		0xFFD	0x022
		0FFE	0xFFFF
		0FFF	0x000

Figure Q1a

Note: Question No. 1 continues on Page 2

- (a) Give (*in hexadecimal*) the 12-bit contents in the two registers **R1** and **SR**, *immediately after* the execution of each instruction given below.

Note: Instructions (i) to (vi) are **not consecutive instructions**. You must use the initial conditions shown in Figure Q1a to derive your answer for each of the instructions given below.

- (i) **MOV R1 , [0x104]**
- (ii) **MOV R1 , [R2+2]**
- (iii) **CMP R1 , [SP+0xFFFF]**
- (iv) **ADD R1 , #0x021**
- (v) **RAR R1**
- (vi) **AND R1 , [R0]**

(12 marks)

- (b) With reference to the VIP assembly language program in Figure Q1b, give (*in hexadecimal*) the 12-bit contents of the **seven** registers **R0**, **R1**, **R2**, **R3**, **PC**, **SP** and **SR** *after* the execution of the instruction at the address label **DONE**. Assume that the execution of the given series of consecutive instructions begins at the label **BEGIN**.

BEGIN	MOV	SP , #0xFF2
	MOV	SR , #0
	MOV	R0 , #0
	MOV	R1 , #2
	MOV	R2 , R0
	PSH	R1
	SUB	R2 , R1
	CMP	R0 , R1
	JGT	NEXT
	DEC	R0
NEXT	MOV	R3 , #0xFFE
	ROL	R3
	JPL	DONE
	SUB	PC , #4
DONE	RET	

Figure Q1b

(13 marks)

2. A VIP assembly language program and the contents of several memory variables are given in Figure Q2a.

- (a) Complete the mnemonics for instructions **(a1)** and **(a2)** based on their associated comments and the manner in which the parameters are passed within the calling program **Main**.

(6 marks)

Main	MOV SP, #0xFFFF ;	
	PSH [0x100] ;	
	PSH #0x101 ;	
	CALL SubX ;	
	:	
SubX	PSHM 7	;
	MOV R0, ?	; retrieve value of Var1 on the stack into R0 (a1)
	MOV R1, ?	; retrieve the address of Var2 on the stack into R1 (a2)
Loop	MOV R2, [R1]	;
	RRC R2	;
	JC ToDo	; (b1)
	JMP Done	; (b2)
ToDo	BCSR 1	; (b3)
	RLC R2	; (b4)
	MOV [R1], R2	; (b5)
	ADD R1, #1	; (b6)
	SUB R0, #1	; (b7)
	JNE Loop	;
Done	BSSR 1	;
	RLC R2	;
	MOV [R1], R2	;
	? ; (c1)	
	? ; (c2)	

Address	Contents
Var1 0x100	0x005
Var2 0x101	0xFFFF
Var3 0x102	0x111
Var4 0x103	0xCC
Var5 0x104	0x777

Figure Q2a

- (b) Re-write the code segment given by instructions **(b1)** to **(b7)** so that the loop body will be optimized. Marks will be awarded based on how well you have optimized the given code segment for both execution speed and code size.

(8 marks)

- (c) Give the mnemonics for the last two instructions **(c1)** and **(c2)** so that the subroutine **SubX** is completed correctly.

(4 marks)

- (d) Based on the memory variable values shown in Figure Q2a, give the 12-bit hexadecimal values of **Var1**, **Var2**, **Var3**, **Var4**, and **Var5** immediately after returning from the subroutine **SubX**. You may assume that the program execution begins at the label **Main**.

(7 marks)

3. (a) Considering only Redundant Array of Independent Disks (RAID) configurations 0, 1, 5 and 6, state for each part, (i) to (iii) shown below, which configuration provides the feature described. For each stated configuration, explain its basic working principle.
- (i) The RAID configuration has 0% disk redundancy. (4 marks)
- (ii) The RAID configuration has 100% disk redundancy. (4 marks)
- (iii) The RAID configuration can recover from more than one hard disk failure. (4 marks)
- (b) Figure Q3a shows a basic Sketch program used on the Arduino UNO R3 board to enable UART communication between the board and its interfacing computer.

```

void setup() {
    //Arduino serial configuration
    //19200 baud rate
    //1 start bit, 8 data bits
    //1 even parity bit, 1 stop bit
    Serial.begin(19200,SERIAL_8E1);

    //Print title with ending line break
    Serial.println("ASCII Table ~ Character Map");
}

//Initialize variable to ASCII character 'U'
int thisByte = 'U';

void loop() {
    Serial.write(thisByte);
    delay(1000);
}

```

Figure Q3a

Note: Question No. 3 continues on Page 5

- (i) The program is compiled and loaded onto the Arduino board. On the PC, the Arduino serial monitor program is started. Assume the software configurations are correct, describe clearly what are expected to be observed on the serial monitor program. (3 marks)
- (ii) The board is configured to send an 8-bit data packet with even parity. Determine the maximum data transfer rate in characters per second. (3 marks)
- (iii) The board may also be configured to send the same data packet with no parity. Using this configuration with no parity, determine the minimum baud rate setting needed to transfer at least 2950 characters per second. The supported baud rates are 19200, 28800, 38400 and 57600. Justify your answer. (5 marks)
- (iv) Describe what would be observed if the program shown in Figure Q3a is compiled and loaded, but with the whole **setup** routine omitted. (2 marks)
4. (a) A microprocessor system uses an embedded DMA controller to handle its data transfer with an I/O device. Given that the bus cycle takes 100ns, the transfer of the bus control between the CPU and the DMA controller takes 50 ns and the I/O device has a data transfer rate of 125 Kbyte/sec.
- (i) If burst-mode is used by the DMA controller, how long will it take to transfer a block of 10 Kbyte data? (5 marks)
- (ii) Repeat the calculation described in part (i) if the DMA controller is using the cycle-stealing mode. Assume that one byte is transferred in each cycle. (5 marks)

Note: Question No. 4 continues on Page 6

- (b) A VIP assembly language program is shown in Figure Q4a. Consider a VIP processor organization with 4 pipeline stages: Fetch Instruction (F), Decode (D), Execute (E) and Store (S).

ADD	R2 ,R1	; R2 = R2+R1 (I1)
RAR	R2	; R2 = R2÷ 2 (I2)
ADD	R3 ,R1	; R3 = R3+R1 (I3)
RAR	R3	; R3 = R3÷ 2 (I4)
ADD	R2 ,R3	; R2 = R2+R3 (I5)

Figure Q4a

- (i) Data dependency between instructions can lead to pipeline conflict. With the help of a pipeline diagram, identify one (or more) dependency between the instructions shown in Figure Q4a. Explain the cause of each identified data dependency.

(6 marks)

- (ii) Show how the instructions can be reordered to mitigate pipeline conflict (by writing down the improved program in the answer booklet). With the help of a pipeline diagram, illustrate how the pipeline conflict is mitigated.

(6 marks)

- (c) The Booth algorithm is to be used to multiply two numbers, namely 0x155 and 0x037. State your choice of multiplicand and multiplier that will result in the least number of operations. Give reasons for your choice. **There is no need to show the solution for the multiplication.**

(3 marks)

NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 2 EXAMINATION 2014-2015

CE1006/CZ1006 – COMPUTER ORGANIZATION AND ARCHITECTURE

Apr/May 2015

Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 7 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. All questions carry equal marks.
5. The VIP Instruction Set Summary Chart is provided in Appendix 1 on page 7.

-
1. Figure Q1a shows the hexadecimal contents of several registers in the VIP processor and a section of its memory.

		MEMORY	
Address	Content		
R0	0x8F1	R1	0x103
R2	0x991	R3	0x7EF
AR	0x003	SP	0xFFB
SR	0x000	PC	0x000
Note: Bit no. 11 4 3 2 1 0			
		SR	V N Z C
Condition Code flags			
:		:	:
0x100	0x333		
0x101	0x260		
0x102	0xFFA		
0x103	0x168		
0x104	0x000		
:	:		
0xFFA	0xEDD		
0xFFB	0x000		
0xFFC	0x846		
0xFFD	0xFFF		
0FFE	0x254		

Figure Q1a

Note: Question No. 1 continues on Page 2

- (a) Give (*in hexadecimal*) the 12-bit contents in the two registers **R2** and **SR**, immediately after the execution of each instruction given below.

Note: Instructions (i) to (vi) are **not consecutive instructions**. You must use the initial conditions shown in Figure Q1a to derive your answer for each of the instructions given below.

- (i) **MOV R2, #0xABCD**
- (ii) **MOV R2, [SP]**
- (iii) **OR R2, [R1]**
- (iv) **PSH R2**
- (v) **ADD R2, R0**
- (vi) **RRC R2**

(12 marks)

- (b) Write the equivalent C high-level language program that is represented by the VIP assembly language program given in Figure Q1b. You may assume that your C integer variables **Var0** and **Var1** are represented by the memory addresses given by labels **Var0** and **Var1** respectively in Figure Q1b.

(8 marks)

START	MOVS [Var0], #0
	MOV [Var1], #10
Label_1	JEQ Label_3
	CMP [Var1], #5
	JGE Label_2
	INC [Var0]
Label_2	DEC [Var1]
	JMP Label_1
Label_3	ADD [Var0], [Var0]

Figure Q1b

- (c) Using the initial conditions given in Figure Q1a and the information given in Appendix 1, give (*in hexadecimal*) the 12-bit contents in the two registers **R3** and **SR** immediately after the execution of the VIP instruction **ADD R3, [PC+0xFFFF]**.

(5 marks)

2. (a) An incomplete VIP assembly language program and the contents of several registers and memory variables are given in Figure Q2. Give the five mnemonics of (I1) to (I5) in the calling program and the six mnemonics of (S1) to (S7) in the subroutine that will complete the instructions based on their associated comments.

(14 marks)

Address																		
0x000	Main	MOV SP, #0xFFFF	; Initialize stack pointer															
0x002		?	; Push decimal value 4 (i.e. array size) to stack (I1)															
0x004		?	; Push start address of memory array KA to stack (I2)															
0x006		?	; Call subroutine SubZ (I3)															
0x008		?	; Copy result passed out to memory variable Ans (I4)															
0x00A		?	; Remove stack parameters (I5)															
:																		
0x050	SubZ	PSHM 0x00A	; Save away used registers															
		MOV R3, SP	; Setup frame pointer R3															
		SUB SP, #2	; Create 2 local variables V1 and V2 on stack frame															
		MOVS [R3+0xFFFF], ?	; Clear local variable V1 (S1)															
		MOV [R3+0xFFE], ?	; Move array size on stack into local variable V2 (S2)															
		MOV R1, ?	; Move start address of array on stack into R1 (S3)															
	Loop	ADD [R3+0xFFFF], ?	; Add next array element to local variable V1 (S4)															
		? ?	; Increment R1 (S5)															
		? ?	; Decrement local variable V2 (S6)															
		? ?	; Loop back until all array elements are added (S7)															
		MOV R0, [R3+0xFFFF]	; Move result of summation into R0 for passing out															
:			; to be completed															
:			; as specified in															
:			; question Q2(c)															
<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>R0</td><td>0xAAA</td> <td>R1</td><td>0xBBB</td> </tr> <tr> <td>R2</td><td>0xCCC</td> <td>R3</td><td>0xDDD</td> </tr> </table> Contents in Registers				R0	0xAAA	R1	0xBBB	R2	0xCCC	R3	0xDDD							
R0	0xAAA	R1	0xBBB															
R2	0xCCC	R3	0xDDD															
<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>Ans</td><td>0x100</td><td>0x000</td></tr> <tr> <td>KA</td><td>0x101</td><td>0x002</td></tr> <tr> <td></td><td>0x102</td><td>0x036</td></tr> <tr> <td></td><td>0x103</td><td>0x023</td></tr> <tr> <td></td><td>0x104</td><td>0x024</td></tr> </table> Contents in Memory				Ans	0x100	0x000	KA	0x101	0x002		0x102	0x036		0x103	0x023		0x104	0x024
Ans	0x100	0x000																
KA	0x101	0x002																
	0x102	0x036																
	0x103	0x023																
	0x104	0x024																

Figure Q2

- (b) Draw a labeled memory map to show all the known contents on the system stack immediately after the execution of the instruction at (S2). Your diagram must include (*in hexadecimal*) the stack addresses and their respective contents. Assume the program given in Figure Q2 begins execution at the address label **Main**.

(7 marks)

- (c) With reference to Figure Q2, give the sequence of VIP assembly language instructions that will allow subroutine **SubZ** to return to the calling program in a correct manner.

(4 marks)

3. (a) For each listed device in Table Q3, state if the memory is volatile or non-volatile. Also, categorize the device as either system or storage memory. Provide your answers using the table format given in Table Q3.

(6 marks)

Table Q3

Device	Volatile/Non-volatile	System/Storage Memory
NAND Flash		
Magnetic Hard Disk		
SRAM		

- (b) Describe what Execute-in-Place (XIP) means and explain why the NOR flash memory supports XIP.

(3 marks)

- (c) Which type of flash memory would you choose when designing high capacity USB Flash Drives for the consumer market? Give one reason for your choice.

(3 marks)

- (d) Figure Q3 shows a basic Sketch program used on the Arduino UNO R3 board to enable UART communication between the board and its interfacing computer.

```
void setup() {
    // 19200 baud rate
    // 1 start bit, 7 data bits
    // 1 even parity bit, 1 stop bit
    Serial.begin(19200,SERIAL_7E1);
}

//Initialize variable to 'y' (Ascii value = 0x79)
int thisByte = 'y';

void loop() {
    Serial.write(thisByte);
    delay(1000); // 1 Second Delay
}
```

Figure Q3

Note: Question No. 3 continues on Page 5

With reference to Figure Q3, answer the following questions:

- (i) What is the maximum number of characters that can be transmitted per second?

(3 marks)

- (ii) Draw the waveform of the UART signal transmitted by the Arduino Board running the given code. Label the START, STOP and PARITY bits.

(5 marks)

- (iii) A UART receiver is configured to receive the signal transmitted by the Arduino Board running the given code. Instead of data ‘0x79’, the receiver repeatedly received a data of ‘0x06’ at an interval of about 1 second. No error is detected by the UART receiver. Determine the UART configuration used in the receiver and give clear explanations for your answer.

(5 marks)

4. (a) State one advantage and one disadvantage for each of the following cache mapping scheme:

- Direct mapped cache.
- N-Way set associative cache.

(6 marks)

- (b) Explain why the code shown in Figure Q4a allows a cache to have a high hit rate.

(6 marks)

```
for (i=0; i<10; i++)
{
    a[i] = b[i]*c[i];
}
```

Figure Q4a

Note: Question No. 4 continues on Page 6

- (c) An array consisting of the length of 8 wires is given by $L[0], L[1], \dots, L[7]$. Describe a scheme to compute the average length of the 8 wires that will yield a result with the highest precision based on the following specifications:

- 12-bit registers are used for storing data and result.
- Only single-precision, fixed-point arithmetic is used.
- Maximum possible length of each wire is 0x3FF.

Give your answer in the form of a mathematical expression and justify your answer.

Note: you do not need to write any code.

(7 marks)

- (d) Consider a processor with 4 pipeline stages: Fetch Instruction (F), Decode (D), Execute (E) and Store (S). Figure Q4b shows the initial 12-bit hexadecimal contents of several registers in the processor and a program that is subsequently executed.

R0	0x00B	R1	0x005	ADD R1,R2 ;R1=R1+R2 (I1)
R2	0x003	R3	0x010	SUB R3,R1 ;R3=R3-R1 (I2)

Figure Q4b

- (i) What is the hexadecimal content of register **R3** after instructions **I1** and **I2** are sequentially executed starting with instruction **I1**?

(2 marks)

- (ii) Identify the pipeline conflict observed in part Q4(d)(i) and explain the cause of the conflict. Suggest one method to resolve this conflict.

(4 marks)

NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2015-2016

CE1006/CZ1006 – COMPUTER ORGANIZATION AND ARCHITECTURE

Nov/Dec 2015

Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 8 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. All questions carry equal marks.
5. The VIP Instruction Set Summary Chart is provided in Appendix 1 on page 8.

-
1. Figure Q1a shows the hexadecimal contents of several registers in the VIP processor and a section of its memory.

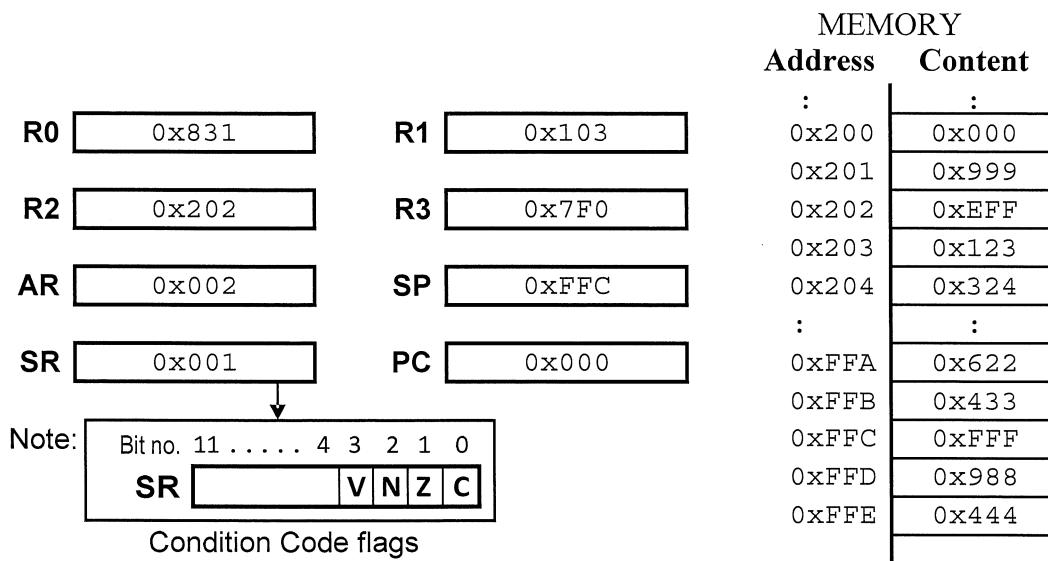


Figure Q1a

Note: Question No. 1 continues on Page 2

- (a) Give (*in hexadecimal*) the 12-bit contents in the two registers **R0** and **SR**, immediately after the execution of each instruction given below.

Note: Instructions (i) to (vi) are **not consecutive instructions**. You must use the initial conditions shown in Figure Q1a to derive your answer for each of the instructions given below.

- (i) **MOV R0 , [0x201]**
- (ii) **MOV R0 , [R2+0xFFD]**
- (iii) **POP R0**
- (iv) **SUB R0 , R1**
- (v) **RLC R0**
- (vi) **EOR R0 , R3**

(12 marks)

- (b) Write the equivalent C high-level code segment that is represented by VIP assembly code segment shown in Figure Q1b. You may assume that your C integer variables **Var1** to **Var3** are represented by the memory addresses given by labels **Var1** to **Var3** respectively.

(4 marks)

Loop	CMP [Var1] , [Var2]
	JLT Done
	SUB [Var1] , [Var2]
	JMP Loop
Done	MOV [Var3] , [Var1]

Figure Q1b

- (c) Using **no more than four** VIP instructions, convert the segment of VIP assembly code in Figure Q1b from a pre-test loop to its post-test loop equivalent. State clearly under what conditions your post-test loop equivalent will fail to work in the same manner as the code segment shown in Figure Q1b.

(6 marks)

- (d) Give a single C statement that can replace the C code segment in Q1(b) such that it will always assign the same numeric result into variable **Var3**, given any positive integer values in **Var1** and **Var2**.

(3 marks)

2. (a) An incomplete VIP assembly language program and the contents of several memory variables are given in Figure Q2. Give the mnemonics of (I1) to (I6) that will complete the missing instructions based on their associated comments.

(8 marks)

Main	MOV SP, #0xFFFF	; Initialize stack pointer									
	?	; Push value in memory variable VarX to stack	(I1)								
	?	; Push value in memory variable VarY to stack	(I2)								
	?	; Push address of memory variable Ans to stack	(I3)								
	CALL SubA	; Call subroutine SubA to update result in Ans									
	?	; Remove parameters on the stack	(I4)								
	:										
SubA	PSHM 0x006	; Save away used registers									
	:	}									
	:	; to be completed as required in question Q2(b)									
	:										
	?	; Restore used registers	(I5)								
	?	; Return to calling program	(I6)								
<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th style="text-align: center;">Address</th> <th style="text-align: center;">Contents</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">VarX 0x200</td> <td style="text-align: center;">0x007</td> </tr> <tr> <td style="text-align: center;">VarY 0x201</td> <td style="text-align: center;">0x006</td> </tr> <tr> <td style="text-align: center;">Ans 0x202</td> <td style="text-align: center;">0x000</td> </tr> </tbody> </table> <p style="text-align: center;">Contents in Memory</p>				Address	Contents	VarX 0x200	0x007	VarY 0x201	0x006	Ans 0x202	0x000
Address	Contents										
VarX 0x200	0x007										
VarY 0x201	0x006										
Ans 0x202	0x000										

Figure Q2

- (b) The subroutine **SubA** implements the equivalent C language statement given by

```
Ans = (VarX + VarY) * 9;
```

Complete the remaining portion of subroutine **SubA** based on the way the parameters **VarX**, **VarY** and **Ans** have been passed in Figure Q2. Assume that C variables **VarX**, **VarY** and **Ans** are 12-bit integer values in the VIP assembly language implementation. State clearly under what condition(s) the results of your VIP implementation will be incorrect. You will be given more marks for a computationally more optimal implementation.

(11 marks)

- (c) Use one or more alternative VIP instructions to implement the equivalent function of **CALL SubA** if you are not allowed to use the **CALL** mnemonic. State clearly the limitation(s) that may arise from your implementation compared to the original **CALL SubA** instruction.

(6 marks)

3. (a) List three differences between Static RAM (SRAM) and Dynamic RAM (DRAM). (6 marks)

(b) List two differences between NOR and NAND flash. (4 marks)

(c) Which type of flash memory would you choose as the system memory for a processor system? Give one reason for your choice. (2 marks)

(d) Figure Q3 shows two processor systems connected via a UART link.

 - System B transmits sensor data continuously over the UART to System A. One UART packet is transmitted with each call to the UART transmit routine in CPU-B.
 - Each time System A's UART peripheral receives a packet of UART data, it will send an interrupt to CPU-A, which will then proceed to read the data in an interrupt service routine (UART_RX_ISR).

Table Q3 shows the various timing and UART parameters of the two systems. Instruction cycle time refers to the time needed to execute one instruction.

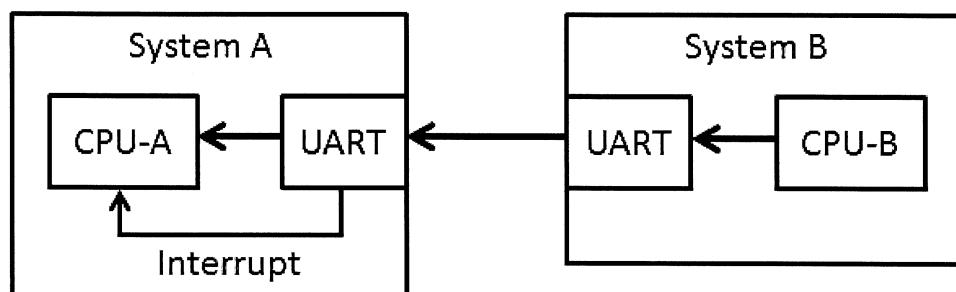


Figure Q3

Note: Question No. 3 continues on Page 5

Table Q3

System A	System B
CPU Interrupt Latency = 10 instruction cycles	CPU Interrupt Latency = 5 instruction cycles
Number of instructions in UART_RX_ISR = 30	Number of instructions in UART transmit routine = 10
Instruction cycle time = 10µs	Instruction cycle time = 20µs
UART Configuration: 1 Start Bit, 7 data bits, Even Parity, 1 STOP bit.	
Allowable UART baud rate: 4800, 9600, 14400, 19200, 28800, 38400, 57600, 115200.	

With reference to Figure Q3 and Table Q3, answer the following questions:

- (i) What is the maximum number of UART_RX_ISR that can be serviced by CPU-A in one second? (2 marks)
- (ii) Ignoring the restriction imposed by the allowable UART baud rates shown in Table Q3, what is the maximum number of UART packets that can be transmitted by System B in one second? (2 marks)
- (iii) Given the UART configuration and the allowable UART baud rates stated in Table Q3, find the maximum data transfer rate in which a data file can be transferred from System B to System A. Give your answer in bytes per second. You should state any assumption you have made in deriving your answer. (5 marks)
- (iv) The data transfer rate requirement for this system is 1800 bytes per second. Based on the calculation in part Q3(d)(iii), state whether the current system can meet the requirement. If not, what needs to be done to enable the system to meet the data transfer rate requirement? Note that no hardware or CPU clock rate changes are allowed and software routines are already speed optimized. (4 marks)

4. (a) Cache design makes use of two locality principles to achieve high cache hit rate.
- (i) What are these two principles? Explain the concept behind these two principles. (4 marks)
- (ii) For each of the principles listed in Q4(a)(i), illustrate how software should be designed in order to leverage on the principle to ensure high cache hit rates. (4 marks)
- (b) Consider a system with a virtual address space of 64 Kbyte, a virtual page size of 1 KByte and a physical address space of 4 KByte. With reference to the paging table (partial) shown in Table Q4, what is the virtual address that is mapped to a physical address of 0x0E00? Note that each memory location contains one byte of data and 1 KByte = 1024 Bytes. (4 marks)

Table Q4

Virtual Page Number	Page Frame Number	Valid Bit
0	2	1
1	-	0
2	3	1
3	1	1
4	-	0
5	0	1
•	-	0
•	-	0

- (c) Given two decimal numbers, X = -11 and Y = 11, describe your choice of multiplicand and multiplier if the Booth algorithm is used to compute their product. Assume 5-bit two's complement notation for multiplicand and multiplier. Illustrate clearly how the multiplication is achieved with the Booth algorithm. (7 marks)

Note: Question No. 4 continues on Page 7

- (d) Consider a processor with 4 pipeline stages: Fetch Instruction (F), Decode (D), Execute (E) and Store (S). The processor supports branch delay and the branch target is only known after the Execute Stage. Figure Q4 shows a code segment which performs accumulation of 100 sets of data and all these instructions are one-word instruction. For the instructions within the loop (**I3** to **I6**), answer the following:
- (i) Which instructions in Figure Q4 can be inserted in the branch delay slots? Give one reason to support your choices. (3 marks)
- (ii) Which instructions cannot be inserted in the branch delay slots? Give one reason to support your choices. (3 marks)

```
MOV  R3, #100    ; I1
MOV  R0, #200    ; I2
Loop ADD  R1, [R0]    ; I3
      INC  R0        ; I4
      DEC  R3        ; I5
      CMP  R3, #0     ; I6
      JNZ  Loop      ; I7
```

Figure Q4

NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2015-2016

CE1006/CZ1006 – COMPUTER ORGANIZATION AND ARCHITECTURE

Nov/Dec 2015

Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 8 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. All questions carry equal marks.
5. The VIP Instruction Set Summary Chart is provided in Appendix 1 on page 8.

-
1. Figure Q1a shows the hexadecimal contents of several registers in the VIP processor and a section of its memory.

		MEMORY	
Address	Content		
R0	0x831	R1	0x103
R2	0x202	R3	0x7F0
AR	0x002	SP	0xFFC
SR	0x001	PC	0x000
Note:		Bit no. 11 4 3 2 1 0	
		SR [V] [N] [Z] [C]	
Condition Code flags			
:		:	:
0x200	0x000	0x200	0x000
0x201	0x999	0x201	0x999
0x202	0xEFF	0x202	0xEFF
0x203	0x123	0x203	0x123
0x204	0x324	0x204	0x324
:	:	:	:
0xFFA	0x622	0xFFA	0x622
0xFFB	0x433	0xFFB	0x433
0xFFC	0xFFFF	0xFFC	0xFFFF
0xFFD	0x988	0xFFD	0x988
0xFFE	0x444	0xFFE	0x444

Figure Q1a

Note: Question No. 1 continues on Page 2

- (a) Give (*in hexadecimal*) the 12-bit contents in the two registers **R0** and **SR**, immediately after the execution of each instruction given below.

Note: Instructions (i) to (vi) are **not consecutive instructions**. You must use the initial conditions shown in Figure Q1a to derive your answer for each of the instructions given below.

- (i) **MOV R0 , [0x201]**
- (ii) **MOV R0 , [R2+0xFFD]**
- (iii) **POP R0**
- (iv) **SUB R0 , R1**
- (v) **RLC R0**
- (vi) **EOR R0 , R3**

(12 marks)

- (b) Write the equivalent C high-level code segment that is represented by VIP assembly code segment shown in Figure Q1b. You may assume that your C integer variables **Var1** to **Var3** are represented by the memory addresses given by labels **Var1** to **Var3** respectively.

(4 marks)

Loop	CMP [Var1] , [Var2]
	JLT Done
	SUB [Var1] , [Var2]
	JMP Loop
Done	MOV [Var3] , [Var1]

Figure Q1b

- (c) Using **no more than four** VIP instructions, convert the segment of VIP assembly code in Figure Q1b from a pre-test loop to its post-test loop equivalent. State clearly under what conditions your post-test loop equivalent will fail to work in the same manner as the code segment shown in Figure Q1b.

(6 marks)

- (d) Give a single C statement that can replace the C code segment in Q1(b) such that it will always assign the same numeric result into variable **Var3**, given any positive integer values in **Var1** and **Var2**.

(3 marks)

2. (a) An incomplete VIP assembly language program and the contents of several memory variables are given in Figure Q2. Give the mnemonics of (I1) to (I6) that will complete the missing instructions based on their associated comments.

(8 marks)

Main	MOV SP, #0xFFFF	; Initialize stack pointer									
	?	; Push value in memory variable VarX to stack	(I1)								
	?	; Push value in memory variable VarY to stack	(I2)								
	?	; Push address of memory variable Ans to stack	(I3)								
	CALL SubA	; Call subroutine SubA to update result in Ans									
	?	; Remove parameters on the stack	(I4)								
	:										
SubA	PSHM 0x006	; Save away used registers									
	:	}									
	:	; to be completed as required in question Q2(b)									
	:										
	?	; Restore used registers	(I5)								
	?	; Return to calling program	(I6)								
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Figure Q2

- (b) The subroutine **SubA** implements the equivalent C language statement given by

```
Ans = (VarX + VarY) * 9;
```

Complete the remaining portion of subroutine **SubA** based on the way the parameters **VarX**, **VarY** and **Ans** have been passed in Figure Q2. Assume that C variables **VarX**, **VarY** and **Ans** are 12-bit integer values in the VIP assembly language implementation. State clearly under what condition(s) the results of your VIP implementation will be incorrect. You will be given more marks for a computationally more optimal implementation.

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(6 marks)

3. (a) List three differences between Static RAM (SRAM) and Dynamic RAM (DRAM). (6 marks)

(b) List two differences between NOR and NAND flash. (4 marks)

(c) Which type of flash memory would you choose as the system memory for a processor system? Give one reason for your choice. (2 marks)

(d) Figure Q3 shows two processor systems connected via a UART link.

 - System B transmits sensor data continuously over the UART to System A. One UART packet is transmitted with each call to the UART transmit routine in CPU-B.
 - Each time System A's UART peripheral receives a packet of UART data, it will send an interrupt to CPU-A, which will then proceed to read the data in an interrupt service routine (UART_RX_ISR).

Table Q3 shows the various timing and UART parameters of the two systems. Instruction cycle time refers to the time needed to execute one instruction.

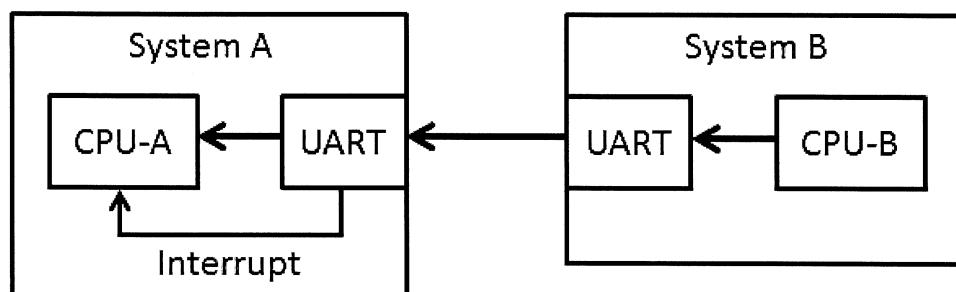


Figure Q3

Note: Question No. 3 continues on Page 5

Table Q3

System A	System B
CPU Interrupt Latency = 10 instruction cycles	CPU Interrupt Latency = 5 instruction cycles
Number of instructions in UART_RX_ISR = 30	Number of instructions in UART transmit routine = 10
Instruction cycle time = 10µs	Instruction cycle time = 20µs
UART Configuration: 1 Start Bit, 7 data bits, Even Parity, 1 STOP bit.	
Allowable UART baud rate: 4800, 9600, 14400, 19200, 28800, 38400, 57600, 115200.	

With reference to Figure Q3 and Table Q3, answer the following questions:

- (i) What is the maximum number of UART_RX_ISR that can be serviced by CPU-A in one second? (2 marks)
- (ii) Ignoring the restriction imposed by the allowable UART baud rates shown in Table Q3, what is the maximum number of UART packets that can be transmitted by System B in one second? (2 marks)
- (iii) Given the UART configuration and the allowable UART baud rates stated in Table Q3, find the maximum data transfer rate in which a data file can be transferred from System B to System A. Give your answer in bytes per second. You should state any assumption you have made in deriving your answer. (5 marks)
- (iv) The data transfer rate requirement for this system is 1800 bytes per second. Based on the calculation in part Q3(d)(iii), state whether the current system can meet the requirement. If not, what needs to be done to enable the system to meet the data transfer rate requirement? Note that no hardware or CPU clock rate changes are allowed and software routines are already speed optimized. (4 marks)

4. (a) Cache design makes use of two locality principles to achieve high cache hit rate.
- (i) What are these two principles? Explain the concept behind these two principles. (4 marks)
- (ii) For each of the principles listed in Q4(a)(i), illustrate how software should be designed in order to leverage on the principle to ensure high cache hit rates. (4 marks)
- (b) Consider a system with a virtual address space of 64 Kbyte, a virtual page size of 1 KByte and a physical address space of 4 KByte. With reference to the paging table (partial) shown in Table Q4, what is the virtual address that is mapped to a physical address of 0x0E00? Note that each memory location contains one byte of data and 1 KByte = 1024 Bytes. (4 marks)

Table Q4

Virtual Page Number	Page Frame Number	Valid Bit
0	2	1
1	-	0
2	3	1
3	1	1
4	-	0
5	0	1
•	-	0
•	-	0

- (c) Given two decimal numbers, X = -11 and Y = 11, describe your choice of multiplicand and multiplier if the Booth algorithm is used to compute their product. Assume 5-bit two's complement notation for multiplicand and multiplier. Illustrate clearly how the multiplication is achieved with the Booth algorithm. (7 marks)

Note: Question No. 4 continues on Page 7

- (d) Consider a processor with 4 pipeline stages: Fetch Instruction (F), Decode (D), Execute (E) and Store (S). The processor supports branch delay and the branch target is only known after the Execute Stage. Figure Q4 shows a code segment which performs accumulation of 100 sets of data and all these instructions are one-word instruction. For the instructions within the loop (**I3** to **I6**), answer the following:
- (i) Which instructions in Figure Q4 can be inserted in the branch delay slots? Give one reason to support your choices. (3 marks)
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Loop ADD  R1, [R0]    ; I3
      INC  R0        ; I4
      DEC  R3        ; I5
      CMP  R3, #0     ; I6
      JNZ  Loop      ; I7
```

Figure Q4

NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2015-2016

CE1006/CZ1006 – COMPUTER ORGANIZATION AND ARCHITECTURE

Nov/Dec 2015

Time Allowed: 2 hours

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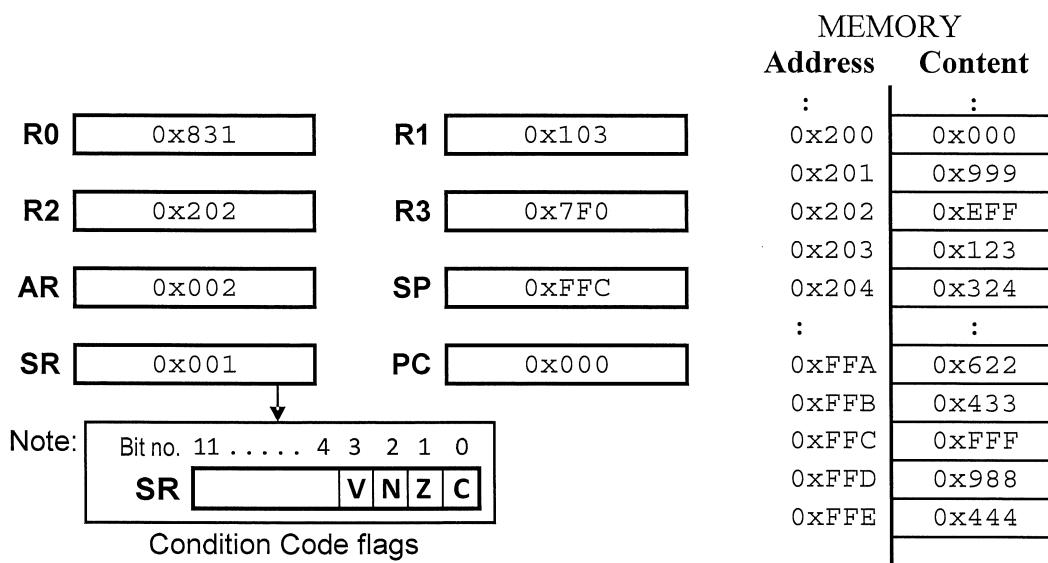


Figure Q1a

Note: Question No. 1 continues on Page 2

- (a) Give (*in hexadecimal*) the 12-bit contents in the two registers **R0** and **SR**, immediately after the execution of each instruction given below.

Note: Instructions (i) to (vi) are **not consecutive instructions**. You must use the initial conditions shown in Figure Q1a to derive your answer for each of the instructions given below.

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(12 marks)

- (b) Write the equivalent C high-level code segment that is represented by VIP assembly code segment shown in Figure Q1b. You may assume that your C integer variables **Var1** to **Var3** are represented by the memory addresses given by labels **Var1** to **Var3** respectively.

(4 marks)

Loop	CMP [Var1] , [Var2]
	JLT Done
	SUB [Var1] , [Var2]
	JMP Loop
Done	MOV [Var3] , [Var1]

Figure Q1b

- (c) Using **no more than four** VIP instructions, convert the segment of VIP assembly code in Figure Q1b from a pre-test loop to its post-test loop equivalent. State clearly under what conditions your post-test loop equivalent will fail to work in the same manner as the code segment shown in Figure Q1b.

(6 marks)

- (d) Give a single C statement that can replace the C code segment in Q1(b) such that it will always assign the same numeric result into variable **Var3**, given any positive integer values in **Var1** and **Var2**.

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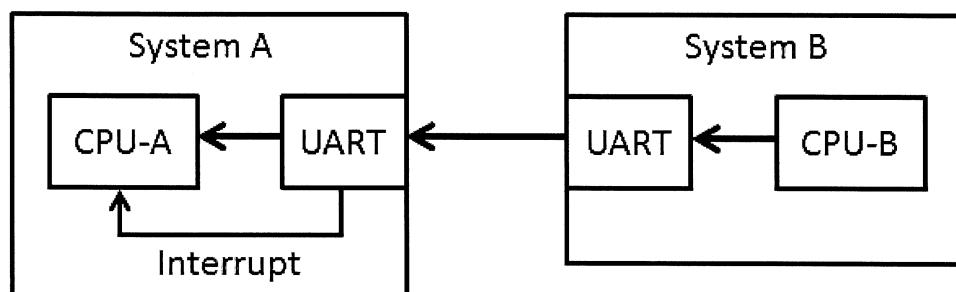


Figure Q3

Note: Question No. 3 continues on Page 5

Table Q3

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4. (a) Cache design makes use of two locality principles to achieve high cache hit rate.
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- (b) Consider a system with a virtual address space of 64 Kbyte, a virtual page size of 1 KByte and a physical address space of 4 KByte. With reference to the paging table (partial) shown in Table Q4, what is the virtual address that is mapped to a physical address of 0x0E00? Note that each memory location contains one byte of data and 1 KByte = 1024 Bytes. (4 marks)

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Note: Question No. 4 continues on Page 7

- (d) Consider a processor with 4 pipeline stages: Fetch Instruction (F), Decode (D), Execute (E) and Store (S). The processor supports branch delay and the branch target is only known after the Execute Stage. Figure Q4 shows a code segment which performs accumulation of 100 sets of data and all these instructions are one-word instruction. For the instructions within the loop (**I3** to **I6**), answer the following:
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MOV  R3, #100    ; I1
MOV  R0, #200    ; I2
Loop ADD  R1, [R0]    ; I3
      INC  R0        ; I4
      DEC  R3        ; I5
      CMP  R3, #0     ; I6
      JNZ  Loop      ; I7
```

Figure Q4

NANYANG TECHNOLOGICAL UNIVERSITY**SEMESTER 2 EXAMINATION 2015-2016****CE1006/CZ1006 – COMPUTER ORGANIZATION AND ARCHITECTURE**

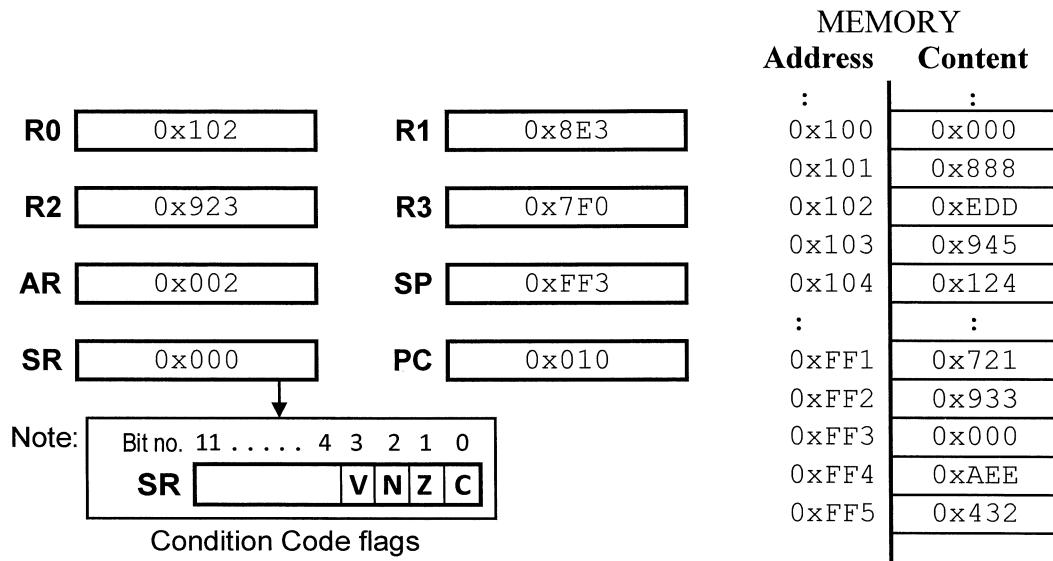
Apr/May 2016

Time Allowed: 2 hours

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1. Figure Q1a shows the hexadecimal contents of several registers in the VIP processor and a section of its memory.

**Figure Q1a**

Note: Question No. 1 continues on Page 2

- (a) Give (*in hexadecimal*) the 12-bit contents in the two registers **R1** and **SR**, immediately after the execution of each instruction given below.

Note: Instructions (i) to (v) are **not consecutive instructions**. You must use the initial conditions shown in Figure Q1a to derive your answer for each of the instructions given below.

- (i) **MOV R1, R3**
- (ii) **MOV R1, [R0]**
- (iii) **OR R1, #0x104**
- (iv) **ADD R1, [SP+0xFFFF]**
- (v) **RAR R1**

(10 marks)

- (b) A VIP assembly language program is given in Figure Q1b. Using the initial conditions shown in Figure Q1a and relevant information in Appendix 1, give (*in hexadecimal*) the 12-bit contents of the **seven** registers **R0**, **R1**, **R2**, **R3**, **PC**, **SP** and **SR** after the execution of the last instruction at the label **FINISH**. Assume the execution of the given series of consecutive instructions begins at the label **START**.

(11 marks)

START	MOV R3, #2
	MOV R1, #0x103
	MOV R2, #2
	MOV R0, [PC]
LOOP	ADD R2, R3
	SUB R3, #1
	JPL LOOP
	MOV [0x103], R3
FINISH	RET

Figure Q1b

- (c) Re-write the code segment given in Figure Q1b so that the program will be optimized. You must ensure that the result produced by the optimized code is identical to that of the original version. (Marks will be awarded based on how well you have optimized the given code segment for both execution speed and code size.)

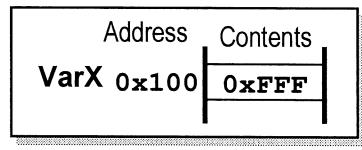
(4 marks)

2. (a) Describe clearly the difference between passing parameter by reference and by value. State how the parameter **VarX** is passed by the instruction (I1) in the VIP assembly program in Figure Q2a.
- (5 marks)
- (b) Give the VIP mnemonics at (I2) and (I3) in Figure Q2a to complete the missing instructions based on their associated comments.
- (4 marks)

```

Main : :
    PSH #0x100 ; Pass parameter to subroutine SubX (I1)
    CALL SubX ; Call subroutine SubX
    ? ; Remove stack parameter (I2)
    :
    :
SubX PSHM 15 ; save registers
    : } ; to be completed as
    : } ; required in question Q2(c)
    ? ; Return to calling program (I3)

```


Figure Q2a

- (c) The VIP subroutine **SubX** computes the absolute value of a 12-bit signed parameter passed to it. For example, the negative value **0xFFFF** in memory variable **VarA** will be converted to the value **0x001** on returning from **SubX**. Complete the partially written subroutine **SubX** shown in Figure Q2a based on the functionality described and the manner in which the parameter has been passed.

(10 marks)

- (d) The C statement in Figure Q2b sets the memory variable **VarA** to **TRUE** (i.e. value of 1) if its current value is a *negative odd number*, otherwise it clears **VarA** to **FALSE** (i.e. value of 0). Using **branchless logic**, implement the equivalent VIP assembly code. You may assume the absolute address of variable **VarA** is given by the label **VarA** and you may use any number of registers in your implementation.

(6 marks)

```

if ((VarA < 0) && ((VarA % 2) == 1)
    VarA = TRUE;
else
    VarA = FALSE;

```

Note: The modulus operator “%” produces the remainder after an integer division

Figure Q2b

3. (a) Determine the most suitable memory to be used for each of the requirements listed in Table Q3a below. The memory types available are: SRAM, DRAM, EEPROM, NAND Flash, NOR Flash and Magnetic HDD. Note that each memory type may be used more than once if deemed most suitable.

Table Q3a

Requirement	Memory Type
Cache Memory to allow very fast access of recent data by CPU	
System memory in the computer system and needs to be able to update and erase every byte individually	
Main data storage in Data Center for cloud storage services	

(6 marks)

- (b) With reference to the structure of a DRAM, explain clearly why there is a need to perform refresh operations when using DRAM to store data.

(4 marks)

- (c) Give a brief description of the two factors that limit the speed in which a parallel bus can operate.

(4 marks)

- (d) Figure Q3 shows two processor systems connected via a UART link.

- System B transmits sensor data continuously over the UART to System A. One UART packet is transmitted with each call to the UART transmit routine in CPU-B.
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Table Q3b shows the various timings and UART parameters of the two systems. Instruction cycle time refers to the time needed to execute one instruction.

Note: Question No. 3 continues on Page 5

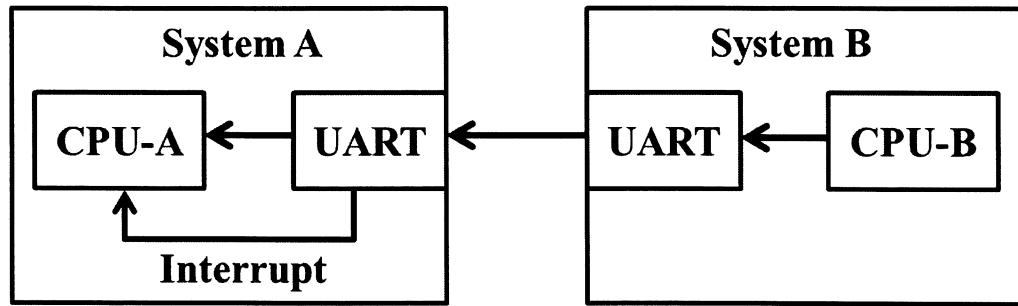


Figure Q3

Table Q3b

System A	System B
CPU Interrupt Latency = 10 instruction cycles	CPU Interrupt Latency = 5 instruction cycles
Number of instructions in UART_RX_ISR = 40	Number of instructions in UART transmit routine = 20
Instruction cycle time = 10µs	Instruction cycle time = 20µs
UART Configuration: 1 Start Bit, 7 data bits, Odd Parity, 1 STOP bit	
Allowable UART baud rate: 4800, 9600, 14400, 19200, 28800, 38400, 57600, 115200	

With reference to Figure Q3 and Table Q3b, answer the following questions:

- (i) In order to achieve the maximum transfer rate, the UART packets are being transferred one after another without any delay between the packets. Calculate and explain whether the system in Figure Q3 will be able to support such transfers at a baud rate of 19200.
(6 marks)
- (ii) Draw the timing diagram of the UART transmission when the data is an ASCII character of value 0x21. Label clearly the Start, Stop, Parity bits and the value of each data bits ('1' or '0').
(3 marks)
- (iii) If delays between each UART packet transmission are allowed, what would be the maximum baud rate that can be used? Choose from the allowable UART baud rate in Table Q3b and explain clearly the reason for choosing the specified baud rate.
(2 marks)

4. (a) List one advantage and one disadvantage for the following

- Magnetic Hard Disk Drive
- Solid State Drive

(4 marks)

(b) Consider a computer system with the characteristics given below, what is the effective access time of this hierarchical memory system?

- Main memory access time = 50 ns
- Cache and main memory access do not overlap
- Cache parameters
 - Cache access time = 5 ns
 - Average cache hit rate = 90%

(4 marks)

(c) One version of the VIP code for multiplication is shown in Figure Q4a.

(i) Comment on the potential issue in using this code to multiply two 12-bit operands.

(2 marks)

(ii) Modify the code in Figure Q4a to perform multiplication of two 12-bit operands correctly. State all assumptions made.

(6 marks)

```
        MOV  AR, #12      ; I1
loop    ROR  R2       ; I2
        JNC  skip      ; I3
        ADD  R0, R3     ; I4
skip    BCSR 1       ; I5
        RLC  R3       ; I6
        JDAR loop     ; I7
```

Figure Q4a

Note: Question No. 4 continues on Page 7

- (d) Consider a processor with 4 pipeline stages: Fetch Instruction (F), Decode (D), Execute (E) and Store (S).
- Branch target address is calculated at the execute stage.
 - Instruction length for every instruction is one word long.
 - Each pipeline stage take 1 cycle to complete.
 - Figure Q4b shows a code segment which performs accumulation of 10 sets of data.
 - **NOP** refers to “No Operation” instruction.
 - Note that this processor is NOT the VIP processor.
- (i) How many cycles does it take to execute the code in Figure Q4b?
Explain clearly how the answer is derived.
(4 marks)
- (ii) Assume that the processor supports delayed branching, modify the code in Figure Q4b to fill up the delay slot(s) with proper instructions.
(2 marks)
- (iii) Explain clearly how the code in Figure Q4b results in less efficient code and how the changes made to the code in Q4(d)(ii) help to improve the efficiency.
(3 marks)

```
MOV  AR, #10      ; I1
MOV  R0, #200     ; I2
MOV  R1, #0       ; I3
NOP             ; I4
loop ADD  R1, [R0] ; I5
INC  R0          ; I6
JDAR loop        ; I7
MOV  R2, R0       ; I8
MOV  R3, R1       ; I9
```

Figure Q4b

NANYANG TECHNOLOGICAL UNIVERSITY**SEMESTER 2 EXAMINATION 2015-2016****CE1006/CZ1006 – COMPUTER ORGANIZATION AND ARCHITECTURE**

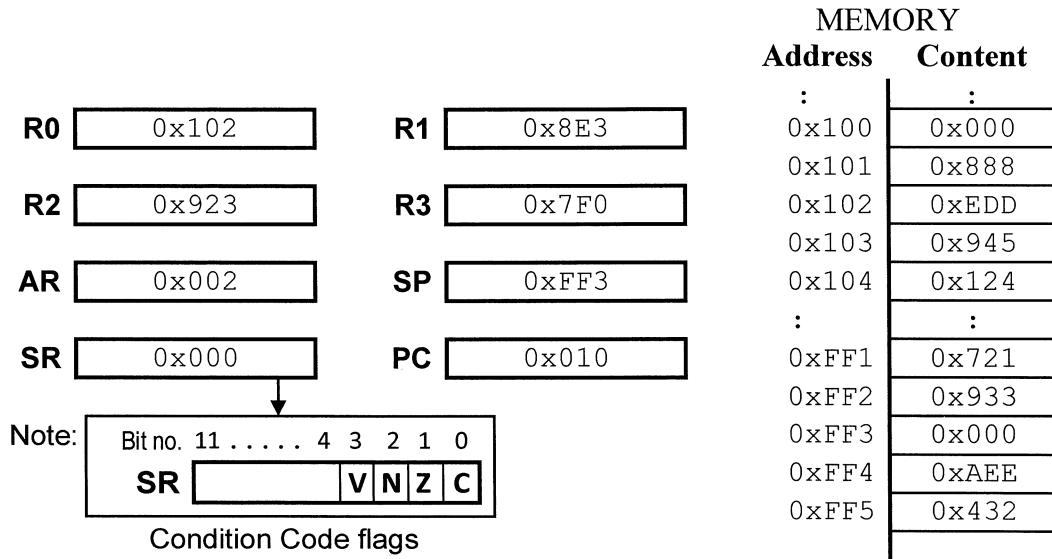
Apr/May 2016

Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 8 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. All questions carry equal marks.
5. The VIP Instruction Set Summary Chart is provided in Appendix 1 on page 8.

1. Figure Q1a shows the hexadecimal contents of several registers in the VIP processor and a section of its memory.

**Figure Q1a**

Note: Question No. 1 continues on Page 2

- (a) Give (*in hexadecimal*) the 12-bit contents in the two registers **R1** and **SR**, immediately after the execution of each instruction given below.

Note: Instructions (i) to (v) are **not consecutive instructions**. You must use the initial conditions shown in Figure Q1a to derive your answer for each of the instructions given below.

- (i) **MOV R1, R3**
- (ii) **MOV R1, [R0]**
- (iii) **OR R1, #0x104**
- (iv) **ADD R1, [SP+0xFFFF]**
- (v) **RAR R1**

(10 marks)

- (b) A VIP assembly language program is given in Figure Q1b. Using the initial conditions shown in Figure Q1a and relevant information in Appendix 1, give (*in hexadecimal*) the 12-bit contents of the **seven** registers **R0**, **R1**, **R2**, **R3**, **PC**, **SP** and **SR** after the execution of the last instruction at the label **FINISH**. Assume the execution of the given series of consecutive instructions begins at the label **START**.

(11 marks)

START	MOV R3, #2
	MOV R1, #0x103
	MOV R2, #2
	MOV R0, [PC]
LOOP	ADD R2, R3
	SUB R3, #1
	JPL LOOP
	MOV [0x103], R3
FINISH	RET

Figure Q1b

- (c) Re-write the code segment given in Figure Q1b so that the program will be optimized. You must ensure that the result produced by the optimized code is identical to that of the original version. (Marks will be awarded based on how well you have optimized the given code segment for both execution speed and code size.)

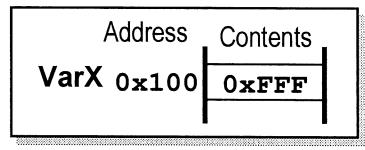
(4 marks)

2. (a) Describe clearly the difference between passing parameter by reference and by value. State how the parameter **VarX** is passed by the instruction (I1) in the VIP assembly program in Figure Q2a.
- (5 marks)
- (b) Give the VIP mnemonics at (I2) and (I3) in Figure Q2a to complete the missing instructions based on their associated comments.
- (4 marks)

```

Main : :
    PSH #0x100 ; Pass parameter to subroutine SubX (I1)
    CALL SubX ; Call subroutine SubX
    ? ; Remove stack parameter (I2)
    :
    :
SubX PSHM 15 ; save registers
    : } ; to be completed as
    : } ; required in question Q2(c)
    ? ; Return to calling program (I3)

```


Figure Q2a

- (c) The VIP subroutine **SubX** computes the absolute value of a 12-bit signed parameter passed to it. For example, the negative value **0xFFFF** in memory variable **VarA** will be converted to the value **0x001** on returning from **SubX**. Complete the partially written subroutine **SubX** shown in Figure Q2a based on the functionality described and the manner in which the parameter has been passed.

(10 marks)

- (d) The C statement in Figure Q2b sets the memory variable **VarA** to **TRUE** (i.e. value of 1) if its current value is a *negative odd number*, otherwise it clears **VarA** to **FALSE** (i.e. value of 0). Using **branchless logic**, implement the equivalent VIP assembly code. You may assume the absolute address of variable **VarA** is given by the label **VarA** and you may use any number of registers in your implementation.

(6 marks)

```

if ((VarA < 0) && ((VarA % 2) == 1)
    VarA = TRUE;
else
    VarA = FALSE;

```

Note: The modulus operator “%” produces the remainder after an integer division

Figure Q2b

3. (a) Determine the most suitable memory to be used for each of the requirements listed in Table Q3a below. The memory types available are: SRAM, DRAM, EEPROM, NAND Flash, NOR Flash and Magnetic HDD. Note that each memory type may be used more than once if deemed most suitable.

Table Q3a

Requirement	Memory Type
Cache Memory to allow very fast access of recent data by CPU	
System memory in the computer system and needs to be able to update and erase every byte individually	
Main data storage in Data Center for cloud storage services	

(6 marks)

- (b) With reference to the structure of a DRAM, explain clearly why there is a need to perform refresh operations when using DRAM to store data.

(4 marks)

- (c) Give a brief description of the two factors that limit the speed in which a parallel bus can operate.

(4 marks)

- (d) Figure Q3 shows two processor systems connected via a UART link.

- System B transmits sensor data continuously over the UART to System A. One UART packet is transmitted with each call to the UART transmit routine in CPU-B.
- Each time System A's UART peripheral receives a packet of UART data, it will send an interrupt to CPU-A, which will then proceed to read the data in an interrupt service routine (UART_RX_ISR).

Table Q3b shows the various timings and UART parameters of the two systems. Instruction cycle time refers to the time needed to execute one instruction.

Note: Question No. 3 continues on Page 5

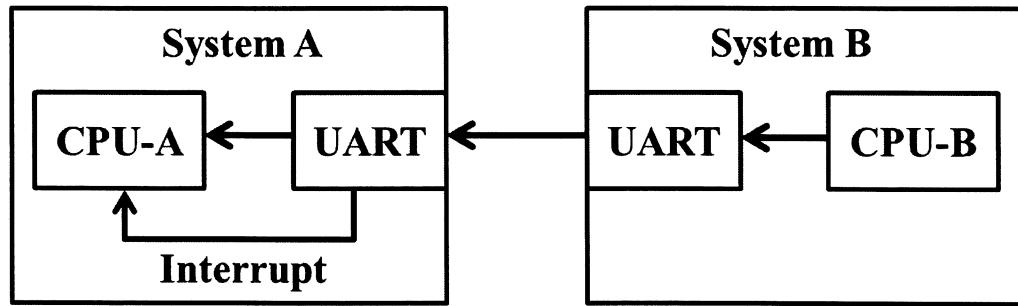


Figure Q3

Table Q3b

System A	System B
CPU Interrupt Latency = 10 instruction cycles	CPU Interrupt Latency = 5 instruction cycles
Number of instructions in UART_RX_ISR = 40	Number of instructions in UART transmit routine = 20
Instruction cycle time = 10µs	Instruction cycle time = 20µs
UART Configuration: 1 Start Bit, 7 data bits, Odd Parity, 1 STOP bit	
Allowable UART baud rate: 4800, 9600, 14400, 19200, 28800, 38400, 57600, 115200	

With reference to Figure Q3 and Table Q3b, answer the following questions:

- (i) In order to achieve the maximum transfer rate, the UART packets are being transferred one after another without any delay between the packets. Calculate and explain whether the system in Figure Q3 will be able to support such transfers at a baud rate of 19200.
(6 marks)
- (ii) Draw the timing diagram of the UART transmission when the data is an ASCII character of value 0x21. Label clearly the Start, Stop, Parity bits and the value of each data bits ('1' or '0').
(3 marks)
- (iii) If delays between each UART packet transmission are allowed, what would be the maximum baud rate that can be used? Choose from the allowable UART baud rate in Table Q3b and explain clearly the reason for choosing the specified baud rate.
(2 marks)

4. (a) List one advantage and one disadvantage for the following

- Magnetic Hard Disk Drive
- Solid State Drive

(4 marks)

(b) Consider a computer system with the characteristics given below, what is the effective access time of this hierarchical memory system?

- Main memory access time = 50 ns
- Cache and main memory access do not overlap
- Cache parameters
 - Cache access time = 5 ns
 - Average cache hit rate = 90%

(4 marks)

(c) One version of the VIP code for multiplication is shown in Figure Q4a.

(i) Comment on the potential issue in using this code to multiply two 12-bit operands.

(2 marks)

(ii) Modify the code in Figure Q4a to perform multiplication of two 12-bit operands correctly. State all assumptions made.

(6 marks)

```
        MOV  AR, #12      ; I1
loop    ROR  R2       ; I2
        JNC  skip      ; I3
        ADD  R0, R3     ; I4
skip    BCSR 1       ; I5
        RLC  R3       ; I6
        JDAR loop     ; I7
```

Figure Q4a

Note: Question No. 4 continues on Page 7

- (d) Consider a processor with 4 pipeline stages: Fetch Instruction (F), Decode (D), Execute (E) and Store (S).
- Branch target address is calculated at the execute stage.
 - Instruction length for every instruction is one word long.
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 - Figure Q4b shows a code segment which performs accumulation of 10 sets of data.
 - **NOP** refers to “No Operation” instruction.
 - Note that this processor is NOT the VIP processor.
- (i) How many cycles does it take to execute the code in Figure Q4b?
Explain clearly how the answer is derived.
(4 marks)
- (ii) Assume that the processor supports delayed branching, modify the code in Figure Q4b to fill up the delay slot(s) with proper instructions.
(2 marks)
- (iii) Explain clearly how the code in Figure Q4b results in less efficient code and how the changes made to the code in Q4(d)(ii) help to improve the efficiency.
(3 marks)

```
MOV  AR, #10      ; I1
MOV  R0, #200     ; I2
MOV  R1, #0       ; I3
NOP             ; I4
loop ADD  R1, [R0] ; I5
INC  R0          ; I6
Jdar loop        ; I7
MOV  R2, R0       ; I8
MOV  R3, R1       ; I9
```

Figure Q4b

NANYANG TECHNOLOGICAL UNIVERSITY**SEMESTER 1 EXAMINATION 2014-2015****CZ1006 – COMPUTER ORGANIZATION AND ARCHITECTURE**

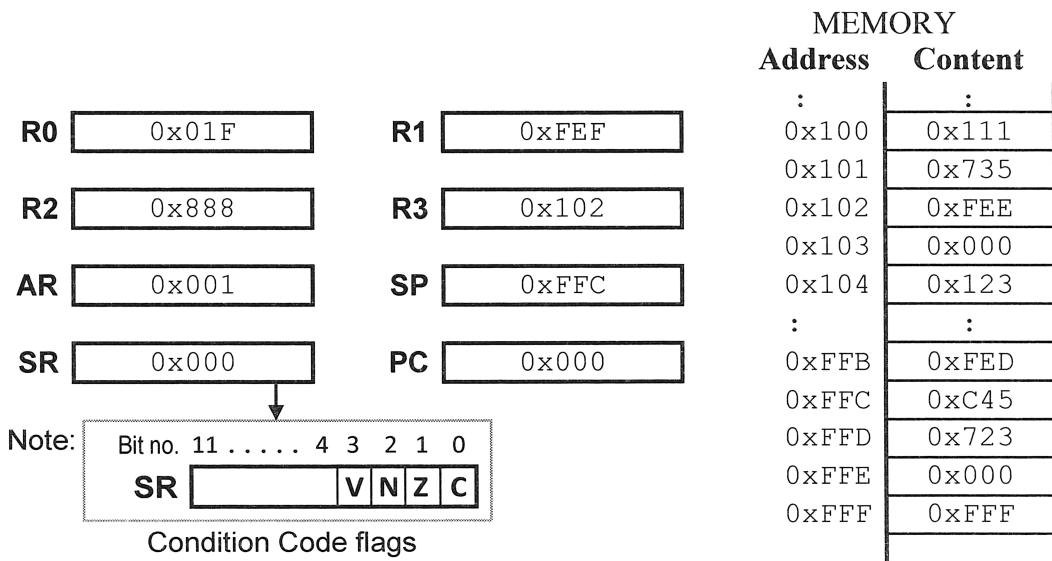
Nov/Dec 2014

Time Allowed: 2 hours

INSTRUCTIONS

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2. Answer **ALL** questions.
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5. The VIP Instruction Set Summary Chart is provided in Appendix 1 on page 7.

1. Figure Q1a shows the hexadecimal contents of several registers in the VIP processor and a section of its memory.

**Figure Q1a**

Note: Question No. 1 continues on Page 2

- (a) Give (*in hexadecimal*) the 12-bit contents in the two registers **R0** and **SR**, immediately after the execution of each instruction given below.

Note: Instructions (i) to (vi) are **not consecutive instructions**. You must use the initial conditions shown in Figure Q1a to derive your answer for each of the instructions given below.

- (i) **MOV** **R0 , R2**
- (ii) **MOV** **R0 , [0x103]**
- (iii) **EOR** **R0 , [R3+0xFFE]**
- (iv) **POPM** **0x003**
- (v) **ADD** **R0 , #0x7F1**
- (vi) **ROR** **R0**

(12 marks)

- (b) Write the equivalent VIP assembly language code that represents part of the C high-level language program instructions given in Figure Q1b. You may assume that the values of these C variables **R0**, **R1**, **R2** and **R3** are *unsigned numbers* located in the 12-bit VIP registers **R0**, **R1**, **R2** and **R3** respectively.

(10 marks)

```

R1=10;
R2=5;
R3=0;
for (R0=1; R0<=3; R0++)
{
    R1=R1+R0;
    R2=R1-R2;
    if (R1>=R1)
    {
        R3=R2+R3;
    }
}

```

Figure Q1b

- (c) Describe clearly how your solution for part Q1(b) will need to be modified if the C variables **R0**, **R1**, **R2** and **R3** in Figure Q1b are now treated as *signed numbers*.

(3 marks)

2. (a) Describe clearly what is meant by passing parameter by reference and give two reasons why you may want to pass a parameter by reference.

(6 marks)

Main	MOV	SP, #0xFFFF	; Initialize stack pointer	(I1)
	PSH	#15	; Push number of elements to sum	(I2)
	PSH	#0x100	; Push start address of array A	(I3)
	PSH	#0x200	; Push start address of array B	(I4)
	PSH	#0x300	; Push start address of array C	(I5)
	CALL	SumArray	; Call subroutine to do $C[i] = A[i] + B[i]$	(I6)
:	:		; Instruction immediately after CALL	(I7)
:	:			

Figure Q2

- (b) Figure Q2 shows a VIP assembly language program that sets up various parameters before calling the subroutine **SumArray**. The subroutine adds **15** consecutive elements of two arrays **A** and **B** that are stored in memory starting at addresses **0x100** and **0x200** respectively. The results of the addition **A[i] + B[i]** will be stored into a third array **C** at the corresponding element position **C[i]**. The array **C** starts at memory address **0x300**.

Write a VIP assembly language subroutine labeled **SumArray** to perform the required function stated above. Your subroutine must only use information from the parameters that have been pushed to the system stack, as shown in Figure Q2. Your solution must also ensure the subroutine is transparent.

(13 marks)

- (c) You would like to determine the memory locations where the main program has been placed. With reference to Figure Q2, give the sequence of VIP assembly language instructions that you would place at **(I7)** onwards in order to compute the start address of the instruction at label **Main**. This address value should be placed into register **R0**. Your sequence of instructions must also remove the parameters that were pushed to the stack earlier.

(6 marks)

3. Figure Q3 shows a basic Sketch program used on the Arduino UNO R3 board to enable UART-based serial communication between the board and its interfacing computer.

```
void setup() {
    // 38400 baud rate
    // 1 start bit, 7 data bits
    // 1 even parity bit, 1 stop bit

    Serial.begin(38400,SERIAL_7E1);
}

// Initialize variable to ASCII character 'U'
int thisByte = 'U';

void loop() {
    Serial.write(thisByte);
    delay(1000);
}
```

Figure Q3

With reference to Figure Q3, answer the questions below.

- (a) Describe the differences between polling, interrupt-driven and DMA data transfer techniques. State which technique is used in the UART communication. (8 marks)
- (b) Describe the differences between synchronous and asynchronous data transfer. State which data transfer method is used in the UART communication. (6 marks)
- (c) The ASCII upper-case character ‘U’ has hexadecimal value 68. What should be the value of its parity bit? (2 marks)
- (d) Determine the maximum data transfer rate in characters per second. (4 marks)

Note: Question No. 3 continues on Page 5

- (e) If the board is re-configured to send the same data packet with no parity, determine the minimum baud rate setting needed to transfer at least 3000 characters per second. The supported baud rates are 19200, 28800, 38400 and 57600. Justify your answer. (5 marks)
4. (a) For each of the devices listed in Table Q4a, state whether its memory is volatile or non-volatile and categorize the device as either system or storage memory. Give your answers using the table format given in Table Q4a. (6 marks)

Table Q4a

Device	Volatile/Non-volatile	System/Storage Memory
DDR SDRAM		
Magnetic Hard-Disk		
Register		

- (b) Table Q4b is an observation table for several direct-mapped cache memory accesses. The address reference strings are provided as hexadecimal numbers and the order of memory access starts from **188** and ends at **27A**.

For each of these address reference strings,

- give the value of the binary bits in the Tag, Block and Word fields.
- state whether each cache memory access registers a hit or a miss, and if the cache content is replaced.

Assume the cache memory is initially empty. Provide your answers using the table format given in Table Q4b.

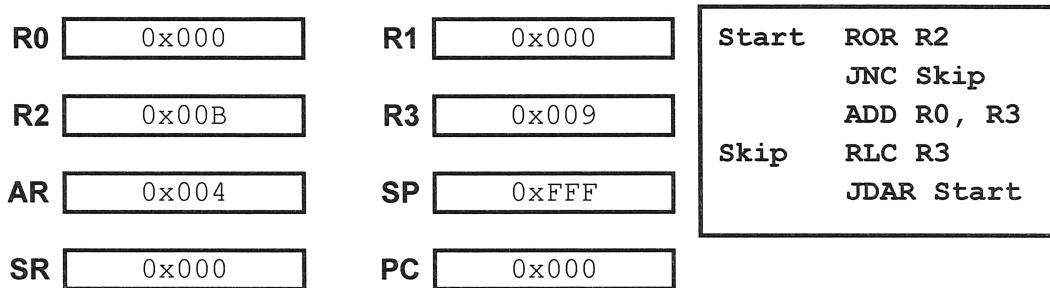
(12 marks)

Note: Question No. 4 continues on Page 6

Table Q4b

Direct-Mapped Cache Memory					
Address Reference String (Hex)	Main Memory Address			Cache Access (Hit/Miss?)	Cache Replace (Yes/No?)
	Tag (2 bits)	Block (4 bits)	Word (4 bits)		
188					
183					
172					
272					
27A					

- (c) Figure Q4 shows the initial contents (in 12-bit hexadecimal format) of several registers in the VIP processor and a VIP program that is to be executed.

**Figure Q4**

After the program is executed, what are the hexadecimal contents of registers **R0**, **R2**, **R3** and **AR**?

(7 marks)