NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 2 EXAMINATION 2012-2013

CE1005/CZ1005 – DIGITAL LOGIC

CPE104/CSC104 – LOGIC DESIGN

April/May 2013 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 6 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. All questions carry equal marks.

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1. (a) Convert the decimal value **3.172** to binary (to 8 significant bits). All steps must be shown clearly.

(4 marks)

(b) Convert the hexadecimal value **EF** to Binary-coded decimal (BCD). All steps must be shown clearly.

(3 marks)

(c) Simplify the following Boolean expression using algebraic manipulations to obtain the minimum cost sum-of-products (SOP) expression.

$$F = [\ a'\ b' + d + b\ (c' + a)'\ ]\ [\ (d\ c')' + a\ c\ ]'$$

(5 marks)

Note: Question No. 1 continues on Page 2

(d) Implement the following Boolean expression using a minimum number of 2-input NOR gates only. Illustrate with a clearly labeled logic circuit diagram.

$$F(w, x, y) = (x + y)(w + y)(x' + y')$$

(6 marks)

(e) Figure Q1 shows a CMOS logic circuit with inputs A, B, C, D and output Z. Obtain its truth table. Give also the Boolean expression of Z. You are not required to minimise the expression.

(7 marks)

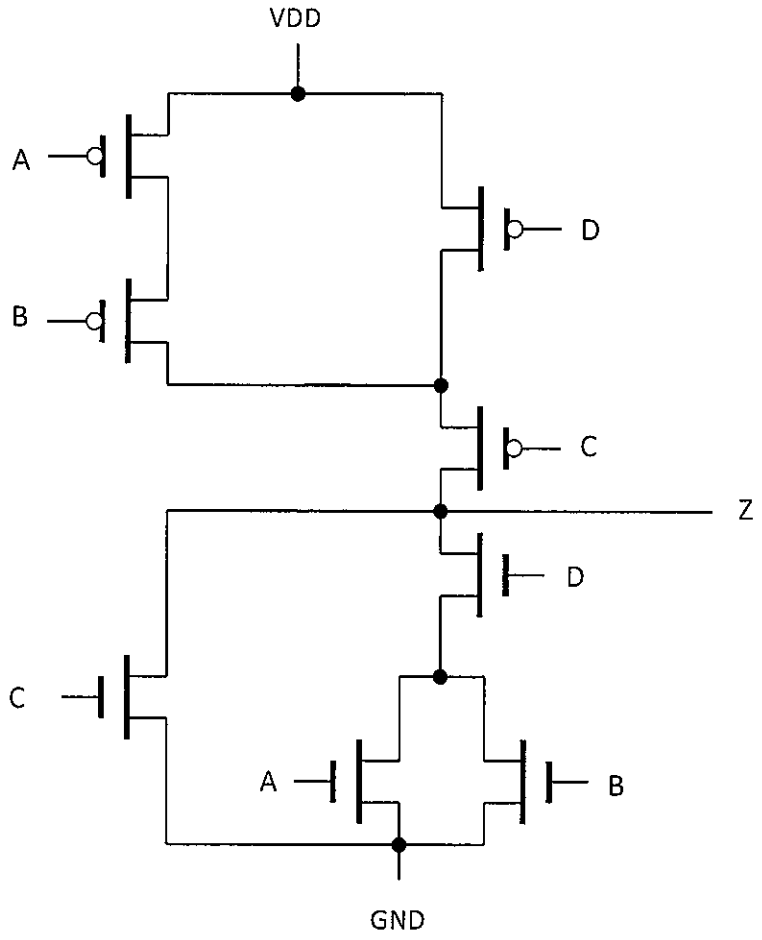

Figure Q1

2. (a) Perform the following signed two's complement multiplication. All steps must be shown clearly. Give also the decimal equivalent of the multiplicands and result.

$$101011 \times 110101$$

(7 marks)

(b) Table Q2 shows the functional truth table of a combinational logic circuit that adds or subtracts two signed numbers, X and Y in 4-bit two's complement representation. The circuit produces logic 1 at the output OVF when there is an arithmetic overflow.

Table Q2

Input	**Outputs**	
ADD*/SUB	Z	OVF
0	Z = X + Y	1 if there is arithmetic overflow. 0 otherwise.
1	Z = X - Y	1 if there is arithmetic overflow. 0 otherwise.

(i) Obtain the Boolean expression of OVF in terms of X, Y and Z when ADD*/SUB = 0.

(ii) Using the result from Q2(b)(ii), obtain a Boolean expression of OVF in terms of X, Y, Z and ADD*/SUB inputs.

(8 marks)

(c) A combinational logic circuit has four inputs A, B, C, D and two outputs P and Q. The canonical expressions for P, Q and the respective "don't care" inputs are given below. In each case, obtain the minimum cost Boolean expression with the use of a Karnaugh map. All loops must be clearly shown.

(i) Give the sum-of-products (SOP) expression for P.

$P(A, B, C, D) = \sum m(0, 3, 7, 9, 10)$
"don't cares" $X(A, B, C, D) = \sum m(2, 6, 8, 14)$

(ii) Give the product-of-sums (POS) expression for Q.

$Q(A, B, C, D) = \prod M(0, 5, 8, 11, 15)$
"don't cares" $Y(A, B, C, D) = \prod M(6, 7, 10, 12)$

(10 marks)

3. (a) Draw the gate level circuit described by the Verilog code in Figure Q3a.

(4 marks)

```
module mod1 (input a, b, c, d, output f);

    not n1 (na, a);
    not n2 (nc, c);
    and a1 (w1, a, b);
    or  o1 (w2, nc, d);
    and a2 (w3, w1, w2);
    and a3 (w4, a, c);
    and a4 (w5, na, nc, d);
    or  o2 (f, w3, w4, w5);
endmodule
```

Figure Q3a

(b) Determine the minimal sum-of-products (SOP) representation for the logic function in Q3(a).

(5 marks)

(c) Hence, write a Verilog module that implements the minimal circuit determined in Q3(b) using a single **assign** statement.

(4 marks)

(d) Briefly explain why this minimisation step is not necessary when using modern design tools and targeting FPGAs.

(3 marks)

(e) Briefly state two advantages of using **assign** statements like the one in Q3(c) as opposed to a gate-level circuit as in Figure Q3a.

(4 marks)

(f) Determine, with explanation, whether the circuit in Figure Q3b implements the same function.

(5 marks)

Note: Question No. 3 continues on Page 5

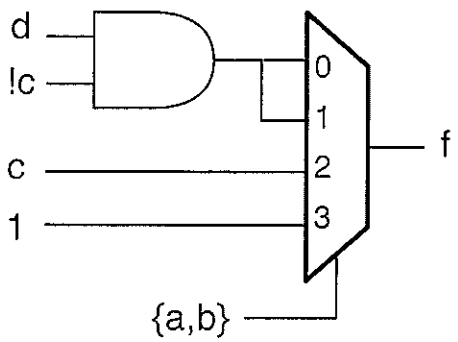

Figure Q3b

4. (a) Identify the three errors in the Verilog code for a counter in Figure Q4a.

(4 marks)

```
module counter (input clk, rst, output [4:0] count);
    always @ *
    begin
        count = count + 1'b1;
    end
endmodule
```

Figure Q4a

(b) Write a correct implementation of an enabled 4-bit up-counter in Verilog. The counter should include an additional *skip* input which, when high, makes the counter increase by 3 rather than increment by 1. Assume all signals are active high.

(6 marks)

(c) If the waveforms in Figure Q4b are used to drive the counter, show the resulting output sequence.

(5 marks)

Note: Question No. 4 continues on Page 6

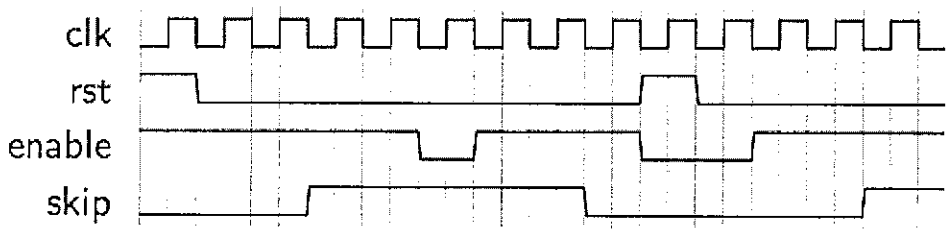

Figure Q4b

(d) Draw the circuit described by the Verilog code fragment in Figure Q4c, labeling all signals accordingly, assuming they are all declared as 1-bit signals. What is this type of circuit called?

(5 marks)

```
always @(posedge clk)
begin
    a <= x;
    s <= m;
    m <= a;
    x <= e;
end
```

Figure Q4c

(e) Briefly discuss the difference between flip-flops and latches, and why flip-flops are preferred in modern design.

(5 marks)

END OF PAPER

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Please read the following instructions carefully:

1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.