NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2012-2013

CE1006/CZ1006 – COMPUTER ORGANIZATION AND ARCHITECTURE

Nov/Dec 2012 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 5 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. All questions carry equal marks.

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1. (a) Consider ARMv5 processor architecture and its instruction set.

   (i) Why can we not use a 32-bit absolute address in ARMv5 architecture?

   (ii) Write a single assembly instruction that will set register (*R*1) to zero, without using a MOV or SUB instruction.

   (iii) What is meant by the term "bus" in the context of the design of a computer architecture and state its purpose?

   (iv) The 32-bit number H'12345678 is held in (byte addressed) memory using the big Endian method starting at memory location H'00001000. What hexadecimal number is held in memory location H'00001002.

   (v) What is meant by the term PC-relative addressing? When is this addressing mode used?

   (10 marks)

Note: Question No. 1 continues on Page 2

(b) Identify the addressing mode of each of the following instructions and explain their operations. Assume ARMv5 processor instruction set.

(i) ADD R1, R1, #100

(ii) STR R0, [R5, #5]

(iii) ADD R1, R2, R3

(iv) BL fn3

(v) LDR R0, #0x100

(15 marks)

2. (a) Find the IEEE754 single precision format representation of the decimal number 10.75. Note that IEEE754-1985 uses 32 bits to represent a single precision number.

(9 marks)

(b) Which of the following Q-formats - Q1.4 or Q1.7 - represents a decimal number 0.78125 accurately? Provide the bit pattern for both formats.

(6 marks)

(c) The following machine code 0xE3A00C01 in ARMv5 architecture loads a 32-bit constant in register R0. Identify the decimal value of the constant stored in register R0.

(6 marks)

(d) Explain Flynn's Taxonomy of computer architecture.

(4 marks)

3. (a) State the advantages and disadvantages of the polled I/O data transfer technique and the interrupt driven I/O data transfer technique.

(6 marks)

(b) Figure Q3 shows the pin layout of a simple microprocessor (μP), a SRAM and a PROM chip. All control signals (**RD**, **WR**, **CS**, etc) are active-high. The microprocessor can be configured to support memory access with or without the use of the **CAS/RAS** control signals.

With reference to Figure Q3, answer the following questions.

(i) What is the total memory space *(in bytes)* supported by the microprocessor if the **CAS/RAS** control signals are NOT used for accessing the memory?

(2 marks)

(ii) What is the total memory space *(in bytes)* supported by the microprocessor if the **CAS/RAS** control signals are used for accessing the memory?

(2 marks)

(iii) What is the memory capacity *(in bits)* of the SRAM and PROM chips?

(4 marks)

(iv) Explain the reason why there is no **WR** control pin on the PROM chip.

(2 marks)

(v) A microprocessor needs to be configured such that addresses ***0x0*** to ***0x3*** are used to store temporary data and addresses ***0x4*** to ***0x7*** are used to store program codes. Using the PROM and the SRAM chips, draw a circuit diagram to show the interconnections between the microprocessor and the required memory chips.

(9 marks)

Note: Question No. 3 continues on Page 4

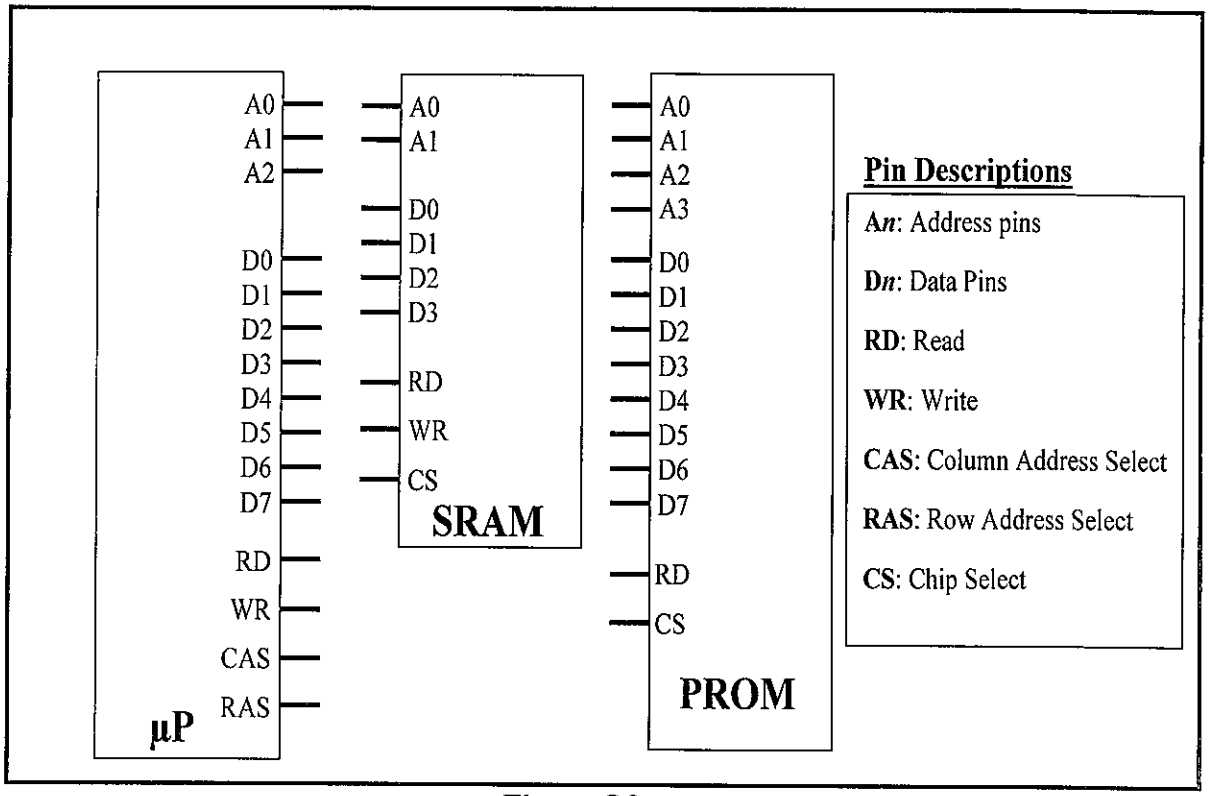

Figure Q3

4. (a) State at least one advantage and one disadvantage of using serial data transfer when compared to using parallel data transfer.

(4 marks)

(b) An asynchronous RS-232 serial port has a baud of 2400. Assuming that the port is transmitting 7-bit ASCII characters, determine the maximum transfer rate (in characters per second) that is achievable? State the asynchronous serial data format that is used to achieve this.

(4 marks)

(c) Table Q4 shows the properties of two magnetic hard disks, **HD_A** and **HD_B**, which are used in a computer system. Assume that the average size of a block being accessed is 32 Kbytes and each data block is stored in consecutive sectors.

Note: Question No. 4 continues on Page 5

Table Q4

Specification	HD_A	HD_B
Number of recording surfaces	16	16
Total number of cylinders	6000	6000
Sectors per track	600	300
Bytes per sector	512	512
Rotational Speed (rpm)	4800	5400
Average Seek Time (ms)	6	6

With reference to the specifications stated in Table Q4, answer the following questions regarding the hard disks and show the calculations performed to obtain your answers:

(i) Calculate the capacities of the hard disks and state which hard disk has the greater capacity?

(5 marks)

(ii) A computer salesman claims that *"a hard disk with a faster rotational speed has a higher average data transfer rate than a hard disk with slower rotational speed"*. By comparing HD_A and HD_B, explain if this claim is always true.

(6 marks)

(d) A processor has a pipeline with four stages: fetch instruction ***(F)***, decode instruction ***(D)***, compute ***(C)*** and write result ***(W)***. Given that each stage will take 1 unit of time and all instructions go through the four stages, determine the minimum units of time required for the processor to complete a sequence of 3 consecutive instructions with the aid of a timing diagram. State any assumptions made.

(6 marks)

END OF PAPER

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Please read the following instructions carefully:

1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.