NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2014-2015

CE1005/CZ1005 – DIGITAL LOGIC

Nov/Dec 2014 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 6 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. All questions carry equal marks.

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1. (a) Perform the following number conversions. All steps must be shown clearly.

(i) Convert 3.91 (decimal) to binary. Give your answer in 8 significant figures.

(3 marks)

(ii) Convert FADE (hexadecimal) to octal.

(3 marks)

(b) Minimise the following logic expression algebraically. Give your answer in Sum-of-Products form. Show all steps clearly.

$$F(a, b, c, d) = (a + c' d') [b' c + (a' d + b c d')']$$

(8 marks)

Note: Question No. 1 continues on Page 2

(c) Figure Q1a shows a CMOS logic circuit with inputs A, B, C and D and output F. Obtain its truth table and the Boolean expression of F. You are not required to simplify the expression.

(7 marks)

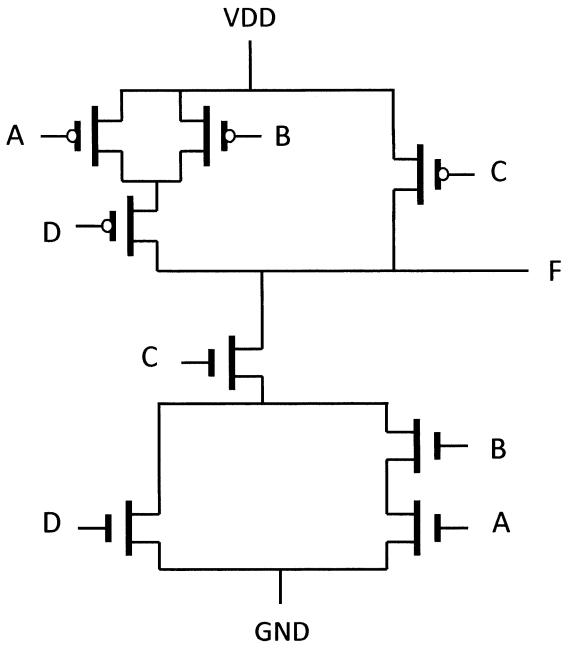

Figure Q1a

(d) The signal shown in Figure Q1b is applied to the input of a Schmitt-trigger inverter with threshold voltages VT- = 0.7 V and VT+ = 1.6 V. Sketch the inverter's output waveform. Show its relation with the input signal clearly.

(4 marks)

Figure Q1b

2. (a) Figure Q2 shows the block diagram of a logic circuit that performs the arithmetic addition X + Y, where X and Y are both 4-bit unsigned numbers stored in memory. The sequence of operation is controlled by the logic signals CLR, LOAD and TRANSFER.

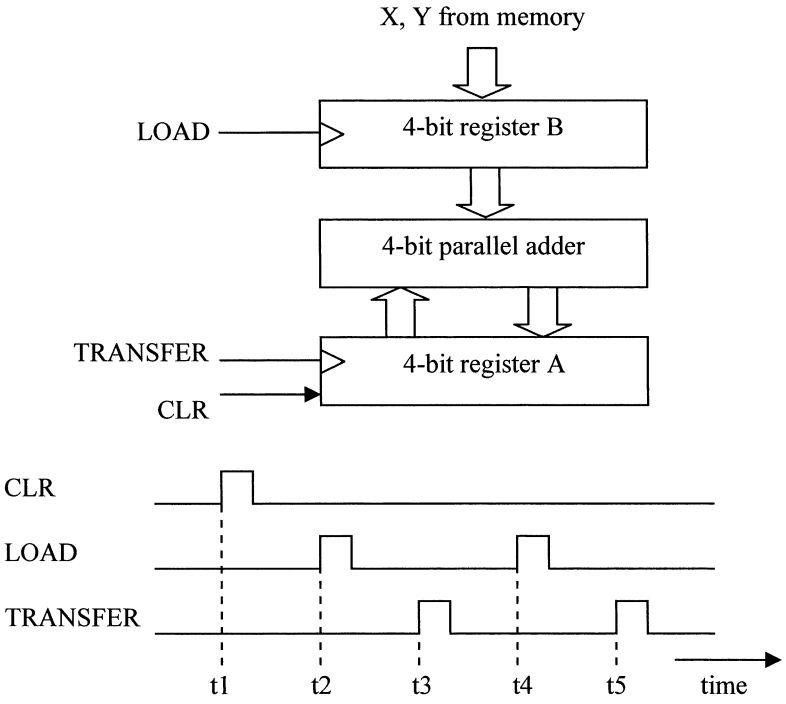

Figure Q2

(i) State the purpose accomplished by the signals CLR, LOAD and TRANSFER for each of the time instances t1, t2, t3, t4 and t5 in Figure Q2.

(5 marks)

(ii) What operation takes place in the circuit between time t4 and t5? Will the circuit still function correctly if the time difference between t4 and t5 is reduced to zero? Explain your answer.

(3 marks)

(b) Perform the arithmetic operation $\mathbf{-92_{10} - 38_{10}}$. Express each signed decimal number in 8-bit two's complement representation and then perform the operation. Show all steps clearly. State whether or not there is overflow.

(5 marks)

Note: Question No. 2 continues on Page 4

(c) A combinational logic circuit's input is a 4-bit unsigned binary number represented by x3 (MSB), x2, x1 and x0 (LSB). Its output y is logic 1 if the input is a prime number. For all other cases, the output y is logic 0. The relevant prime numbers are 2, 3, 5, 7, 11 and 13 (in decimal).

(i) Construct a truth table for the logic circuit.

(6 marks)

(ii) Using Karnaugh map, obtain a minimized Sum-of-Products expression for the output. Show all loops clearly.

(6 marks)

3. You are required to implement a combinational circuit that determines the number of days in a month.

(a) The combinational circuit has a 4-bit input bus (*M[3:0]*) and 2-bit output bus (*D[1:0]*). The binary encoding for **Month** (*M[3:0]*) and **Days** (*D[1:0]*) are shown in Table Q3. When there are no valid inputs for **Month**, *D[1:0]* = 00.

(i) Find the minimal Boolean expressions (Sum-of-Products or Product-of-Sums) for *D[1]* and *D[0]*.

(4 marks)

(ii) Write the Verilog **assign** statements to implement the minimal circuit determined in Q3(a)(i).

(4 marks)

Table Q3

Month	M[3:0]	Days	D[1:0]
January	0001	31	11
February	0010	28	01
March	0011	31	11
April	0100	30	10
May	0101	31	11
June	0110	30	10
July	0111	31	11
August	1000	31	11
September	1001	30	10
October	1010	31	11
November	1011	30	10
December	1100	31	11

Note: Question No. 3 continues on Page 5

(b) The combinational circuit in Q3(a) is modified to include an additional active high input (*leap_year*) and an additional output (*D[2]*). When *leap_year* is asserted and the input **Month** is February, *D[2]* = 1, otherwise *D[2]* = 0. The function for *D[1:0]* is the same as described in Q3(a).

(i) Implement the function for *D[2]* using structural gate-level primitives in Verilog.

(5 marks)

(ii) Write a single Verilog **assign** statement to implement the function for *D[2]*.

(3 marks)

(iii) Using only behavioral description, write the Verilog module for the modified combinational circuit with inputs (*M[3:0]*, *leap_year*) and output (*D[2:0]*).

(9 marks)

4. (a) Figure Q4a shows a 2-bit counter with synchronous reset. Complete the timing diagram for the counter in Figure Q4b by filling in the waveform for *cnt[1:0]*.

(4 marks)

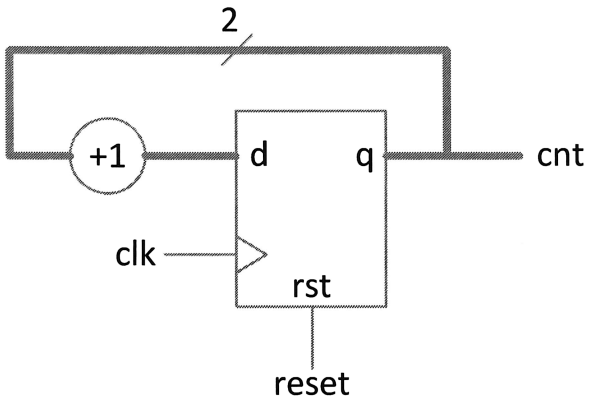

Figure Q4a

Note: Question No. 4 continues on Page 6

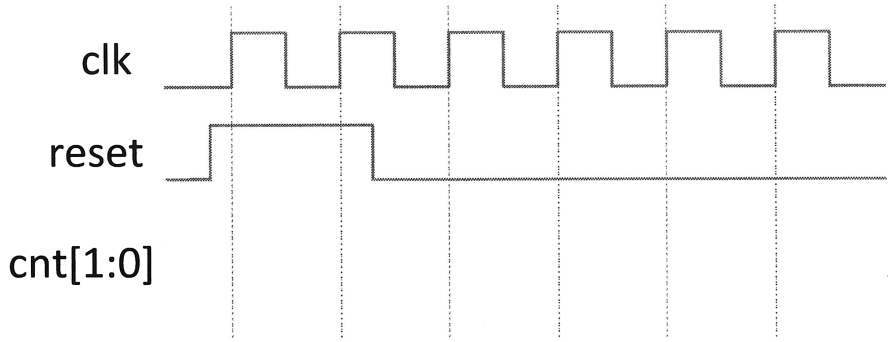

Figure Q4b

(b) A driver alert system monitors the eyes of the driver and alerts the driver when the eyes are closed for a period of time. The finite state machine (FSM) has five active high inputs: *start*, *stop*, *open, close, timeout*; and two outputs: *on_alarm*, *rst_timer*:

- The FSM starts in the *idle* state.
- In the *idle* state, if *start* is asserted, the FSM moves to the *check_eye_status* state.
- In the *check_eye_status* state, if both *close* and *timeout* are asserted, the FSM moves to the *alert_driver* state.
- In the *check_eye_status* state, if *open* is asserted, the FSM moves to the *reset_timer* state.
- In the *check_eye_status* state, if *stop* is asserted, the FSM moves to the *idle* state.
- In the *alert_driver* state, the *on_alarm* output is HIGH and the FSM moves to the *reset_timer* state at the rising edge of the clock. The *on_alarm* output is LOW in other states.
- In the *reset_timer* state, the *rst_timer* output is HIGH and the FSM moves to the *check_eye_status* state at the rising edge of the clock. The *rst_timer* output is LOW in other states.

(i) Draw the state transition diagram that captures the above behavior.

(7 marks)

(ii) Implement the FSM in Verilog. Use a combinational **always** block for the state transitions, and a separate synchronous **always** block for the register process.

(14 marks)

END OF PAPER

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Please read the following instructions carefully:

1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.