NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2013-2014

CE1005/CZ1005 – DIGITAL LOGIC

Nov/Dec 2013 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 6 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. All questions carry equal marks.

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1. (a) Perform the following unsigned number conversions. All steps must be shown clearly.

   (i) Convert 9B (hexadecimal) to octal.

   (ii) Convert 10101.101 (binary) to decimal.

   (iii) Convert 2.4 (decimal) to binary (with 8 significant bits).

   (7 marks)

   (b) The operands (enclosed in pairs of square brackets) in the following arithmetic operations are given in signed decimal. In each case, express the operands in 8-bit two's complement representation and perform the operation using two's complement arithmetic. All steps must be shown clearly. In each case, state whether or not arithmetic overflow has occurred.

   (i) [-87] + [110]

   (ii) [93] – [-54]

   (6 marks)

Note: Question No. 1 continues on Page 2

(c) Using Boolean algebra, minimize the following logic expression to SOP (sum-of-product) form. All steps must be shown clearly.

F (a, b, c, d) = a' (c' + d)' (a c)' [a' c d + (b' + c)']'

(6 marks)

(d) Determine the minimum number of bits required to represent the number specified in each case below. All steps must be shown clearly.

(i) unsigned decimal **99**

(ii) any signed 20-digit decimal number

(6 marks)

2. (a) A facility is fitted with four sensors T, M, H and L, each of which produces a logic output independently. Depending on the logic outputs of the sensors, two independent controllers W and X, are to be activated as specified in Table Q2.

Table Q2

Outputs of sensors	**Controllers to be activated**
T, M, H and L are all 0	None
H or/and L are 1; T and M are both 0	W only
H and L are 0; T or M (but not both) is 1	W only
H or/and L are 1; T or M (but not both) is 1	X only
T and M are both 1	Both W and X

Design a combinational logic circuit that takes the four sensor logic signals as inputs, and produces two outputs W and X, such that they are logic 1 when the corresponding controllers are to be activated.

(i) Determine the truth table of the circuit.

(ii) Obtain the simplified Boolean expressions for W and X in SOP (sum-of-product) form with the aid of Karnaugh maps. All loops must be clearly shown.

(15 marks)

Note: Question No. 2 continues on Page 3

(b) Figure Q2 shows a CMOS logic circuit with inputs A, B, C, D and output F. Determine its truth table and logic expression.

(6 marks)

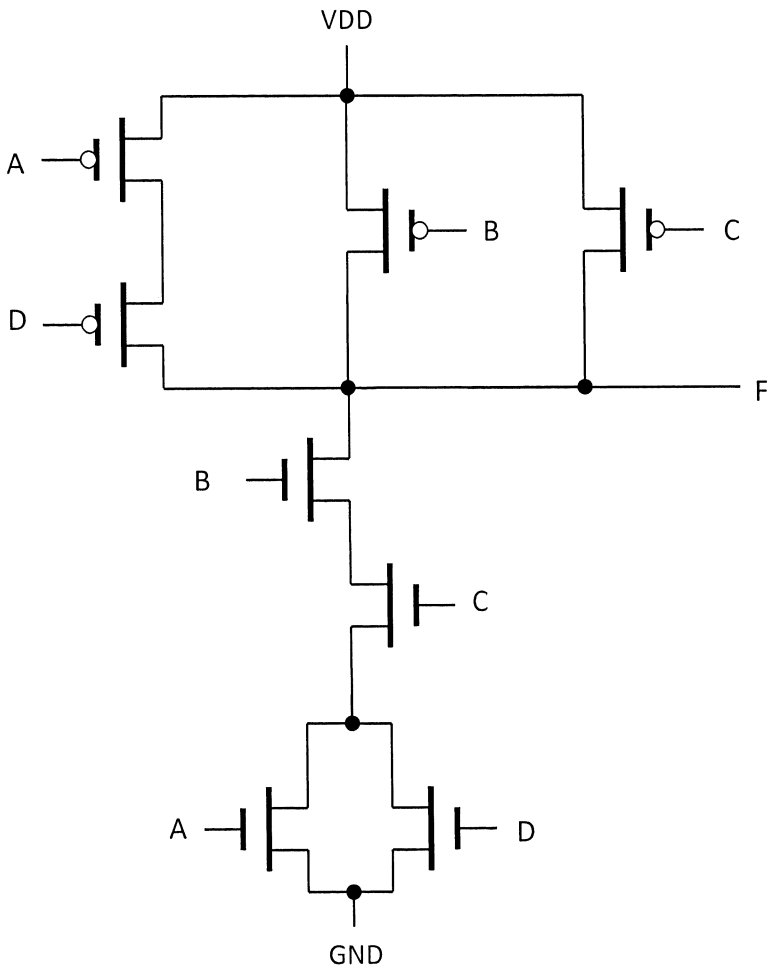

Figure Q2

(c) Briefly describe each of the following terms and how they may affect the performance of a logic circuit.

(i) Propagation delay

(ii) Noise margin

(4 marks)

3. A pressure gauge measures tyre pressure relative to atmospheric pressure, referred to as the relative pressure (*Rp*). The pressure gauge produces a relative pressure output between 0 kPa and 400 kPa. The absolute pressure is the relative pressure plus the atmospheric pressure, which at sea level is approximately 100 kPa.

(a) Sketch a simple circuit using a single unsigned adder and a single multiplexer which will output (as *Pout*) the relative pressure if a 1-bit *Disp* signal is a logic '0', and the absolute pressure if *Disp* is a logic '1'. Clearly indicate the size (in bits) of all inputs and outputs. Note that the circuit should only have two inputs and one output (*Pout*).

(6 marks)

(b) Write a structural Verilog module to implement the circuit in Q3(a) by instantiating the adder module declared below. You are not required to implement the adder.

```
module adder #(parameter SIZE=4)(
        input [SIZE-1:0] A, B, output Cout, output [SIZE-1:0] Sum);
```

(11 marks)

(c) Write a behavioural Verilog module to implement the circuit in Q3(a).

(8 marks)

4. (a) Figure Q4a shows a negative edge-triggered flip-flop, a level sensitive latch, and a positive edge-triggered flip-flop. Complete the timing diagram in Figure Q4b by filling in the waveforms for *Out1*, *Out2* and *Out3*.

(6 marks)

(b) Figure Q4c shows a circuit with two inputs (*Clk* and *Rst*), and a 4-bit output bus (*Q[3:0]*). When *Rst* is HIGH, *Q[3:0]* = 0000. When *Rst* is LOW, the chain of flip-flops behaves like a shift register.

Note: Question No. 4 continues on Page 5

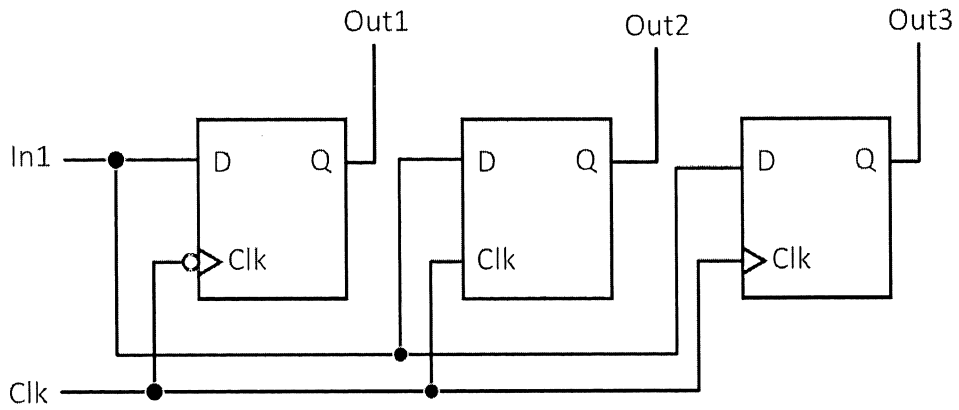

Figure Q4a

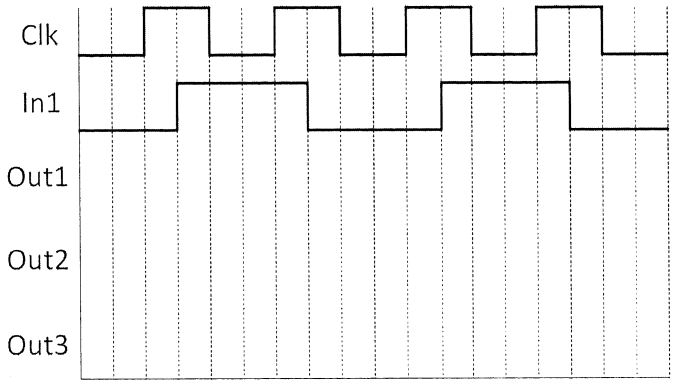

Figure Q4b

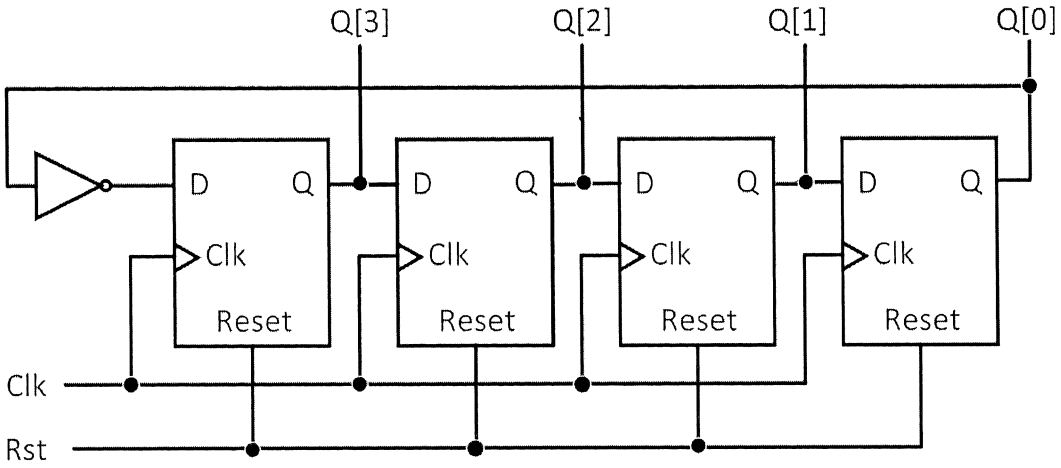

Figure Q4c

Note: Question No. 4 continues on Page 6

(i) Draw the state transition diagram of the circuit in Figure Q4c. Each state must be labeled with the output values (*Q[3:0]*). Show how the input *Rst* affects the state transitions.

(6 marks)

(ii) Write a Verilog module for the circuit in Figure Q4c.

(6 marks)

(c) A factory uses a sensor to detect cans on a conveyor belt, and increments the number of cans detected and the number of missing cans. The finite state machine (FSM) has three inputs: *start*, *stop*, *detected*; and two outputs: *inc_cans*, *inc_missing*:

- The FSM starts in the *idle* state and moves to that state when *stop* is asserted.
- In the *idle* state, if *start* is asserted, the FSM moves to the *check_sensor* state.
- In the *check_sensor* state, if *detected* is asserted, the FSM moves to the *detected* state.
- In the *check_sensor* state, if *detected* is de-asserted, the FSM moves to the *missing* state.
- In the *detected* state, the *inc_cans* output is HIGH and the FSM moves to the *check_sensor* state at the rising edge of the clock. The *inc_cans* output is LOW in other states.
- In the *missing* state, the *inc_missing* output is HIGH and the FSM moves to the *check_sensor* state at the rising edge of the clock. The *inc_missing* output is LOW in other states.

Draw a state transition diagram that captures the above behaviour.

(7 marks)

END OF PAPER

CE1005 DIGITAL LOGIC
CZ1005 DIGITAL LOGIC

Please read the following instructions carefully:

1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.