NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 2 EXAMINATION 2011-2012

CE1006/CZ1006 – COMPUTER ORGANISATION AND ARCHITECTURE

April/May 2012 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 6 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. All questions carry equal marks.

---

1. Computers store numbers in many different ways, including signed and unsigned integers, Q-format (fractional format), and using IEEE754 representation.

   (a) Determine the 6-bit binary result when the two's complement representation of decimal values 5 and -5 are fed into an ALU which is set to perform an AND operation. Note which of the flags N, Z, C and V are set when the operation completes. Repeat for EOR and ADD.

   (9 marks)

   (b) Calculate how many bits the 8-bit immediate value 0x7E needs to be rotated right within a 32-bit register to produce the value 0xF800 0001. State why the ARM needs to use this kind of procedure to load a large immediate number (such as the one shown) into a register.

   (7 marks)

   (c) IEEE754-1985 defines single and double precision floating point numbers of size 32-bits and 64-bits, respectively. Show how the decimal value 56 can be stored in single precision IEEE754 format.

   (9 marks)

2. A simple CPU with ARM-style instructions is shown in Figure Q2a. The #n indicates an immediate value, and [#n] an absolute memory address. The instruction `b m5` would branch to the instruction at memory location 5, and 'halt' ends the execution.

(a) Construct a table as shown in Table Q2b that will trace through the operation of this CPU beginning in the state shown in Figure Q2a. In each row, record the state of the CPU after executing the current instruction. For your convenience, the first row has been completed.

(10 marks)

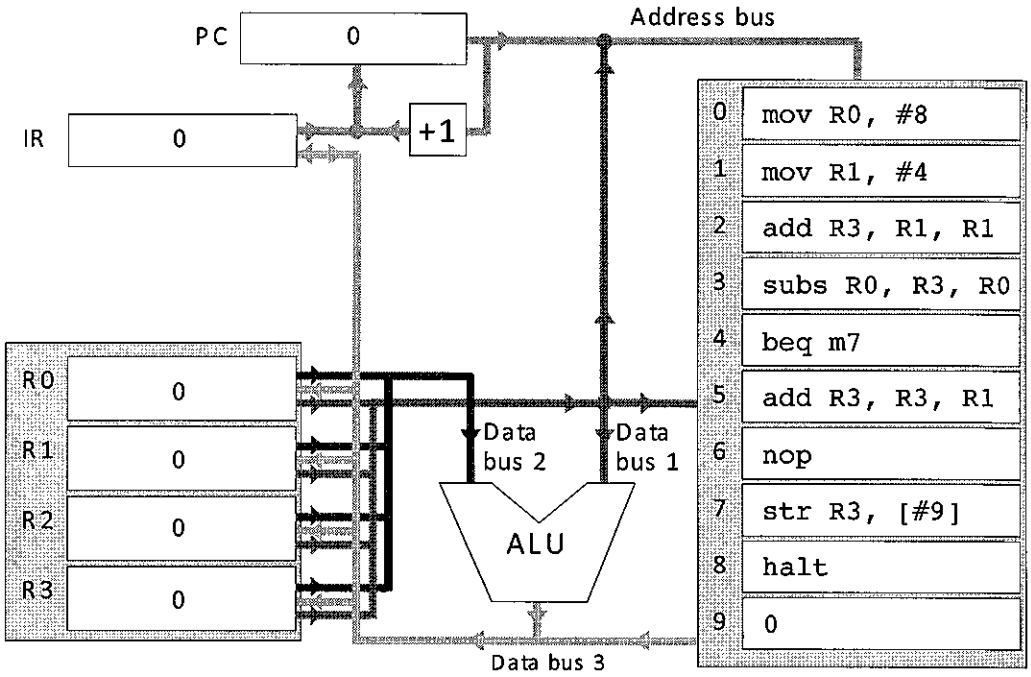

Figure Q2a

Table Q2b

Instruction	PC	R0	R1	R3
`mov R0, #8`	1	8	0	0

(b) Briefly explain the purpose of the connection leading from the IR to the PC in Figure Q2a. State during which instruction (if any) it will be active.

(3 marks)

Note: Question No. 2 continues on Page 3

(c) Does the arrangement of the link discussed in Q2(b) imply that either absolute or PC-relative branching is used?

(4 marks)

(d) By noting the limitations imposed by the direction arrows shown on the various buses in Figure Q2a, state whether this CPU would be able to execute the following instructions in a single clock cycle.

(i) add R0, [#9], [#8]

(ii) sub [#9], R1, R2

(iii) mov R0, #10

(iv) add R0, R1, #5

(8 marks)

3. (a) A processor has a pipeline with three stages: fetch instruction (FI), decode instruction (DI) and execute instruction (EI). Assume that each stage will take 1 unit of time and that all instructions go through the three stages.

(i) With the aid of a timing diagram, determine the minimum units of time required for the processor to complete a sequence of 4 consecutive instructions. State any assumptions made.

(6 marks)

(ii) Determine the total units of time required for the processor to complete a sequence of 4 consecutive instructions if the pipeline is disabled.

(2 marks)

(b) List two differences in the characteristics between a read-only memory (ROM) and a random-access memory (RAM). Explain why most computer systems would have both these types of memory.

(4 marks)

Note: Question No. 3 continues on Page 4

(c) What is the difference between DRAM and SRAM in terms of characteristics such as speed, capacity and cost?

(3 marks)

(d) Table Q3a shows a page table for a logical address space (composed of 8 pages of 1024 bytes each) mapped into 4096 bytes of physical address space. With reference to Table Q3a, answer the following questions assuming that all numbers are decimal, everything is numbered starting from 0 and all addresses are memory byte addresses.

(i) How many bits are required to store the page frame number for each entry of the page table?

(2 marks)

(ii) Explain the possible use of the 'Valid bit' and the 'Modify bit' in the page table.

(4 marks)

(iii) Complete the table started in Table Q3b to indicate the corresponding physical address, if any, for each of the virtual addresses listed. If necessary, indicate whether a page fault has occurred.

(4 marks)

Table Q3a

Virtual Page Number	Valid bit	Modify bit	Page Frame Number
0	1	1	3
1	0	0	-
2	1	0	2
3	0	0	-
4	1	1	1
5	0	0	-
6	1	0	0
7	0	0	-

Table Q3b

Virtual Address	Physical Address
0	
1234	
3001	
6789	

4. (a) Figure Q4a shows a waveform captured from the output of an RS-232 port.

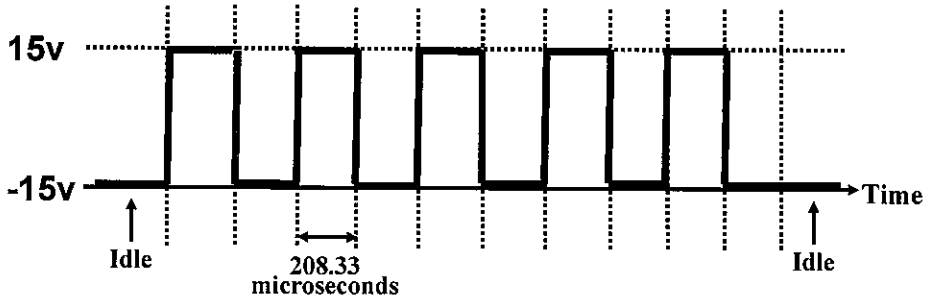

Figure Q4a

Table Q4b

MS / LS	0	1	2	3	4	5	6	7
0	NUL	DLE	SP	0	@	P	'	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	'	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	HT	EM	)	9	I	Y	i	y
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[	k	{
C	FF	FS	,	<	L	\	l	|
D	CR	GS	-	=	M	]	m	}
E	SO	RS	.	>	N	^	n	
F	SI	US	/	?	O	_	o	DEL

(i) Assume that one character was received error-free with the parity bit enabled. Specify the asynchronous serial data format and the baud rate used by this RS-232 interface.

(5 marks)

Note: Question No. 4 continues on Page 6

(ii) Using the ASCII table shown in Table Q4b, state the ASCII character transmitted, assuming that the least-significant bit is transmitted first.

(2 marks)

(iii) Calculate the data transfer rate of this RS-232 interface in characters per second (cps).

(2 marks)

(iv) Re-compute Q4(a)(iii) if the parity bit is now disabled. Discuss what has been sacrificed for this gain in transfer rate.

(4 marks)

(b) A magnetic hard disk has 16 recording surfaces with a total of 12,000 cylinders. There is an average of 300 sectors per track and each sector contains 512 bytes of data. The hard disk operates with a rotational speed of 5400 rpm and has a 6 ms average seek time. The average size of a block being accessed is 32 Kbytes and each data block is stored in consecutive sectors. Answer the following questions regarding this hard disk and show the calculations performed to obtain your answers.

(i) What is the maximum number of bytes that can be stored on this hard disk?

(2 marks)

(ii) What is the average data transfer rate (in bytes per second) for accessing consecutive data blocks on the same track?

(2 marks)

(iii) What is the average percentage of the total time occupied by the seek and rotational delays for accessing a random data block on the hard disk?

(6 marks)

(iv) Using an additional hard disk with similar properties, which RAID configuration would improve the fault tolerance of the array?

(2 marks)

END OF PAPER

CE1006 COMPUTER ORGANISATION AND ARCHITECTURE
CZ1006 COMPUTER ORGANISATION AND ARCHITECTURE

Please read the following instructions carefully:

1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.