NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 2 EXAMINATION 2015-2016

CE1005/CZ1005 – DIGITAL LOGIC

Apr/May 2016 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 6 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. All questions carry equal marks.

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1. (a) A 16-bit integer **9A6D** (hexadecimal) is stored in a digital system. For each of the following representations of the integer, determine the decimal value, and sign where applicable. Show all steps clearly.

(i) unsigned binary

(2 marks)

(ii) sign-magnitude

(2 marks)

(iii) two's complement

(3 marks)

(b) (i) Represent the unsigned decimal value **25.904** in 16-bit fixed-point format, with 8 bits each allocated to the integer and the fractional parts. Show all steps clearly.

(3 marks)

(ii) Briefly describe how the value in Q1(b)(i) may be represented in a 16-bit floating-point format.

(3 marks)

Note: Question No. 1 continues on Page 2

(c) Use algebraic manipulations to obtain a minimum cost Sum-of-product (SOP) expression for the following Boolean function. Show all steps clearly.

$$F(w, x, y, z) = (wz' + y)' (xy'z + x'yz) ((w'x)' + y'z')'$$

(6 marks)

(d) A digital circuit has logic inputs Enable*, A, B*, C and output G*, where * denotes an active Low signal. When the circuit is disabled, the output G* is negated. When the circuit is enabled, the output G* is asserted if-and-only-if exactly 2 out of the 3 inputs A, B*, C are asserted. Sketch a clearly-labelled logic circuit diagram using suitable symbols to illustrate the circuit implementation. You are not required to simplify the circuit.

(6 marks)

2. (a) Sketch a timing diagram to illustrate each of the following parameters of an inverter:

- Rise time, tr
- Fall time, tf
- Propagation delay, tPHL
- Propagation delay, tPLH

(6 marks)

(b) Briefly describe the following types of digital circuit output:

(i) Tristate

(3 marks)

(ii) Open-drain

(3 marks)

(c) Perform the following 5-bit 2's complement signed multiplication. Show all steps clearly. Give the answer in decimal value.

11001 x 10010

(5 marks)

Note: Question No. 2 continues on Page 3

(d) The output F of a 4-input logic circuit has the following canonical expression along with the don't care inputs specified by D. Use a Karnaugh map to obtain a minimum cost Product-of-sum (POS) expression for the output F. Show all loops clearly.

$F(w, x, y, z) = \sum m(1, 6, 11, 12)$
$D(w, x, y, z) = \sum m(7, 10, 13, 14, 15)$

(8 marks)

3. (a) State whether each of the following statements is TRUE or FALSE.

- An N-input decoder has 2N outputs.
- An n-input multiplexer requires $\log_2(n)$ select bits.
- When using structural gate-level primitives in Verilog module, order of statements is important.
- Identifiers in Verilog can start with letters, numbers, underscore (_) and dollar ($).
- Sensitivity list must contain all signals that affect output.

(5 marks)

(b) Sketch each of the following logic gates which is implemented using only 2:1 multiplexer:

- NOT gate
- AND gate
- OR gate

(6 marks)

Note: Question No. 3 continues on Page 4

(c) Determine the function of the schematic shown in Figure Q3 and write a Verilog module using ***if-else*** statement. The module will have two inputs (A, B) and one output (Y).

(6 marks)

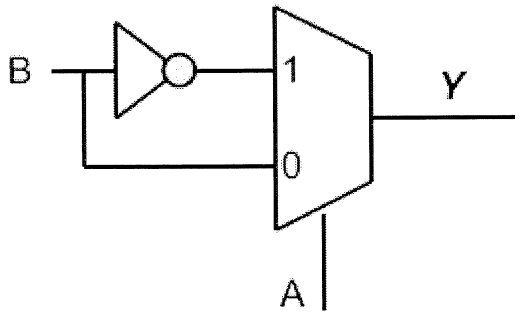

Figure Q3

(d) There are four doors in an auditorium. In order to best manage the crowd, only one door is opened at any one time. You are to design a circuit based on a 2x4 decoder which will guide the guests to the opened door. The input to the circuit is a 2-bit binary number. The circuit has four outputs. Each output controls a light bulb that is placed above each door. You are required to write a Verilog module to implement this circuit using ***case*** statements.

(8 marks)

4. (a) Determine the value of a and b for the following Verilog code segments and briefly explain the reasons for your answer. Assume initial value of a = 10.

(i)
```
always@(posedge clk)
  begin
    a = a + 1;
    b = a + 1;
  end
```

(ii)
```
always@(posedge clk)
  begin
    a <= a + 1;
    b <= a + 1;
  end
```

(6 marks)

Note: Question No. 4 continues on Page 5

(b) Figure Q4a shows a 3-bit binary counter with two inputs (***CLK*** & ***RESET***) and one 3-bit output (***Q[2:0]***). The initial state of the counter is ***Q[0] = Q[1] = Q[2] = 0***. Based on the schematic shown in Figure Q4a:

(i) Complete the timing diagram shown in Figure Q4b. Assume the counter is at initial state and the reset signal is low.

(7 marks)

(ii) Determine whether the counter shown in Figure Q4a is an up or a down counter.

(2 marks)

(iii) Write a Verilog module for the 3-bit counter that you have determined in Q4(b)(ii).

(6 marks)

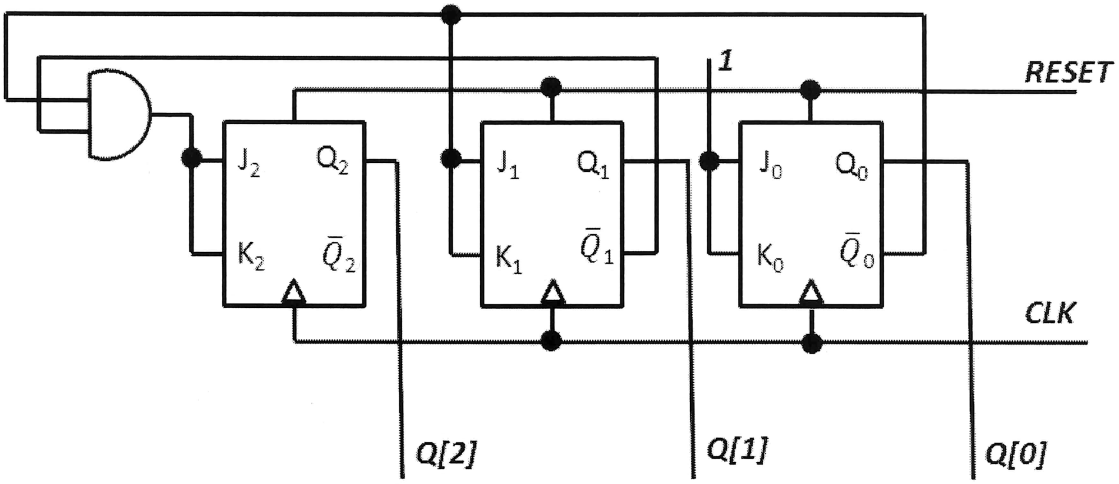

Figure Q4a

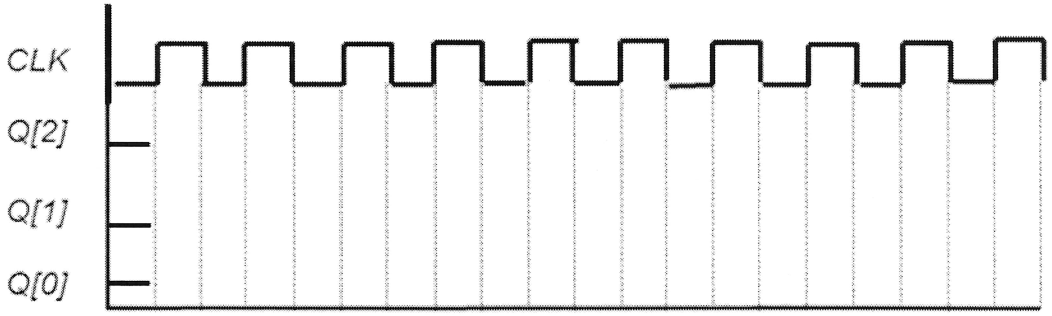

Figure Q4b

Note: Question No. 4 continues on Page 6

(c) Figure Q4c shows a FSM which detects a particular bit sequence. Determine the output sequence for the following sequence of inputs:

- 0,0,1,1,1,0,1,1,1,1,0,1

(4 marks)

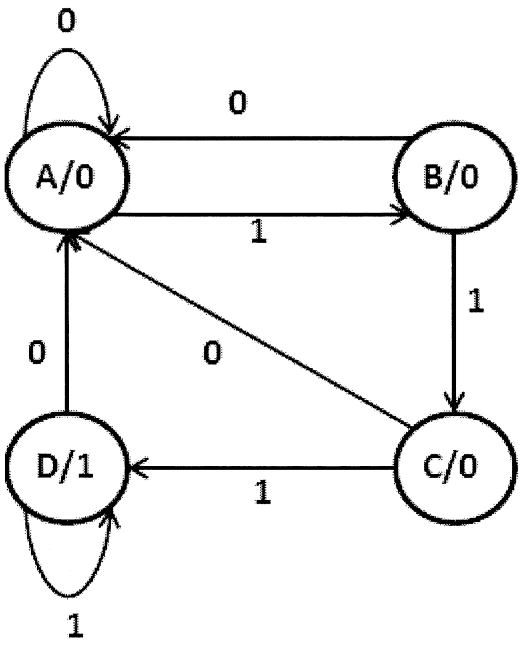

Figure Q4c

END OF PAPER

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Please read the following instructions carefully:

1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.