Roll: 1703100

Requirements:

- ✓ Word size of CPU - 6
- ✓ ALU Operations - XOR, NOT
- ✓ Register Number - 3
- ✓ Size of RAM – 7, so address line = 3 bit
- ✓ Word Size of RAM and ISA - 18
- ✓ Register Mode - Y
- ✓ Immediate Mode - Y
- ✓ JLE – Y

ISA Design:

- ISA format of ALU Instruction (Register Mode) is:

Opcode (3 bit)		Ra	Rb	Unused
2 bits	1 bit	2 bits	2 bits	11 bits
00	Operation 0 = XOR 1 = NOT	(00 - 11)	(00 - 11)	xxxx xxxx xxx

Example: XOR Ra, Rb: 00 0 00 01 00000000000

- ISA format of ALU Instruction (Immediate Mode) is:

Opcode (3 bit)		Ra	Value	Unused
2 bits	1 bit	2 bits	6 bits	7 bits
01	Operation 0 = XOR 1 = NOT	(00 - 11)	(000000 - 111111)	xxxx xxx

Example: XOR Ra, Value: 01 0 00 000100 0000000

- ISA format of Branching Mode is:

Opcode (3 bit)		Address	Unused
2 bits	1 bit	3 bits	12 bits
10	Operation 0 = JLE	(000 - 111)	xxxx xxxxx

Example: JLE Address: 10 0 100 000000000000

ROM Module:

Address	Code	Instructions	ROM (Physical Address)	Mode
000	XOR R1,R2	00 0 01 10 00000000000	03000	Register Mode
001	NOT R0	00 1 00 0000000000000	08000	Register Mode
010	XOR R1,7	01 0 01 000111 0000000	12380	Immediate Mode
011	NOT R2	01 1 10 0000000000000	1C000	Immediate Mode
100	JLE 4	10 0 100 000000000000	24000	Branching
101	XOR R0,7	01 0 00 000111 0000000	00800	Immediate Mode
110	XOR R0,R1	00 0 00 01 00000000000	10380	Register Mode
111	JLE 3	10 0 011 000000000000	23000	Branching