BARC 2021

12th Annual Boston Area Architecture Workshop

January 29, 2021

Bringing together computer architecture community in the Greater Boston area and beyond.

Each year BARC is composed of numerous informal 15-30 minute presentations, long discussion breaks sessions, and talks by notable community members doing interesting things in computer architecture. As always, elegant as well as preliminary solutions to architectural problems are welcome. This year we have excellent talks lined up, and we hope you'll enjoy them and learn something new in the process. Please reach out to the presenters with questions, collaboration ideas, insights, or comments.

The goal of BARC is to provide a forum for computer architects in the Greater Boston area and beyond to get together and present/discuss the 'latest and greatest' in the area of computer architecture. Each year, community members discuss current ideas and concepts in Microarchitecture, Multicore/manycore processors, GPUs, Memory systems, I/O, Networking and communication, Low power systems, Adaptive and hybrid systems, Architectures based on emerging technologies, Accelerator-based architectures, Embedded processing, Performance evaluation techniques, and more!

Directions

BARC 2021 will be held virtually. Login info and any schedule changes will be announced on the workshop's website, https://bostonarch.github.io/2021/.

Schedule

BARC 2021 is a single-day workshop occurring on January 29, 2021. The workshop will begin at 8:45 am Eastern Standard Time (EST), with the first talk at 9:00am EST and the last talk expected to end at 6:00pm EST.

Morning session starts at 9AM EST at https://mit.zoom.us/j/98053942371
Afternoon session starts at 1PM EST at https://mit.zoom.us/j/93979355599
Tutorial starts at 4PM EST at https://mit.zoom.us/j/96193004619
J-Core AMA starts at 5PM EST at https://mit.zoom.us/j/97731992575

The complete schedule is listed on the following page.

BARC 2021, Presentation Schedule

URLs will be posted Friday morning. All times EST

8:45-9:00		Welcome
9:00–9:30	Olof Kindgren	SERV : The World's Smallest RISC-V (AMA)
9:30–10:00	Anne Elster	The European Factor: Europe´s Impact on Computing & Processors
10:00–10:30	Xi Wang, Brody Williams, Nathan Stoddard	xBGAS: Extended Base Global Address Space for High Performance Computing
10:30-11:00	Theodore Omtzigt, Peter Marosan	Introducing the Cambridge Architecture
11:00-11:30	Pantea Kiaei, Yuan Yao, Patrick Schaumont	Real-time Detection and Adaptive Mitigation of Power-based Side-Channel Leakage in SoC
11:30-12:00	Xinfei Guo	Cross-layer Codesign for Resilient Hardware
12:00-12:30	Ron Minnich	Building small stateless network-controlled appliances with linuxboot and Plan 9's cpu command
12:30-1:00	Lunch/ Discussion	
1:00-1:30	Udit Gupta, Young Geun Kim, Sylvia Lee, Jordan Tse, Hsien-Hsin S. Lee, Gu-Yeon Wei, David Brooks, Carole-Jean Wu	Illuminating the Elusive Carbon Footprint of Computing
1:30-2:00	Connor Kenyon, Glenn Volkema, Gaurav Khanna	Overcoming Limitations of GPGPU-Computing in Scientific Applications
2:00–2:30	Casey Nelson, R. Iris Bahar, Tamara Lehman	Investigating the Potential for Near Data Processing to Reduce Secure Memory Overheads
2:30–3:00	Trinayan Baruah, Yifan Sun, Ali Tolga Dincer, Saiful A Mojumder, José L Abellán, Yash Ukidave, Ajay Joshi, Norman Rubin, John Kim, David Kaeli	Griffin: Hardware-Software Support for Efficient Page Migration in Multi-GPU Systems
3:00–3:30	Samuel Hsia, Mark Wilkening, Udit Gupta, Caroline Trippel, Carole-Jean Wu, David Brooks, Gu-Yeon Wei	Cross-Stack Characterization and Solid State Drive-Based Near Data Processing for Recommendation Workloads
3:30–4:00	Samuel Thomas, Tamara Lehman, R. Iris Bahar, Joseph Izraelevitz	Partial Recovery of Secure Non-Volatile Main Memories
4:00–5:00	Steven Hoover	Tutorial: Transaction-Level Verilog and its Ecosystem
5:00–6:00	Rob Landley, D. Jeff Dionne	Why the J-core Open Processor is Cool (AMA)