J1 — SNESConn

Pin	Signal		Signal	Pin
1	PA0	PA1	2	PA1_snes
3	PA2	PA3	4	PA3_snes
5	PA4	PA5	6	PA5_snes
7	PA6	PA7	8	PA7_snes
9	PAWR_n	PARD_n	10	PARD_n_snes
11	D0	D1	12	D1_snes
13	D2	D3	14	D3_snes
15	D4	D5	16	D5_snes
17	D6	D7	18	D7_snes
19	RST_n	VCC_5V	20	VCC5
21	SMP_CLK	DOT_CLK	22	DOT_CLK_snes
23	GND	EXPAND	24	
25	MONO-OUT	IRQ_n	26	IRQ_n_snes
27	SL_IN	SR_IN	28	

Inputs: PA0_snes, PA2_snes, PA4_snes, PA6_snes, PAWR_n_snes, D0_snes, D2_snes, D4_snes, D6_snes, RST_n_snes, SMP_CLK_snes

GND / VCC5

U1 — 74LVCH1T45

Pin	Signal
1	VccA (VCC3_3)
2	GND
3	A — PAWR_n_fpga
6	VccB (VCC5)
5	DIR — PAWR_n_DIR_fpga
4	B — PAWR_n_snes

C1 10p, GND

U2 — 74LVCH1T45

Pin	Signal
1	VccA (VCC3_3)
2	GND
3	A — RST_n_fpga
6	VccB (VCC5)
5	DIR — RST_n_DIR_fpga
4	B — RST_n_snes

C2 10p, GND

U3 — 74LVCH1T45

Pin	Signal
1	VccA (VCC3_3)
2	GND
3	A — PARD_n_fpga
6	VccB (VCC5)
5	DIR — PARD_n_DIR_fpga
4	B — PARD_n_snes

C3 10p, GND

U4 — 74LVCH1T45

Pin	Signal
1	VccA (VCC3_3)
2	GND
3	A — IRQ_n_fpga
6	VccB (VCC5)
5	DIR — IRQ_n_DIR_fpga
4	B — IRQ_n_snes

C4 10p, GND

U5 — 74ALVC164245

Pin	Signal		Signal	Pin
1	1DIR (PA_DIR_fpga)	1OE_n	48	
2	1B0 (PA0_snes)	1A0	47	PA0_fpga
3	1B1 (PA1_snes)	1A1	46	PA1_fpga
4	GND	GND	45	
5	1B2 (PA2_snes)	1A2	44	PA2_fpga
6	1B3 (PA3_snes)	1A3	43	PA3_fpga
7	VccB	VccA	42	VCC3_3
8	1B4 (PA4_snes)	1A4	41	PA4_fpga
9	1B5 (PA5_snes)	1A5	40	PA5_fpga
10	GND	GND	39	
11	1B6 (PA6_snes)	1A6	38	PA6_fpga
12	1B7 (PA7_snes)	1A7	37	PA7_fpga
13	2B0 (D0_snes)	2A0	36	D0_fpga
14	2B1 (D1_snes)	2A1	35	D1_fpga
15	GND	GND	34	
16	2B2 (D2_snes)	2A2	33	D2_fpga
17	2B3 (D3_snes)	2A3	32	D3_fpga
18	VccB	VccA	31	
19	2B4 (D4_snes)	2A4	30	D4_fpga
20	2B5 (D5_snes)	2A5	29	D5_fpga
21	GND	GND	28	
22	2B6 (D6_snes)	2A6	27	D6_fpga
23	2B7 (D7_snes)	2A7	26	D7_fpga
24	2DIR (D_DIR_fpga)	2OE_n	25	

GND / VCC5 / VCC3_3

U6 — 74LVCH1T45

Pin	Signal
1	VccA (VCC3_3)
2	GND
3	A — DOT_CLK_fpga
6	VccB (GND)
5	DIR (VCC5)
4	B — DOT_CLK_snes

C5 10p, GND

U7 — 74LVCH1T45

Pin	Signal
1	VccA (VCC3_3)
2	GND
3	A — SMP_CLK_fpga
6	VccB (GND)
5	DIR (VCC5)
4	B — SMP_CLK_snes

C6 10p, GND

LEDs

- LEDG_0_fpga — R1 200R — LED1 Green — GND
- LEDG_1_fpga — R2 200R — LED2 Green — GND
- VCC5 — R3 270R — LED3 Red — GND

J2 — DE0nanoIDC_40

Pin	Signal		Signal	Pin
1	GPIO_X_IN0 (SMP_CLK_fpga)	GPIO_X0	2	
3	GPIO_X_IN1 (DOT_CLK_fpga)	GPIO_X1	4	
5	GPIO_X2	GPIO_X3	6	
7	GPIO_X4	GPIO_X5	8	
9	GPIO_X6 (LEDG_0_fpga)	GPIO_X7	10	
11	VCC_5v	GND	12	LEDG_1_fpga
13	GPIO_X8 (PARD_n_fpga)	GPIO_X9	14	PARD_n_DIR_fpga
15	GPIO_X10 (PAWR_n_fpga)	GPIO_X11	16	PAWR_n_DIR_fpga
17	GPIO_X12 (RST_n_fpga)	GPIO_X13	18	RST_n_DIR_fpga
19	GPIO_X14 (IRQ_n_fpga)	GPIO_X15	20	IRQ_n_DIR_fpga
21	GPIO_X16 (PA0_fpga)	GPIO_X17	22	PA_DIR_fpga
23	GPIO_X18 (PA2_fpga)	GPIO_X19	24	PA1_fpga
25	GPIO_X20 (PA4_fpga)	GPIO_X21	26	PA3_fpga
27	GPIO_X22 (PA6_fpga)	GPIO_X23	28	PA5_fpga
29	VCC_3v	GND	30	
31	GPIO_X24 (D0_fpga)	GPIO_X25	32	PA7_fpga
33	GPIO_X26 (D2_fpga)	GPIO_X27	34	D1_fpga
35	GPIO_X28 (D4_fpga)	GPIO_X29	36	D3_fpga
37	GPIO_X30 (D6_fpga)	GPIO_X31	38	D5_fpga
39	GPIO_X32 (D_DIR_fpga)	GPIO_X33	40	D7_fpga

VCC3_3 / GND

Decoupling Capacitors

VCC3_3: C7, C8, C9, C10 — 100n
VCC5: C11, C12, C13, C14 — 100n
GND

Title Block

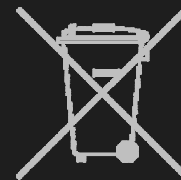| Title	SNES Extension Header to IDC Header (with translation)
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Number	RNG-0003
Revision	B
Date	6/28/2015
Sheet	1 of 1
File	C:\Users\..\maxout_conn.SchDoc
Drawn By	Evan Custodio

RNG DESIGNS

SNES-Tap

Rev B
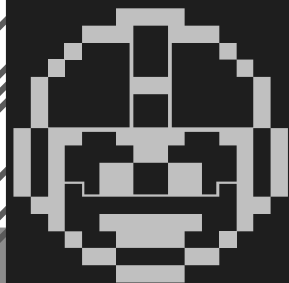
2015 @defparam

RNG
DESIGNS

5.38 (cm)

SNES PWR

FPGA LED 0

FPGA LED 1

Board S