LINFINITY MICROELECTRONICS

SG1525A/SG2525A/SG3525A
SG1527A/SG2527A/SG3527A

REGULATING PULSE WIDTH MODULATOR

DESCRIPTION

The SG1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lower external parts count when used to implement all types of switching power supplies. The on-chip +5.1 volt reference is trimmed to ±1% initial accuracy and the input common-mode range of the error amplifier includes the reference voltage, eliminating external potentiometers and divider resistors. A Sync input to the oscillator allows multiple units to be slaved together, or a single unit to be synchronized to an external system clock. A single resistor between the C_T pin and the Discharge pin provides a wide range of deadtime adjustment. These devices also feature built-in soft-start circuitry with only a timing capacitor required externally. A Shutdown pin controls both the soft-start circuitry and the output stages, providing instantaneous turn-off with soft-start recycle for slow turn-on. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for input voltages less than that required for normal operation. Another unique feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The SG1525A output stage features NOR logic, giving a LOW output for an OFF state. The SG1527A utilizes OR logic which results in a HIGH output level when OFF.

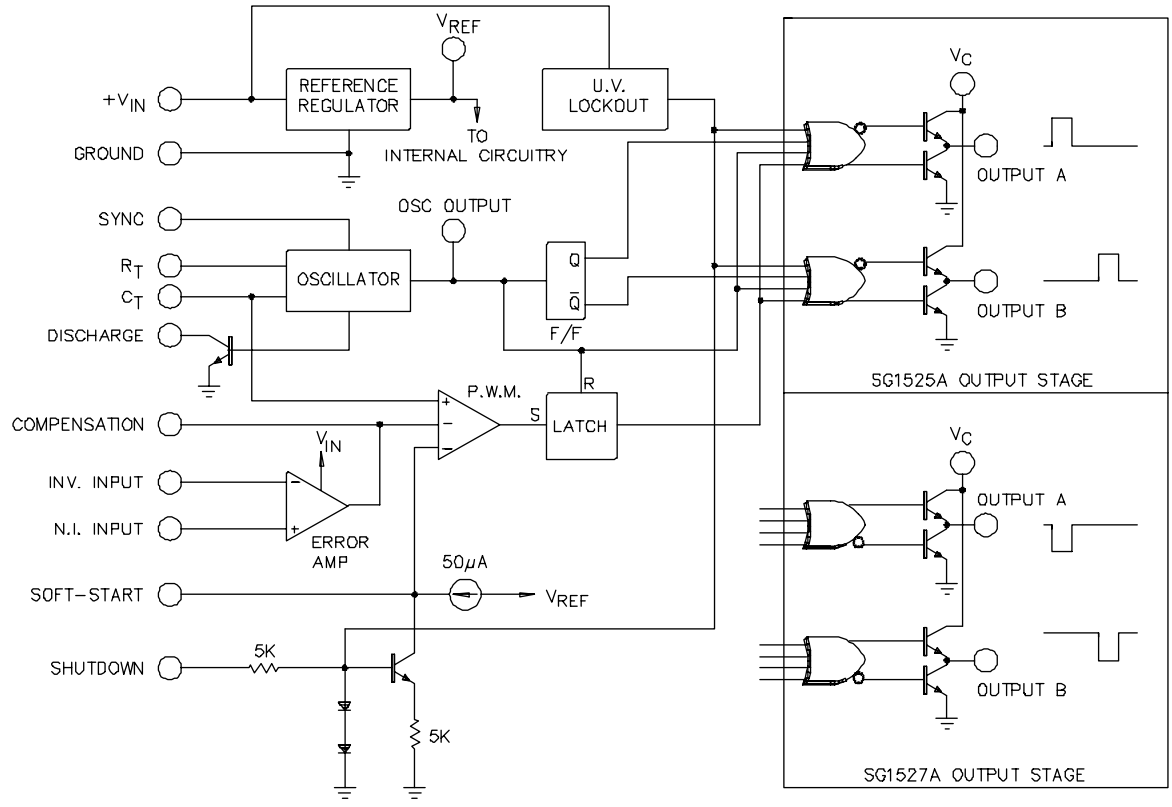
FEATURES

- **8V to 35V operation**
- **5.1V reference trimmed to ±1%**
- **100Hz to 500KHz oscillator range**
- **Separate oscillator sync terminal**
- **Adjustable deadtime control**
- **Internal soft-start**
- **Input undervoltage lockout**
- **Latching P.W.M. to prevent multiple pulses**
- **Dual source/sink output drivers**

HIGH RELIABILITY FEATURES - SG1525A, SG1527A

- ♦ **Available to MIL-STD-883B**
- ♦ **MIL-M38510/12602BEA - JAN1525AJ**
- ♦ **MIL-M38510/12604BEA - JAN1527AJ**
- ♦ **Radiation data available**
- ♦ **LMI level "S" processing available**

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ($+V_{IN}$) 40V
Collector Supply Voltage (V_C) 40V
Logic Inputs ..... -0.3V to 5.5V
Analog Inputs ..... -0.3V to V_{IN}
Output Current, Source or Sink 500mA
Reference Load Current 50mA
Oscillator Charging Current 5mA
Operating Junction Temperature Range
  Hermetic (J, L Packages) ..... 150°C
  Plastic (N, DW Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1. Values beyond which damage may occur.

THERMAL DATA

J Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 30°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 80°C/W
DW Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 40°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 95°C/W
L Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 35°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 120°C/W
N Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 40°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 65°C/W

Note A. Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
Note B. The above numbers for θ_{JC} are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θ_{JA} numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage ($+V_{IN}$) ..... 8V to 35V
Collector Voltage (V_C) ..... 4.5V to 35V
Sink/Source Load Current (steady state) ..... 0 to 100mA
Sink/Source Load Current (peak) ..... 0 to 400mA
Reference Load Current ..... 0 to 20mA
Oscillator Frequency Range ..... 100Hz to 350KHz
Oscillator Timing Resistor (R_T) ..... 2KΩ to 150KΩ
Deadtime Resistor Range (R_D) ..... 0Ω to 500Ω
Maximum Shutdown Source Impedance 5KΩ
Oscillator Timing Capacitor (C_T) ..... 0.001µF to 0.1µF
Operating Ambient Temperature Range
  SG1525A/SG1527A ..... -55°C to 125°C
  SG2525A/SG2527A ..... -25°C to 85°C
  SG3525A/SG3527A ..... 0°C to 70°C

Note 2: Range over which the device is functional.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1525A/SG1527A with -55°C ≤ T_A ≤ 125°C, SG2525A/SG2527A with -25°C ≤ T_A ≤ 85°C, SG3525A/SG3527A with 0°C ≤ T_A ≤ 70°C, and $+V_{IN}$ = 20V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section								
Output Voltage	T_J = 25°C	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V_{IN} = 8V to 35V		10	30		10	30	mV
Load Regulation	I_L = 0 to 20mA		20	50		20	50	mV
Temperature Stability (Note 3)	Over Operating Temperature Range		20	50		20	50	mV
Total Output Voltage Range (Note 3)	Over Line, Load and Temperature	5.00		5.20	4.95		5.25	V
Short Circuit Current	V_{REF} = 0V, T_J = 25°C		80	100		80	100	mA
Output Noise Voltage (Note 3)	10Hz ≤ f ≤ 10KHz, T_J = 25°C		40	200		40	200	µVrms
Long Term Stability (Note 3)	T_J = 125°C		20	50		20	50	mV/khr

Note 3. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 4. F_{OSC} = 40KHz (R_T = 3.6KΩ, C_T = 0.01µF, R_D = 0Ω)
Note 5. Applies to SG1525A/2525A/3525A only, due to polarity of output pulses.

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ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Oscillator Section (Note 4)								
Initial Accuracy	T_J = 25°C	37.6	40	42.4	37.6	40	42.4	KHz
Voltage Stability	V_{IN} = 8V to 35V		±0.3	±1		±1	±2	%
Temperature Stability (Note 3)	MIN ≤ T_J ≤ MAX		±3	±6		±3	±6	%
Minimum Frequency (Note 3)	R_T = 150KΩ, C_T = 0.1µF			150			150	Hz
Maximum Frequency (Note 3)	R_T = 2KΩ, C_T = 1nF	350			350			KHz
Current Mirror	I_{RT} = 2mA	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude		3.0	3.5		3.0	3.5		V
Clock Width	T_J = 25°C	0.3	0.5	1.0	0.3	0.5	1.0	µs
Sync Threshold		1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V		1.0	2.5		1.0	2.5	mA
Error Amplifier Section (V_{CM} = 5.1V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	10		1	10	µA
Input Offset Current				1			1	µA
DC Open Loop Gain	R_L ≥10MΩ, T_J = 25°C	60	75		60	75		dB
Gain-Bandwidth Product (Note 3)	A_V = 0dB, T_J = 25°C	1	2		1	2		MHz
Output Low Level			0.2	0.5		0.2	0.5	V
Output High Level		3.8	5.6		3.8	5.6		V
Common Mode Rejection	V_{CM} = 1.5V to 5.2V	60	75		60	75		dB
Supply Voltage Rejection	V_{IN} = 8V to 35V	50	60		50	60		dB
P.W.M. Comparator Section								
Minimum Duty Cycle	V_{COMP} = 0.6V			0			0	%
Maximum Duty Cycle	V_{COMP} = 3.6V	45	49		45	49		%
Input Threshold (Note 4)	Zero Duty Cycle	0.6	0.9		0.6	0.9		V
	Maximum Duty Cycle		3.3	3.6		3.3	3.6	V
Input Bias Current			.05	2.0		.05	2.0	µA
Soft-Start Section								
Soft Start Current	$V_{SHUTDOWN}$ = 0V	25	50	80	25	50	80	µA
Soft Start Voltage	$V_{SHUTDOWN}$ = 2V		0.4	0.6		0.4	0.6	V
Shutdown Input Current	$V_{SHUTDOWN}$ = 2.5V		0.4	1.0		0.4	1.0	mA
Output Drivers Section (each transistor, V_C = 20V)								
Output High Level	I_{SOURCE} = 20mA	18	19		18	19		V
	I_{SOURCE} = 100mA	17	18		17	18		V
Output Low Level	I_{SINK} = 20mA		0.2	0.4		0.2	0.4	V
	I_{SINK} = 100mA		1.0	2.2		1.0	2.2	V
Undervoltage Lockout	V_{COMP} and V_{SS} = High	6	7	8	6	7	8	V
Collector Leakage (Note 5)	V_C = 35V			200			200	µA
Rise Time	C_L = 1nF, T_J = 25°C		100	600		100	600	ns
Fall Time	C_L = 1nF, T_J = 25°C		50	300		50	300	ns
Shutdown Delay (Note 3)	V_{SD} = 3V, C_S = 0, T_J = 25°C		0.2	0.5		0.2	0.5	µs
Total Standby Current								
Standby Current	V_{IN} = 35V		14	20		14	20	mA

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OSCILLATOR SECTION

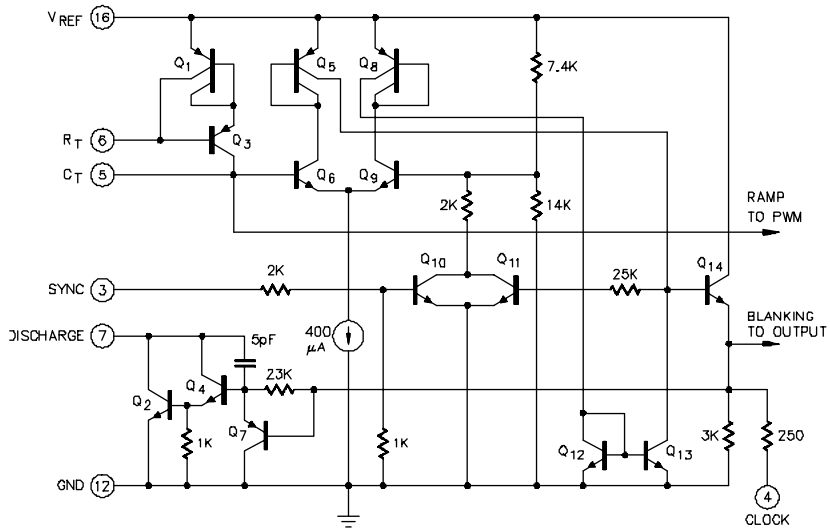

FIGURE 1 - OSCILLATOR SCHEMATIC

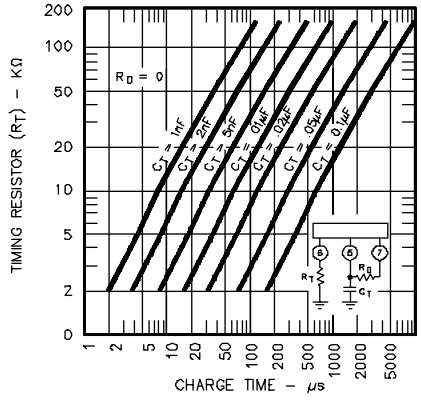

FIGURE 2 - OSCILLATOR CHARGE TIME VS. R_T AND C_T

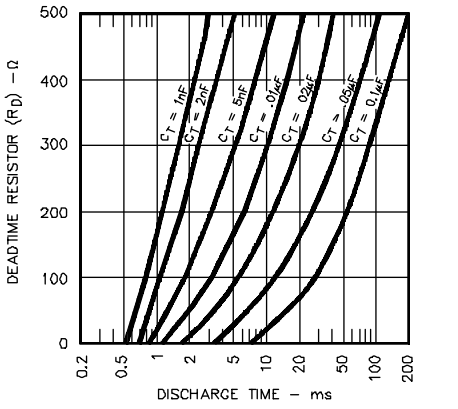

FIGURE 3 - OSCILLATOR DISCHARGE TIME VS. R_D AND C_T

ERROR AMPLIFIER SECTION

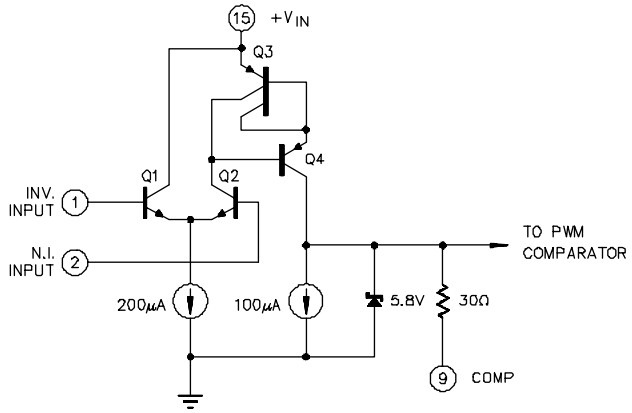

FIGURE 4 - ERROR AMPLIFIER

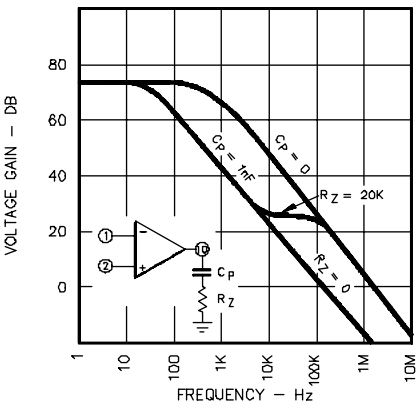

FIGURE 5 - ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE

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OUTPUT SECTION

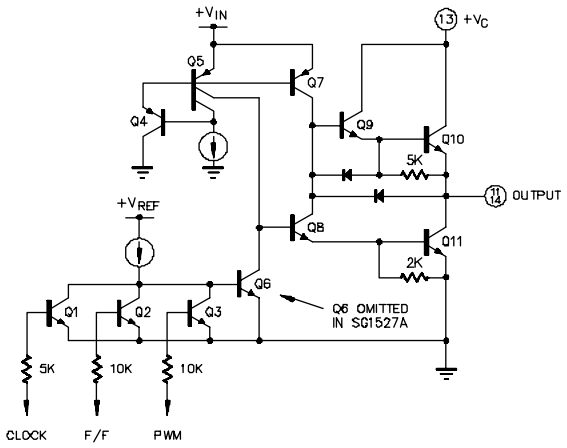


FIGURE 6 -OUTPUT CIRCUIT (½ Circuit Shown)

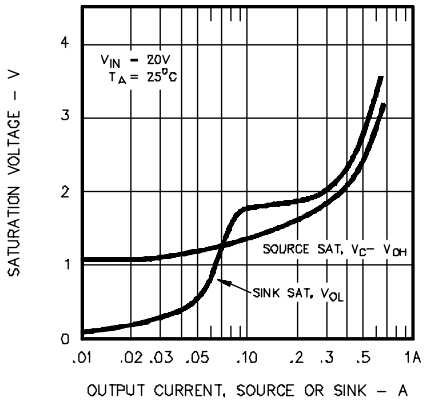
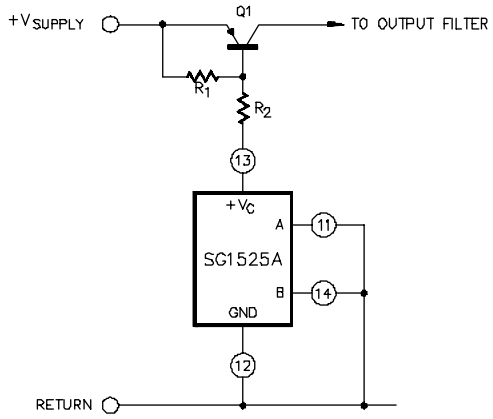
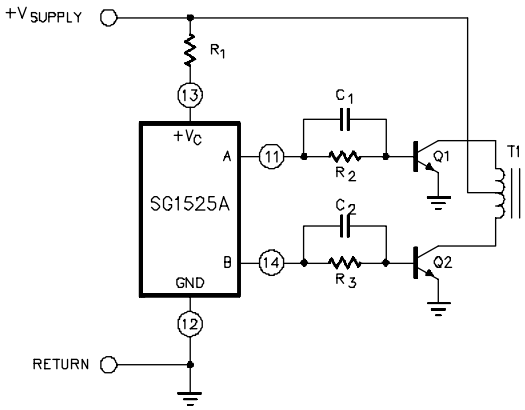


FIGURE 7 - OUTPUT SATURATION CHARACTERISTICS

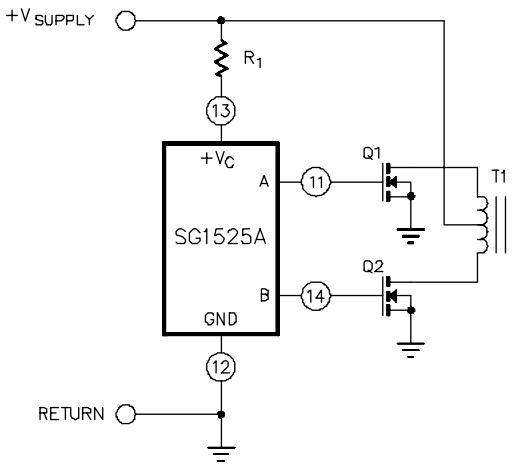
APPLICATION INFORMATION



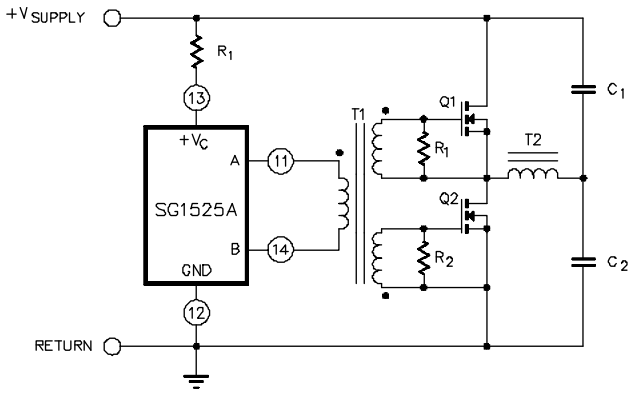
For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.



In conventional push-pull bipolar designs, forward base drive is controlled by R_1 - R_3 . Rapid turn-off times for the power devices are achieved with speed-up capacitors C_1 and C_2 .



The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.



Low power transformers can be driven directly by the SG1525A. Automatic reset occurs during deadtime, when both ends of the primary winding are switched to ground.

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APPLICATION INFORMATION (continued)

SHUTDOWN OPTIONS

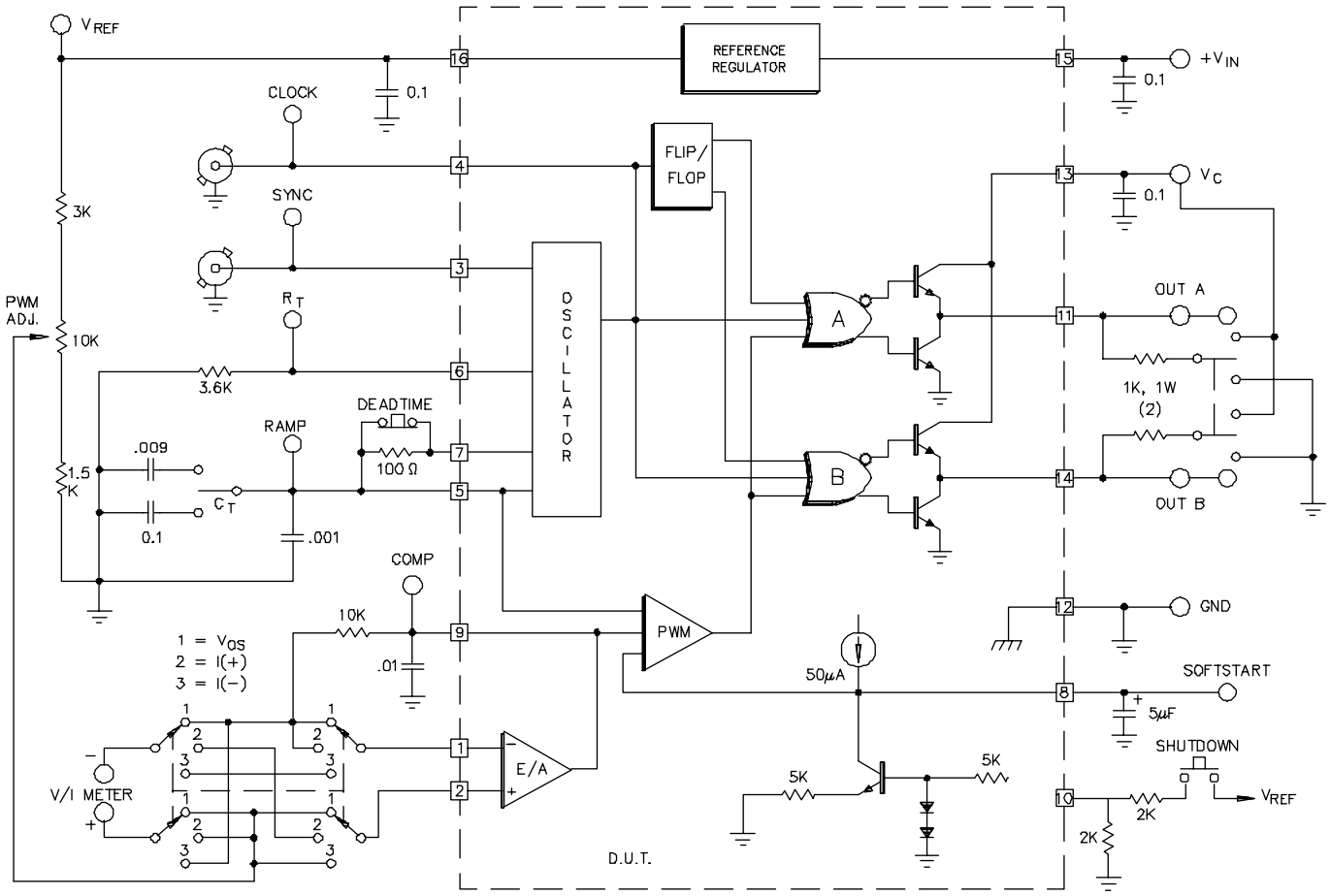
1. Use an external transistor or open-collector comparator to pull down on the Comp terminal. This will set the PWM latch turning off both outputs. If the shutdown signal is momentary, pulse-by-pulse protection can be accomplished as the PWM latch will be reset with each clock pulse.

2. The same results can be accomplished by pulling down on the Soft-Start terminal with the difference that on this pin, shutdown will not affect the amplifier compensation network but must discharge any Soft-Start capacitor.

3. Apply a positive-going signal to the Shutdown terminal. This will provide most rapid shutdown of the outputs but will not immediately set the PWM latch if there is a Soft-Start capacitor. This capacitor will discharge but with a current of approximately twice the charging current.

4. The shutdown terminal can be used to set the PWM latch on a pulse-by-pulse basis if there is no external capacitance on Soft-Start terminal. Slow turn-on may still be accomplished by applying an external capacitor, blocking diode, and charging resistor to the comp terminal. (See SG1524 Application Note).

SG1525A/1527A LAB TEST FIXTURE



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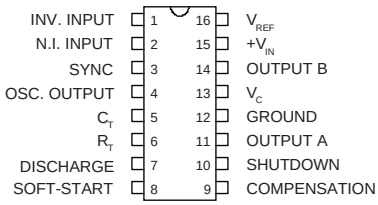
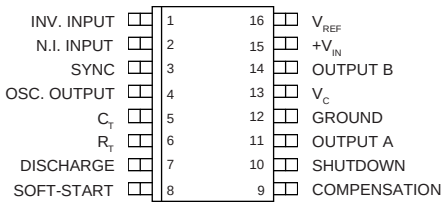
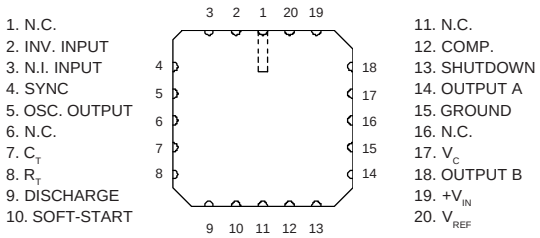
CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG1525AJ/883B JAN1525AJ SG1525AJ/DESC SG1525AJ SG2525AJ SG3525AJ SG1527AJ/883B JAN1527AJ SG1527AJ/DESC SG1527AJ SG2527AJ SG3527AJ	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
16-PIN PLASTIC DIP N - PACKAGE	SG2525AN SG3525AN SG2527AN SG3527AN	-25°C to 85°C 0°C to 70°C -25°C to 85°C 0°C to 70°C	
16-PIN WIDE BODY PLASTIC S.O.I.C. DW - PACKAGE	SG2525ADW SG3525ADW SG2527ADW SG3527ADW	-25°C to 85°C 0°C to 70°C -25°C to 85°C 0°C to 70°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG1525AL/883B SG1525AL SG1527AL/883B SG1527AL	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

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