HardwareX 6 (2019) e00085

Contents lists available at ScienceDirect

HardwareX

journal homepage: www.elsevier.com/locate/ohx

Low-cost active electromyography

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ARTICLE INFO

Article history:
Received 22 August 2019
Received in revised form 7 October 2019
Accepted 11 October 2019

Keywords:
EMG
Rehabilitation
Right leg driver
Bar electrodes
Bio-sensing
Bio-instrumentation

ABSTRACT

Electromyography (sEMG) is the technique applied to measure the bio-potential signal produced by a contracting skeletal muscle. sEMG has been used for subject intention estimation, force estimation, limb angle estimation and determining muscle activation timing. Typically most sEMG devices on the market, and in literature, are not open source hardware. This results in a device that can be considered as a black box, as it is difficult to determine the applied signal processing. This paper presents an open source low-cost active sEMG circuit, allowing an understanding of sEMG and the challenges involved in designing a high quality device. An open source sEMG design reduces the time and cost associated with initial sEMG research, providing a larger number of researchers with the opportunity to utilise sEMG. The device has been tested on three subjects, resulting in a low baseline noise $\leqslant 5.2\,\mu V_{rms}$ and great line noise rejection, resulting in a sensitive device that can capture high quality bio-potential signals.

Specifications table:

Hardware name	POLE (Portable Open source Low-cost Electromyography) Sensor
Subject area	• Bio-engineering • Mechatronics Engineering • Electrical engineering • Physiotherapy • Bio-mechatronics
Hardware type	• Electromyography • Bio-sensing • Bio-instrumentation • Field measurements and sensors
Open source license	Creative Commons Attribution-NonCommercial-ShareAlike 4.0 International
Cost of hardware	USD $112 (for one), USD $750 (for ten)
Source file repository	available with the article

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https://doi.org/10.1016/j.ohx.2019.e00085

1. Hardware in context

Surface electromyography (sEMG) is the non-invasive technique applied to measure the bio-potential signal produced by a contracting skeletal muscle, and there is a need for low cost open source sEMG. The skeletal muscle is controlled by the motor unit and its associated alpha motor system, consisting of the lower motor neuron, its axon and the various muscle fibres it innervates [1,2]. Voltage-gated ion channels located in the axon control the flow of various ions within close proximity. The binary state of the voltage-gated ion channels are controlled by their electric potential. If there is a large enough spatial and temporal summation of excitatory potentials, the sodium ion voltage-gated channels open, resulting in an inrush of sodium ions. The sudden influx of sodium ions depolarises the cell, causing an action potential. When an action potential travels down the axon and reaches the synapses, a neurotransmitter is released. The release of the neurotransmitter causes a breakdown of the ionic barrier of the muscle tissues. This process creates a motor unit action potential (MUAP), causing the muscle fibres to contract. The recorded amplitude of the MUAP is a function of muscle tissue, muscle fibre diameter, the distance the depolarisation must travel along the muscle fibre to the recording electrode, electrode properties and the subject's adipose tissue layer. The MUAP is the bio-electric signal captured by an sEMG device [3,4]. The bio-potential is a bipolar signal with an amplitude of $\leqslant$10 mV pk-pk, which contains its useful energy within the frequency range of 0–500 Hz, [5,6]. sEMG has been used for subject intention estimation, force estimation, limb angle estimation and determining the level of muscle activation [7–10]. These properties can be used in many applications, including physiotherapy and biomechanics research.

The sEMG device outlined in this paper consists of two silver bar electrodes, a reference electrode, a pre-amplification stage, a low-pass filter, a high-pass filter in the form of an AC-coupler, a right leg driver (RLD) to reduce common mode noise, and an analogue-to-digital converter (ADC). A high level block diagram is shown in Fig. 1.

2. Hardware description

Commercial, research-level sEMG devices can be expensive, and are not open source hardware, resulting in a device that must be treated as a black box, as it is difficult to determine the applied signal processing. This sEMG circuit has been designed due to the need for a low cost, portable sEMG device that has high quality near-raw signal output with adjustable gain and an open signal processing architecture. The device uses an active bipolar electrode configuration with silver bar electrodes. The design implements a band-pass filter and a RLD. The analog signal is digitised with a 24-bit sigma-delta ADC. These design choices, in combination with being an open source design reduce common challenges with sEMG.

2.1. Customisation

The biggest driving factor to designing this sEMG device was the requirement for capturing high quality bio-potentials while knowing and understanding the applied signal processing techniques. Occasionally a commercially available sEMG device will provide their schematics [11], but component values and part numbers are not given. To produce a fully customisable device, an understanding of the bio-potential origin and sEMG limitations must be understood. This open source sEMG documentation details design choices around minimising sEMG limitations, saving time and money for future researchers and designers.

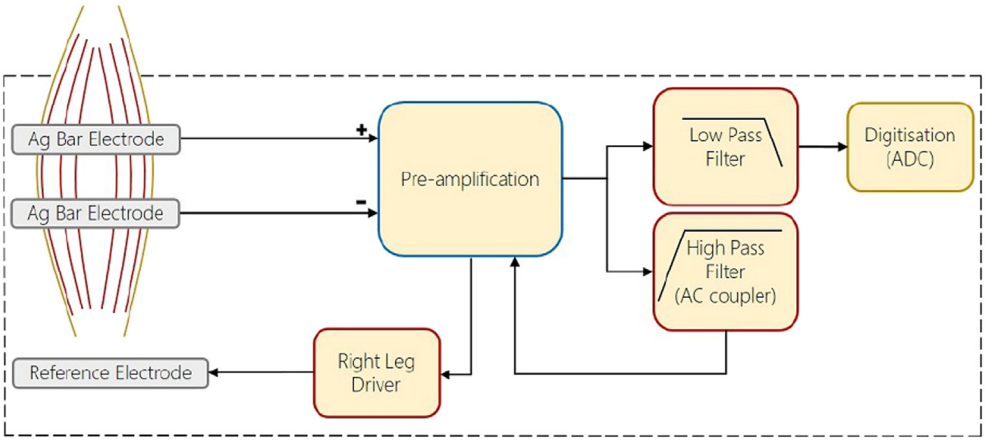

Fig. 1. High level block diagram of the sEMG device.

2.2. Noise and filtering

One of the biggest challenges with sEMG is noise reduction. Two major forms of noise are due to coupled electromagnetic interference (EMI) and motion artefact, which get superimposed onto the bio-potential signal. EMI gets capacitively coupled to the subject's body and detected by the sEMG device, where the dominant source is the surrounding AC line noise. This coupled EMI is low frequency (50–60 Hz) and appears as a common-mode voltage; however, an impedance imbalance between recording electrodes can convert common-mode voltage to differential-mode voltage [12]. Motion artefact is a low frequency interference ($\leqslant$ 20 Hz) that is produced by relative motion between the electrodes and the recording surface, or motion of the cables that link the electrodes and the sEMG device. This sEMG device applies design techniques to reduce current limitations.

In the rare case that a schematic of an sEMG design has been supplied, mains interference is commonly reduced by implementing either a notch filter, simply relying on the common mode rejection ratio (CMRR) of the instrumentation amplifier [13,14,11], or the use of post-processing [15,16]. The notch filter not only attenuates the coupled EMI, but also frequencies of interest within close proximity. Secondly, the notch filter does not attenuate the multiple harmonics associated with the coupled EMI. Post-processing of the signal can increase processing power requirements, decrease throughput rate or result in a device that is non-real-time. A RLD [17] is typically the best method of EMI suppression, driving the inverted common-mode voltage back onto the subject, cancelling the effect from the coupled EMI whilst maintaining signal quality in the pass-band. A RLD is real-time and attenuates the wide band of coupled EMI, not only the coupled mains frequency.

The use of a 20–500 Hz band-pass filter is typical in sEMG design. The filter helps to remove motion artefact (low frequency) and high frequency noise. However, a first order band-pass filter may not provide enough attenuation, resulting in aliasing and motion artefact. Designing the sEMG circuit into the recording electrodes (active electrodes) is an effective method to reduce motion artefact. Active electrodes eliminate the need for cables linking the electrodes to the recording device, and the electrodes typically have a fixed spacing, removing the possibility of relative motion between the electrode pair. Inadequate removal of coupled EMI reduces the signal-to-noise ratio (SNR), limiting the sensitivity of the device.

The signal amplitude is dependent on many task-specific factors: muscle group of interest, adipose layer thickness, type of exercise and contraction strength; therefore, the gain of the sEMG device should be adjustable to accommodate these variable requirements over different subjects and tasks. However, adjusting the gain should not affect the filtering characteristics. The design outlined in this paper combines all necessary filter requirements to produce an open source device that is capable of capturing high quality, low latency *raw* sEMG signals. The applied methods are outlined in Table 1 and further detailed in Section 5.3.

2.3. Cost

Commercial research level sEMG devices can be expensive. Low-cost sEMG is becoming more readily available but are limited by the aforementioned challenges. This design is low-cost (USD $112 for one, USD $750 for ten) and as this design is open source, it makes the device easily adaptable to the researcher/designer's needs. The sEMG design is modular and some aspects can be removed as desired. If the sEMG design will be used on a specific subject and task, the digital gain adjustment can be removed, and the device gain set to a specific value without degrading device performance. If the digital conversion is not required because a high quality data acquisition system is used, the ADC can be removed, reducing cost while maintaining a high quality signal. Even though high quality components have been used, the result is still a low-cost high quality module.

2.4. Digital system

The sEMG signal is sampled and digitised using an on-board ADC, resulting in a low-latency, high-resolution, low-noise device that benefits from both analogue and digital techniques. Having a digital output increases immunity to noise, which is particularly useful in situations where sources of noise are in close proximity. Having an inbuilt 24-bit sigma-delta (Σ-Δ) ADC that the design is optimised for, results in a high quality sEMG signal that is independent of the microcontroller operating it. A device that is dependent on an unknown ADC means the anti-aliasing filter of the sEMG device may not function as intended and result in reduced signal quality. Typically, microcontrollers come with inbuilt 10- to 13-bit ADCs; however, these are usually SAR type ADCs, which are better suited for capturing high frequency signals with lower precision when

Table 1
Summary of the applied techniques by this design to reduce common sEMG challenges.

Interference	Reduction Method
Coupled EMI	Active electrodes and right leg driver
Motion artefact	Active electrodes, fixed electrode spacing and AC-coupler
Inherent circuit noise	64th order low pass digital filter
Anti-aliasing	Analog filter meeting ADC requirements
Signal amplitude variance	24-bit ADC and adjustable filter gain

compared to Σ-Δ ADCs; therefore, using the ADC proposed in this sEMG device provides greater resolution and linear response while simplifying the design of the anti-aliasing filter. Another benefit of having the ADC incorporated into the sEMG device is the four on-board GPIO pins. These are used to control a digital potentiometer, resulting in adjustable gain control through the digital interface. This allows real-time, repeatable, fine adjustment gain control of the analogue signal.

2.5. Electrodes

Commonly, sEMG devices are designed to use single-use clip-on self-adhesive silver-silver chloride (Ag-AgCl) electrodes. This chemical composition is used as it is less sensitive to electrolyte concentration and has a low DC offset associated with the half-cell potential, however, they do have disadvantages. Ag-AgCl electrodes are single use, needing to be replaced every time a new recording site or subject is required. The adhesive surface typically requires a large area, producing a large inter-electrode distance ($\geqslant$20 mm), resulting in less sensitive recordings being more susceptible to crosstalk. This sEMG design resolves these issues by using 1 mm round 99.99% pure silver wire for the recording electrodes. This configuration produces a 1 $\times$ 10 mm electrode, with a 10 mm interelectrode spacing, minimising crosstalk from nearby muscles [18], Fig. 2. Using silver instead of Ag-AgCl has the disadvantage of having a larger DC offset associated with the half-cell potential, resulting in a lower pre-amplifier gain. A single-use clip-on self-adhesive Ag-AgCl electrode ($\geqslant$20 mm diameter) placed on an electrically neutral part of the subject's body is used as the reference electrode, driven by the RLD.

2.6. Summary

Raw sEMG is the most versatile signal type, as it allows the researcher to apply custom signal processing. The previous iteration of this sEMG design, [19], has been used for crosstalk detection and removal [20,21], simultaneous sEMG detection during electrical stimulation [22], muscle torque estimation [9] and assist-as-need exoskeleton control [10]. This design, although composed of existing methods, being an open source design results in a large step forward for low-cost high quality sEMG devices.

- Low-cost portable high quality bio-sensing
- Voluntary assist-as-need exoskeleton control
- Muscle activation levels and/or timing
- Muscle recovery monitoring

3. Design files

Although proprietary software has been used in the development process of this EMG device, all files required to manufacture and understand the operation of the product are supplied in an open source file format.

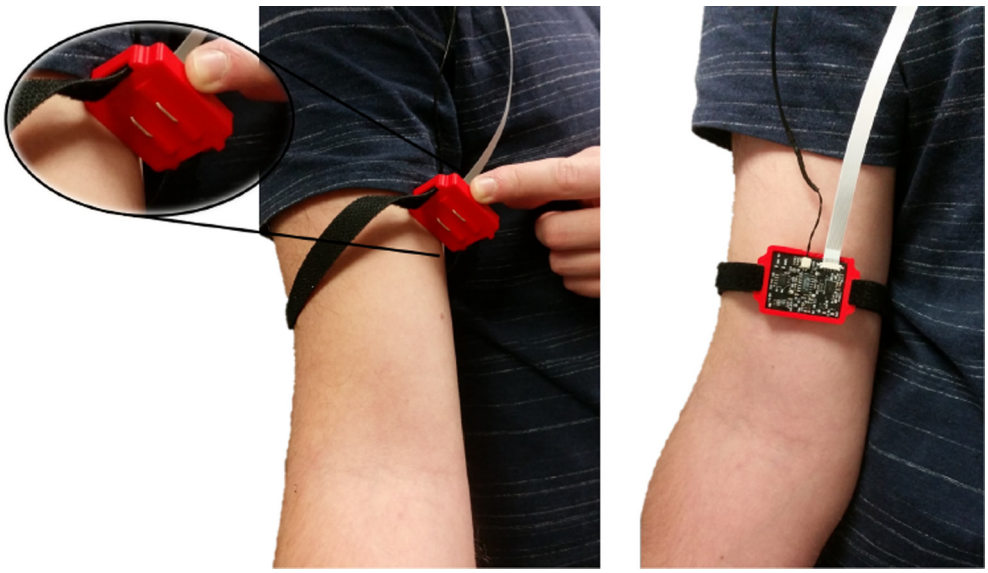

Fig. 2. Electrode position for recording from the biceps brachii. The white flat flexible cable connects to the microcontroller. The black cable is the right leg driver cable, typically attached to the elbow when recording from the biceps brachii.

3.1. Altium files

The sEMG circuit was developed using Altium Designer (18.1.9, Altium Limited). As Altium is proprietREQUIREDary software, PDF schematics have also been supplied. EMG_project_altium.zip contains the schematic library, PCB library, compiled library, schematic files (Analog.SchDoc, Digital.SchDoc, Power.SchDoc), the PCb project document and a rules file containing the design constraints for JLCPCB (the chosen PCB manufacturer). Although not tested with this design, the open source *Altium2kicad* package may convert the Altium files to open source cross platform KiCad EDA (5.1.2, KiCAD) files.

3.2. Bill of materials

A complete, editable bill of materials (BOM) has been provided for the sEMG board.

3.3. Gerber and drill files

A cable adapter board was designed in case the user does not want to use the FFC connection, further detailed in Section 5.1. The Gerber and drill files are the files that are required to be sent to the PCB manufacturer. Files for both the sEMG board and the cable adapter board are provided.

3.4. 3D printing

To provide a non-conductive housing for the sEMG board, that supports the PCB and the silver bar electrodes, a 3D printed case was designed, the STL file is provided. A block with the width of 9 mm was also produced to permit easy bending of the silver bar. The STL file is included.

3.5. Arduino file

An example Arduino script is provided. It sets the required on-board registers, permits adjustable gain and captures the ADC data. This example script was used to capture the data for the results outlined in Section 7.

3.6. Design files summary

Design filename	File type	Open source license	Location of the file
EMG_project_altium.zip	Altium project	CC BY–NC–SA 4.0	Available with the article
EMG.pdf	pdf Schematic	CC BY–NC–SA 4.0	Available with the article
EMG_BOM.xlsx	BOM spreadsheet	CC BY–NC–SA 4.0	Available with the article
EMG_gerber_files.zip	Gerber and drill files	CC BY–NC–SA 4.0	Available with the article
cable_adapter.zip	Gerber and drill files	CC BY–NC–SA 4.0	Available with the article
EMG_case.STL	3D print file	CC BY–NC–SA 4.0	Available with the article
electrode_spacing.STL	3D print file	CC BY–NC–SA 4.0	Available with the article
EMG_example_code.ino	Ardiuino script	CC BY–NC–SA 4.0	Available with the article

4. Bill of materials

Designator	Component	Number	Cost per unit (USD)	Total cost (USD)	Source of materials
J1	2 Position Header	1	$0.44	$0.44	Digi-key
J2,3	99.99% Pure Silver 1 mm Round Wire	0.06 m	$8.30	$0.5	Regal Castings Ltd.
J4	6 pin FFC connector	1	$1.17	$1.17	Digi-key
U1	24-bit ADC	1	$12.96	$12.96	Digi-key
U2	quad op-amp	1	$10.91	$10.91	Digi-key
U3	Instrumentation Amplifier	1	$10.52	$10.52	Digi-key
U4	Digital Potentiometer	1	$2.89	$2.89	Digi-key
U5	3.3 V Regulator	1	$2.36	$2.36	Digi-key

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Designator	Component	Number	Cost per unit (USD)	Total cost (USD)	Source of materials
U6	2.5 V Regulator	1	$1.48	$1.48	Digi-key
U7	−2.5 V Regulator	1	$4.62	$4.62	Digi-key
Vcm1	Red LED	1	$0.14	$0.14	Digi-key
TP	Test Points	7	$0.24	$1.68	Digi-key
PCB	PCB and Stencil	5 PCBs (minimum qty.) 1 Stencil	$2 for five, $8.86	$41.21 shipped to NZ	JLCPCB

5. Build instructions

5.1. Overview

An overview of the design process of the sEMG board is outlined below and shown in Fig. 3.

1. Order components and PCB
2. Populate the sEMG board with everything but the electrodes
3. Bend the silver wire around the electrode spacing block to produce the silver electrodes
4. Place the sEMG board into the 3D printed housing and populate the silver bar electrodes
5. Solder the reference electrode cable to the RLD cable and connect the RLD and SPI cables to the sEMG board
6. Connect the SPI line from the sEMG device to the microcontroller and program the microcontroller to obtain the data from the ADC.

The sEMG board has a 6 pin FFC connector that keeps the connection slim, but it means another surface mount FFC connector must be used. If the sEMG design is to be used without making a PCB that the microcontroller and FFC connector mounts to, the cable adapter board can be used. The cable adapter board converts the FFC style connector to a standard through hole male pin header with 2.54 mm spacing (breadboard/vero board spacing). For the FFC to FFC connection, the longest tested cable was 228 mm (9 inch). If a longer cable is desired, terminating the SPI data lines with a series resistor will slow down the signal edges, improving signal integrity [23]. When using the cable-adapter board, the jumper wires that

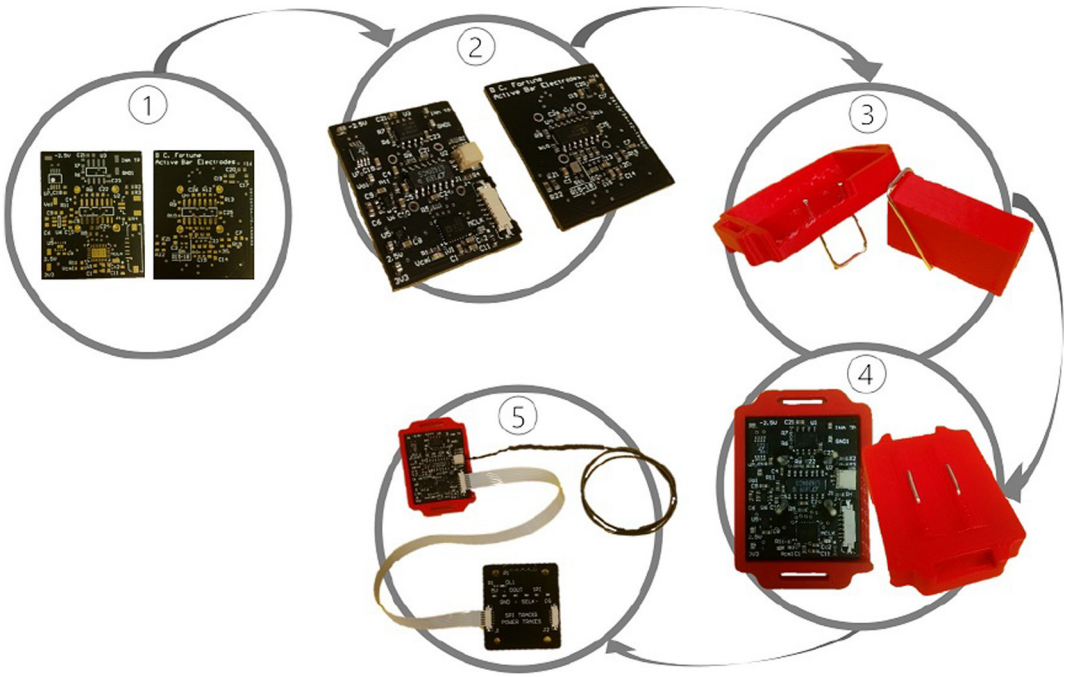

Fig. 3. Assembly process of the EMG board. The EMG board is shown to be connected to the cable adapter board in the final stage.

connect to the chosen microcontroller are required to be short, otherwise the transmission lines become noisy, resulting in loss of data. The transmission line using the FFC to male pin header was successfully tested with the same FFC cable (228 mm) and 50 mm jumper wire. Although the maximum length was not tested, it may be possible to have longer jumper wires without sacrificing signal transition integrity.

5.2. Risks

As the sEMG board is interfacing with the human body there can be risks: the risk level is dependent on the power supply system. The sEMG device was designed to operate from a battery, this removes the risk associated with AC powered bench-top supplies. In rare cases the power supply can cause current loops with the power grid, this should be avoided. When using a power supply that is connected to mains and/or connected to a computer, the device should be isolated. This can be done by using an isolated DC-DC converter and/or USB isolator. However, using a battery and a regulator is the simplest option and also results in a portable device.

The current sEMG device is designed to operate from a **5 V power supply, with 3.3 V CMOS logic**. If 5 V digital logic levels are required, an off-board logic level shifting IC is the easiest method, other possible options are described in Section 5.3.2.

5.3. Design decisions

Beyond the design decisions outlined in Section 2, particular requirements further defined the specific component choice. As the system had to be multi-channel capable, the number of interfacing wires was kept to a minimum, and the device size compact. Ideally the device voltage would be high to take advantage of the CMRR capabilities of the instrumentation amplifier, but there is a trade-off with size and number of wires interfacing the sEMG board to the microcontroller. The design schematics are comprised of three sheets: analog system (INA.SchDoc), digital system (ADC.SchDoc), and the power supplies (power.SchDoc). A high level schematic is outlined in Fig. 4.

5.3.1. Digital system

With a device that involves an analogue-to-digital conversion, it is best to define the ADC first. The bipolar signal has an amplitude of $\leqslant$10 mV pk-pk, containing its useable energy within 0–500 Hz, but predominantly in the range of 50–150 Hz [6]; therefore, a minimum sampling rate of 1 kHz with a high precision is required. The most suitable ADC architecture for a low frequency, high precision signal is Σ-Δ, as this type of architecture typically has a high number of bits and implements oversampling.

As the signal is bipolar, there are multiple options for the ADC input method: single-ended input ADC with a DC offset being applied to the signal; a differential input ADC, by applying the bipolar signal to the inverting input, and a positive

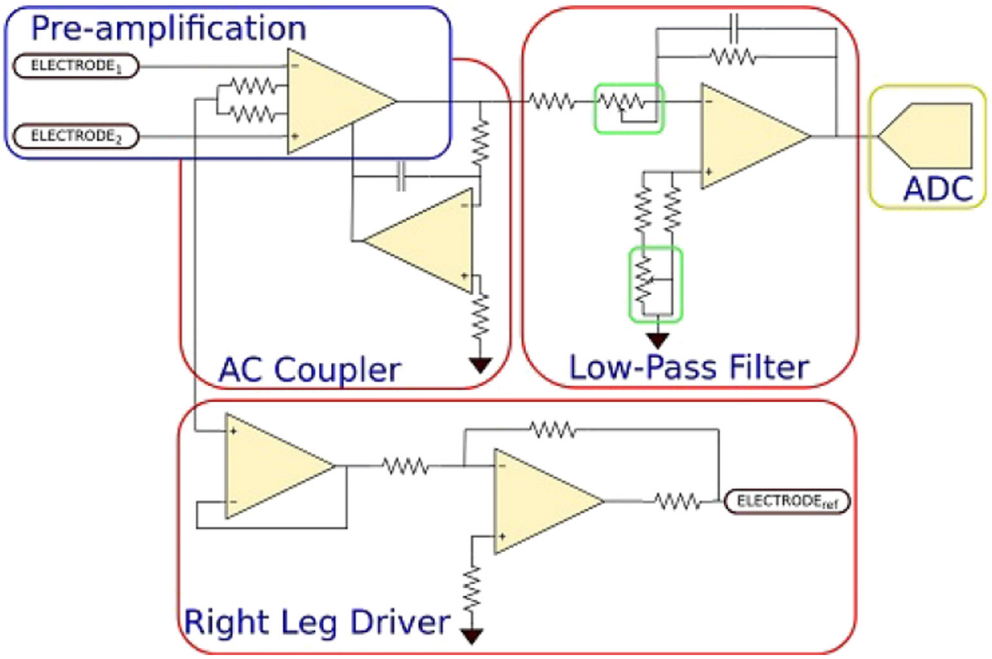

Fig. 4. High level sEMG schematic. Coloured boxes correspond to individual integrated circuits.

voltage to the non-inverting pin to offset the differential voltage; or a true bipolar ADC. Applying a shift to the bipolar signal without increasing the component count minimises the options. The most feasible option is to apply a shift within the filtering stage; however, this requires the filtering op-amps to have an asymmetric split power supply. Having an asymmetric split power supply decreases the op-amps power supply rejection ratio and removes ADC input voltage protection. Using the differential option is also limited as some ADCs require the individual analog inputs to be within the supply voltage rails. This means that the ADC requires a negative rail that matches the rest of the device and a positive rail that is twice the analogue positive supply voltage. The method used to avoid increasing component count, while ensuring the signal was within the ADC input limit is to use a true bipolar ADC. The input signal is single-ended, but there are a greater number of options available for a differential input ADC.

To make the sEMG device adaptable to many projects, an ADC that can operate from either 3.3 V or 5 V digital logic was required. Ideally the serial interface would be I^2C (fewer wires), but SPI is the only option when applying the other ADC criteria. A development board that met these criteria, while providing a fast and powerful solution with on-board data storage (SD card) is the Teensy 3.5 and 3.6. Therefore, the sEMG device was designed around the 3.3 V digital logic of the Teensy 3.6.

5.3.1.1. ADC (U1: AD7768-1). Analog Device's AD7768-1 was the chosen ADC, and is configured in SPI mode to increase device flexibility. The ADC pin connections and associated design choices are outlined in Table 2. The ADC has a programmable 64th order finite impulse response (FIR) filter, where both power consumption and bandwidth are tunable. A 2.048 MHz CMOS clock is used as recommend by the ADC manufacturer for lower power consumption [24]. The output data rate (ODR) is a function of the master clock frequency, MCLK, master clock divider factor, MCLK_divider, and a decimation factor, Eq. (1),

$$\mathrm{ODR} = \frac{\mathrm{MCLK}}{\mathrm{MCLK\_divider} \cdot \mathrm{Decimation}} = \frac{2.048 \times 10^6}{2 \cdot 1024} = 1000\ \mathrm{Hz} \tag{1}$$

The FIR filter pass-band and cutoff frequency are a function of the ODR, Eqs. (2) and (3) respectively. The ODR was chosen to be 1 kHz, meeting the required minimum sampling frequency while producing a cutoff frequency of 430 Hz. The next available sampling frequency is 2 kHz, resulting in a FIR filter cutoff frequency of 860 Hz.

$$\mathrm{Passband} = 0.4 \times \mathrm{ODR} = 400\ \mathrm{Hz} \tag{2}$$

$$\mathrm{Cutoff} = 0.43 \times \mathrm{ODR} = 430\ \mathrm{Hz} \tag{3}$$

Table 2
Summary of the ADC connections.

Pin No.	Mnemonic	Note
1	$\overline{\text{RESET}}$	NC, controlled through SPI register write
2	$\overline{\text{SYNC IN}}$	Connect to $\overline{\text{SYNC OUT}}$
3	$\overline{\text{SYNC OUT}}$	Synchronises the ADC with MCLK
4	REGCAPD	Decouples an internal regulator
5	IOVDD	Internal digital voltage supply
6	$\overline{\text{PIN}}$/SPI	Pull high, sets ADC to SPI mode
7	DGND	Digital ground
8	CLKSEL	Clock type selection controlled through SPI register write
9	DOUT	MISO, the mnemonic are with respect to the ADC
10	SCLK	SPI clock
11	SDI	MOSI
12	$\overline{\text{CS}}$	Active low chip select
13	XTAL1	Tie to ground when using CMOS clock
14	MCLK	Connect to external CMOS oscillator chip
15	GPIO_0	Digital potentiometer, Mode control selection
16	GPIO_1	Digital potentiometer, Channel selection
17	GPIO_2	Digital potentiometer, Increment/decrement mode selection
18	GPIO_3	Digital potentiometer, Increment/decrement wiper position
19	$\overline{\text{DRDY}}$	Can obtain through SPI, pin DOUT/$\overline{\text{RDY}}$
20	REGCAPA	Decoupling of an internal regulator
21	AVSS	−2.5 V, provided to operate in true bipolar mode
22	AVDD2	+2.5 V, analogue supply voltage
23	AVDD1	+2.5 V, analogue supply voltage
24	REF+	+2.5 V, provides full positive voltage swing
25	REF-	−2.5 V, provides full negative voltage swing
26	AIN-	Re-inverts the signal after filtering stage
27	AIN+	Permits single-ended inverting true bipolar ADC configuration
28	VCM	LED is used for debugging

5.3.2. Voltage supplies

The sEMG device operates from a single 5 V supply. The voltage is split and regulated into ± 2.5 V and 3.3 V, producing the largest possible bipolar voltage range that permits both 3.3 V and 5 V digital logic options. An advantage of the ADC is its capability to operate from both 3.3 V and 5 V digital logic. Switching the digital logic level requires changing the CMOS clock, the IOVDD voltage (bypass the 3.3 V regulator), and the GPIO voltage divider (outlined in Section 5.3.3.2.5); however, the current CMOS clock cannot be replaced by an equivalent 5 V option as there is no 5 V device that shares the footprint. To make this design more versatile, the CMOS clock footprint should be replaced by one that is common to both 3.3 V and 5 V logic levels. Although changing the digital logic voltage has not been tested, the ADC should operate correctly [24].

Three on-board voltage regulators are required: −2.5 V, 2.5 V and 3.3 V. The voltage regulator from the ADP7104 family (ADP7104ARDZ-3.3-R7) was selected as recommended by the ADC manufacturer. The remaining regulators must also operate from a 5 V supply and have a small form factor. As the sEMG device has a low current draw, inductor-less charge pump regulators are the best option, and using separate regulators to provide the split supply provides a larger range of solutions. This resulted in the use of the LTC1550LCMS8-2.5 for the −2.5 V supply and the REG710NA-2.5/250 for the 2.5 V supply. Even though not all parts of the device have been introduced yet, a summary of the voltage supply distribution is outlined in Table 3.

5.3.3. Analogue system

The analogue system is comprised of three subsystems: pre-amplification, filtering and adjustable gain. The pre-amplification system amplifies the bio-potential difference of the electrical signal detected on the electrodes with respect to the reference. The filtering stage is comprised of a quad operational amplifier (op-amp) for the analogue signal processing. A digital potentiometer is used to adjust the gain of the analogue signal.

5.3.3.1. Pre-amplification (U3: INA128U). The pre-amplification of the differential signal with respect to the reference is performed using an instrumentation amplifier. The differential voltage associated with the half-cell potential produces a 10 mV DC offset when adequate skin preparation is performed. To prevent pre-amplification saturation, while providing head room for less adequate skin preparation, the pre-amplifier gain is set to 50. The pre-amplifier is not required to be rail-to-rail, as an AC-coupler circuit (Section 5.3.3.2.3) is used to remove DC offsets within a ±2.5 V range, and the bio-potential signal after pre-amplification has a maximum amplitude of 0.5 V pk-pk (10 mV pk-pk × 50).

The INA128 was the selected instrumentation amplifier as it has the required performance: high CMRR (110 dB minimum over the pass band), low noise ($10\,nV/\sqrt{Hz}$ in the pass band) and the common-mode input voltage range for a supply voltage of ±2.5 V was ±0.5 V minimum. The resistance required to achieve a gain of 50 is 1020 Ω with the INA128. To provide a centre tap, permitting access to the common-mode voltage needed for the RLD (Section 5.3.3.2.2), two gain resistors of 510 Ω were used. A second generation of this chip has been released (INA828), however, it has not been tested in this design.

5.3.3.2. Filtering (U2: LT6204). The signal conditioning process has three stages: RLD, AC coupler and the low-pass filter. A quad op-amp package provided a compact solution. The LT6204 quad op-amp package met the required performance: ±2.5 V power supply, rail-to-rail for both input and output, unity gain stability, and a gain bandwidth product of 100 kHz; however, the LT6204 requires input bias current compensation.

5.3.3.2.1. Input bias current. Input bias currents cause erroneous DC offsets. The bias current flowing through an op-amp's input resistor produces a voltage at the input terminals, biasing the input voltage and producing a DC offset. To minimise erroneous voltage offsets, a compensation resistor that is equal to the parallel combination of the input and feedback resistances is required. This will not remove all error associated with the input bias current as the currents are not truly equal (input offset current $\neq 0$) and vary with temperature.

5.3.3.2.2. Right leg driver, RLD. The RLD operates as a feedback loop with the subject, minimising interference by driving the inverted common-mode voltage onto the subject. The RLD in this sEMG design follows the design outlined in [17]. The quad op-amp has two pairs of matched op-amps. The match pair, op-amp A and op-amp D, are used for the RLD. As the feedback resistor to the RLD is far greater than the input resistance, the input bias current compensation resistor is equal to the input resistance.

5.3.3.2.3. AC coupler. The AC coupler is an integrating op-amp circuit providing feedback to the instrumentation amplifier's reference, removing DC offset while attenuating low frequency noise. The cutoff frequency of the AC coupler is defined in the

Table 3
Summary of voltage rail distribution. Coloured boxes correspond to integrated circuits outlined in Fig. 4.

Device	−2.5 V	2.5 V	3.3 V
Pre-amplification	V−	V+	·
Quad op-amp	V−	V+	·
Digital potentiometer	V_SS	V_DD	·
CMOS clock	·	·	V_CC
ADC	AVSS, REF−	AVDD1, AVDD2, REF+	IOVDD, $\overline{PIN}$/SPI

same way as a first order RC filter. A 21.2 Hz cutoff frequency was obtained by using a 10 μF capacitor and a 750 Ω resistor. As the AC coupler is comprised of only one resistive component, the compensation resistor is equal to the filtering resistor (750 Ω).

5.3.3.3. Adjustable Gain (U4: AD5222). The gain of the low-pass filter is tunable in real-time, producing a device that can record over a range of muscles, contraction strength, and different adipose layer thicknesses. The AD5222 was the only digital potentiometer that met the required performance: ±2.5 V power supply, ensuring the analogue signals do not saturate; controllable through the GPIO pins; dual channel, permitting real-time tuning of both gain resistor and input bias compensation resistor. The AD5222 comes in a 10 kΩ option; however, the resistance tolerance is ±30%. A digital logic voltage divider is also required as the maximum digital input is 2.8 V.

5.3.3.3.1. Designing the GPIO voltage divider. The voltage divider was designed to meet two requirements: current draw and noise margins. The ADC's GPIO can source 500 μA, and the potentiometer's digital input draws ±1 μA. The logic high output from the ADC (2.64–3.3 V) is required to be within the logic high input range of the digital potentiometer (2.0–2.8 V), Fig. 5. The divider network is formed from a 39 kΩ and a 220 kΩ resistor. The maximum current draw is 12.7 μA and the digital potentiometer input voltage range is 2.21–2.77 V, inclusive of the voltage associated with the digital potentiometer's input transistor bias current.

5.3.3.3.2. GPIO connections. The digital potentiometer requires all four ADC GPIO pins, connections and functionality outlined in Table 4. The digital potentiometer is configured as a rheostat, pin A and pin W are tied together as a fail safe, prohibiting the filter from open loop gain.

5.3.3.3.3. Low-pass filter. A first order active low-pass filter with a cutoff frequency of 459 Hz was designed to meet the ADC's anti-aliasing requirements. The real-time 64th order digital low-pass filter results in a device cutoff frequency of 430 Hz, Section 5.3.1.1. The anti-aliasing filter has a gain of 4.74–68 V/V, resulting in a sEMG device gain of 237–3400 V/V. This range in gain ensures the sEMG device can capture the maximum expected signal (10 mv pk-pk) while being sensitive enough to capture weak contractions.

6. Operation instructions

6.1. Software

The ADC is configured by writing to its registers; however, the registers utilise volatile memory. All register executions (except reading the 24-bit signal data) are 8-bits long. Configuring some settings requires writing to multiple 8-bit registers, a detailed list of register functionality is described in [24], pg 66. The register configuration process requires pulling chip select low, writing an initial 8-bits comprised of an active low frame bit (0), a read (1) or write (0) bit and a 6-bit register address, followed by the 8 bit data that is to be read or written. An example script has been developed using the Arduino

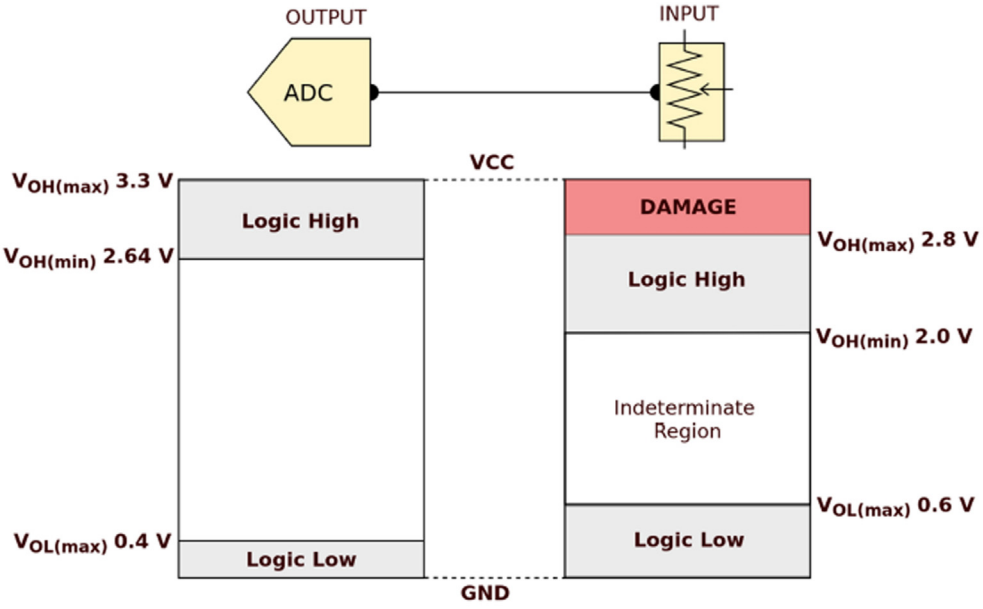

Fig. 5. A voltage divider must be used to lower the logic levels from the ADC output to prevent exceeding the maximum input voltage of the digital potentiometer, preventing potential latch up.

Table 4
Summary table for the AD5222 digital potentiometer connections, values in the square brackets indicates the logic level required to implement that function.

Pin No.	GPIO	Mnemonic	Functions
1	·	B_1	Channel 1 input
2	·	A_1	Fail safe
3	·	W_1	Channel 1 output
4	·	V_{ss}	Negative power supply
5	·	W_2	Channel 2 output
6	·	A_2	Fail safe
7	·	B_2	Channel 2 input
8		GND	Analogue ground
9	**0**	MODE	Independent **[1]**/dependent **[0]** wiper control
10	**1**	DACSEL	Increment channel 1 **[0]** or channel 2 **[1]**
11	**2**	$U/\overline{D}$	Increase **[1]**/decrease **[0]** wiper position on CLK pulse
12	**3**	CLK	Increment channel(s) **[pulse]**
13	·	$\overline{CS}$	Chip select
14	·	V_{DD}	Positive power supply

IDE to obtain data from the ADC using a Teensy 3.6, "EMG_example_code.ino". This example contains comments that outline why each instruction has been performed.

Digital gain and offset permit individual ADC calibration. Both metrics are 24-bit, signed, two's complement registers, formed from three 8-bit registers. As the digital gain does not increase the analogue accuracy, it is set to 1. To maintain the true bipolar nature of the system, the offset is set to 0. Eq. 4 outlines how the digital gain and offset registers effect the output data,

$$\text{Data} = \left[\frac{3 \times \text{V\_IN}}{\text{V\_REF}} \times 2^{21} - \text{Offset}\right] \times \frac{\text{Gain}}{4} \times \frac{4,194,300}{2^{42}} \tag{4}$$

To calibrate the offset, the output data should equal zero when the input is zero, $V_{REF} = REF_+ - REF_- = 5$, (fine tuning may be required to obtain zeroed offset); therefore, the offset register value is 0x00. To calibrate the gain, the output data should be equal to half the data range minus 1 for an input at the top rail; therefore, the gain register is set to 0xAAAAB4 (11,184,820 decimal).

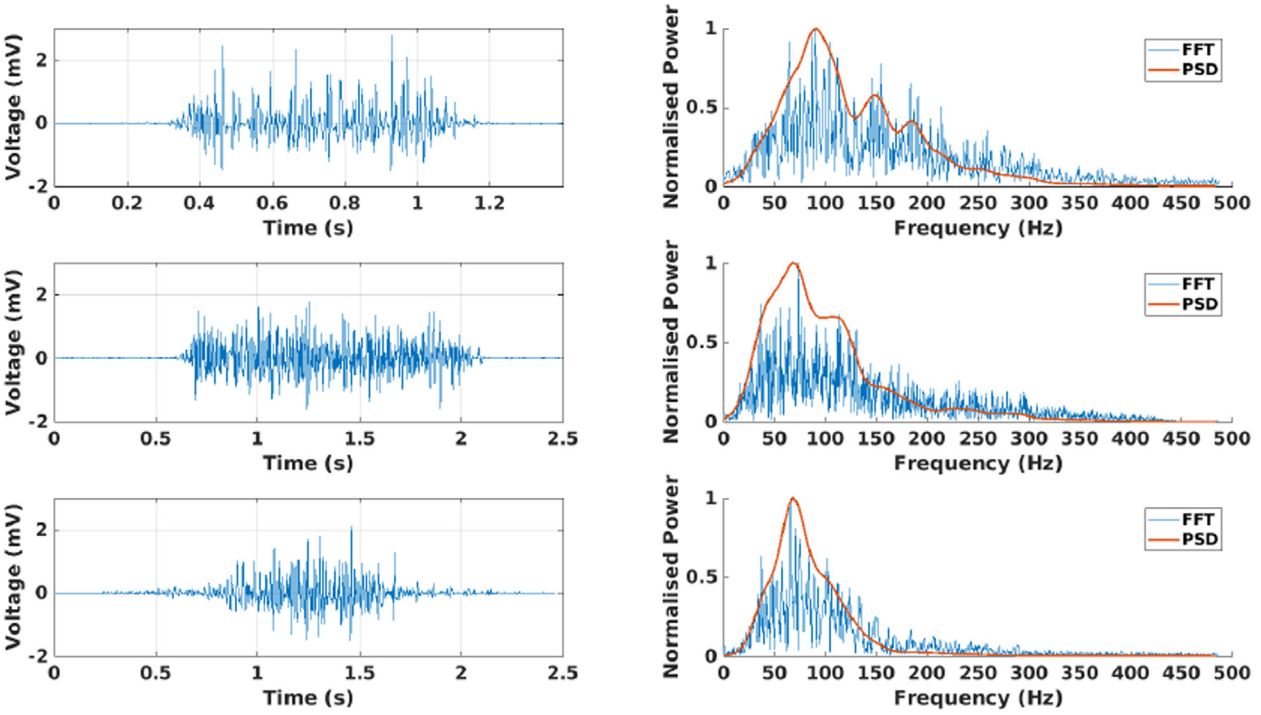

Fig. 6. Raw sEMG, normalised fast Fourier transform and power spectral density estimate for a single biceps brachii contraction from three able-body subjects.

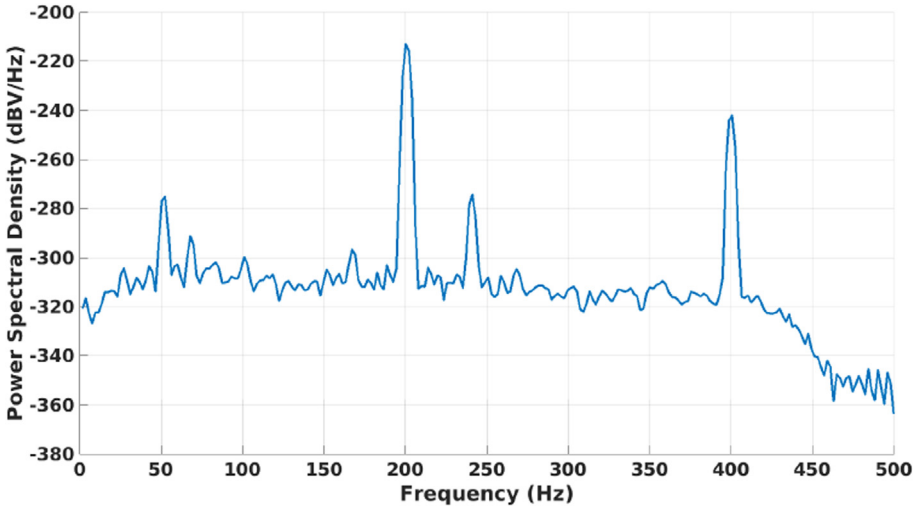

Fig. 7. Power spectral density estimate of the input referred noise using Welch's method.

Table 5
sEMG device performance parameters.

Parameter	Value	Unit
Resolution	298	nV
Bandwidth	21.2–430	Hz
Dimensions	44.5×31	mm
Gain Range	237–3400	V/V
Baseline Noise	$\leqslant 5.2, 3.4$ typical	μV_rms
Full Scale Input	1.47–21.2	pk-pk mV
ADC Resolution	24	bit
Skin preparation	Abrasive	REQUIRED
Sampling Frequency	1,000	Hz

7. Validation and characterization

Sub-maximal isometric contractions were captured from the biceps brachii for three able body subjects, Fig. 6. The data was captured using the provided example code,"EMG_ example_code.ino", then processed using MATLAB (R2017a, MathWorks) to produce the fast Fourier transform (FFT) and power spectral density (PSD) estimate using the Welch's averaged, modified periodogram method. The PSD estimate of the input referred noise, Fig. 7, was calculated by shorting the recording electrodes together and connecting the RLD driver cable to one of the electrodes. Device characteristics are based on these results, Table 5. This inexpensive open source sEMG device has a large full scale input range, low baseline noise and good interference suppression, resulting in a device that bridges the gap between high quality sEMG and affordability.

Human and animal rights

This study was approved by the Human Ethics Committee, University of Canterbury (HEC 2019/68) and informed consent was obtained from each participant prior the experiment.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgements

This research did not receive any specific grant from funding agencies in the public, commercial, or not-for-profit sectors.

Appendix A. Supplementary data

Supplementary data associated with this article can be found, in the online version, athttps://doi.org/10.1016/j.ohx.2019.e00085.

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