- **Single Chip Mixer/Oscillator and Synthesizer**
- **VHF-L, VHF-H, UHF 3-Band Local Oscillator**
- **I^{2}C Bus Protocol**
- **Bidirectional Data Transmission**
- **30-V Tuning Voltage Output**
- **4-Channel NPN Type Band Switch Drivers**
- **Programmable Reference Divider Ratio (512, 640 or 1024)**
- **5-V Power Supply**
- **32-Pin TSSOP Package**

DA PACKAGE
(TOP VIEW)

VOL OSC B	1	32	UHF RF IN2
VOL OSC C	2	31	UHF RF IN1
OSC GND	3	30	VHF RF IN2
VHS OSC B	4	29	VHF RF IN1
VHS OSC C	5	28	RF GND
UHF OSC B1	6	27	MIX OUT2
UHF OSC C1	7	26	MIX OUT1
UHF OSC C2	8	25	BS4
UHF OSC B2	9	24	BS3
IF GND	10	23	BS2
IF OUT1	11	22	BS1
IF OUT2	12	21	NC
V$_{CC}$	13	20	ADC
CP	14	19	AS
VTU	15	18	SDA
XTAL	16	17	SCL

NC – No internal connection

description

SN761672A is a single chip synthesized tuner IC designed for TV/VCR tuning systems. The circuit consists of a PLL synthesizer, 3-band local oscillators and mixer, a 30-V output tuning amplifier, and four NPN band switch drivers. It is available in a small package outline. The 15-bit programmable counter and reference divider is controlled by I^{2}C bus protocol. Tuning step frequency is selectable by this reference-divider ratio for a 4-MHz crystal oscillator.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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block diagram

Terminal Functions

| TERMINAL		I/O	DESCRIPTION
NAME	NO.		
ADC	20	I	ADC input (see Figure 7)
AS	19	I	Address selection input (see Figure 7)
BS1 BS2 BS3 BS4	22 23 24 25	O	Band switch1 output (NPN emitter follower) (see Figure 8)
CP	14	O	Charge pump output (see Figure 5)
IF GND	10		IF ground (see Figure 4)
IF OUT1	11	O	IF output (see Figure 4)
IF OUT2	12	O	IF output (see Figure 4)
MIX OUT1 MIX OUT2	26 27	O	Mixer outputs (see Figure 9)
OSC GND	3		OSC ground
RF GND	28		RF ground
SCL	17	I	Serial clock input (see Figure 7)
SDA	18	I/O	Serial data input/output (see Figure 7)
UHF OSC B1	6	I	UHF oscillator input, base 1 (see Figure 3)
UHF OSC B2	9	I	UHF oscillator input, base 2 (see Figure 3)
UHF OSC C1	7	O	UHF oscillator output, collector 1 (see Figure 3)
UHF OSC C2	8	O	UHF oscillator output, collector 2 (see Figure 3)
UHF RF IN1 UHF RF IN2	31 32	I	UHF RF inputs (see Figure 11)
V_{CC}	13		Supply voltage for mixer/oscillator/PLL: 5 V
VHF RF IN1 VHF RF IN2	29 30	I	VHF RF inputs (see Figure 10)
VHI OSC B	4	I	VHF hi oscillator input base (see Figure 2)
VHI OSC C	5	O	VHF hi oscillator output collector (see Figure 2)
VLO OSC B	1	I	VHF low oscillator input base (see Figure 1)
VLO OSC C	2	O	VHF low oscillator output collector (see Figure 1)
VTU	15	O	Tuning voltage amplifier output (see Figure 5)
XTAL	16	I	4-MHz crystal oscillator input (see Figure 6)

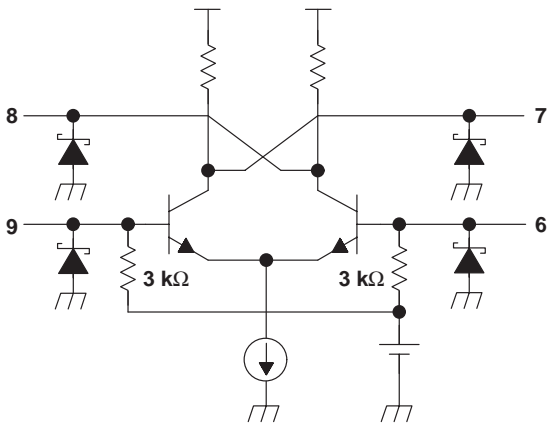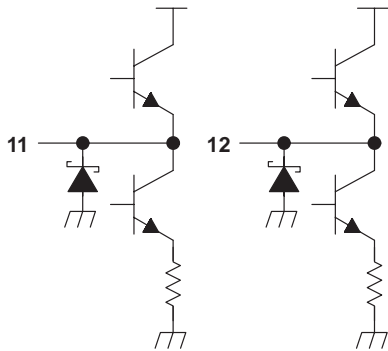## schematics
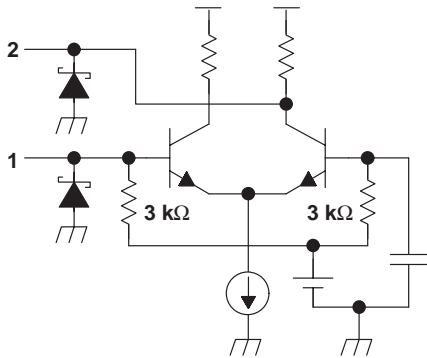
Figure 1
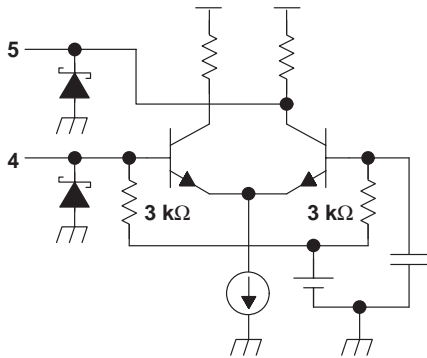
Figure 2

Figure 3

Figure 4
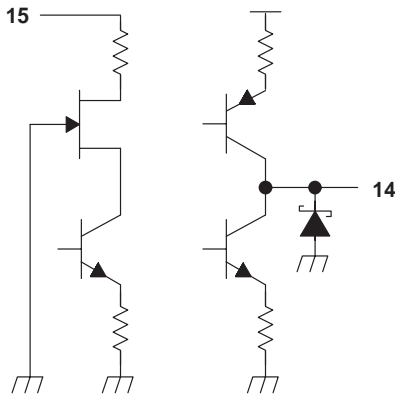
Figure 5
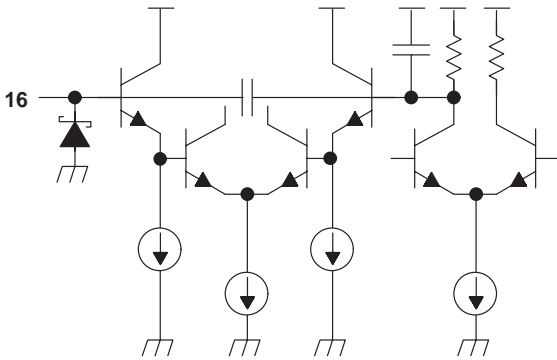
Figure 6

schematics (continued)
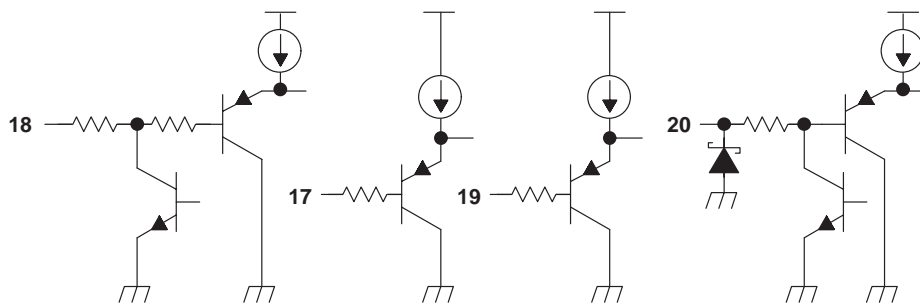
Figure 7
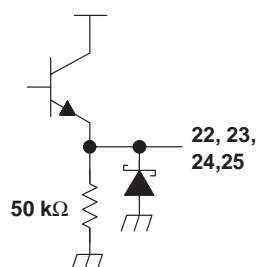
Figure 8

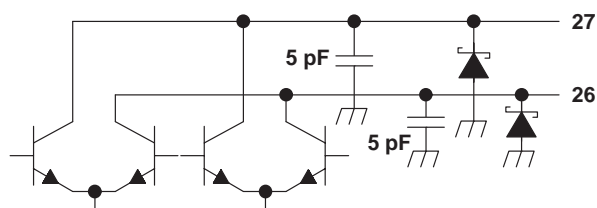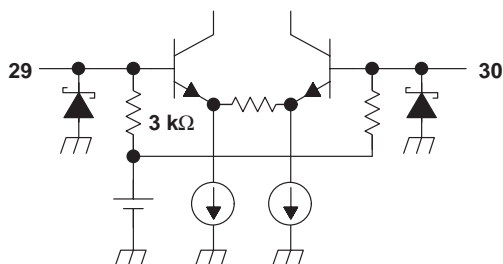**Figure 9**

Figure 10

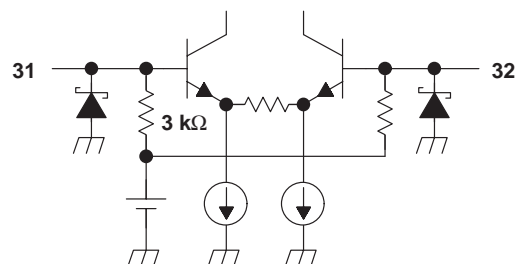**Figure 11**

SN761672A
TV/VCR TUNER IC

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . −0.4 V ~ 7 V

Input voltage 1, $V_{I(GND)}$ (see Note 1) . . . . −0.4 V ~ 0.4 V

Input voltage 2, $V_{I(VTU)}$ . . . . −0.4 V~ 35 V

Input voltage 3, $V_{(VTU)}$ (see Note 1) . . . . −0.4 V ~ 7 V

Continuous total dissipation at (or below T_A = 25°C . . . . See Dissipation Rating Table

Operating free-air temperature, T_A . . . . −20°C to 85°C

Storage temperature range, T_{stg} . . . . −65°C to 150°C

Maximum junction temperature, T_J . . . . 150°C

Maximum lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

Maximum short circuit time, $t_{(SCMAX)}$, All pins to V_{CC} . . . . TBD

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1:   Voltage values are with respect to the IF GND of the circuit.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	OPERATING FACTOR $T_A \leq 25°C$
DA	1040 mW	8.33 mW/°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Tuning supply voltage, $V_{SS(TU)}$		30	33	V
Output current of band switch, one port ON, I_O			10	mA
Operating free-air temperature, T_A	−20		85	°C

CAUTION:
It is advised that precautions to be taken to avoid damage due to high static voltages or electrostatic fields in handling this device. Pins 4–6 and 9 withstand 150 V, and all other pins withstand 200 V, according to EIAJ (0 Ω, 200 pF).

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POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

electrical characteristics

total device and serial interface (V_{CC} 4.5 V to 5.5 V, T_A = −20°C to 85°C) (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC(1)}$	Supply current 1				60	80	mA
$I_{CC(2)}$	Supply current 2		One band switch ON − $I_{(BS)}$ = 10 mA		70	90	mA
V_{IH}	High-level input voltage (SCL, SDA)			3			V
V_{IL}	Low-level input voltage (SCL, SDA)					1.5	V
I_{IH}	High-level input current (SCL, SDA)					10	µA
I_{IL}	Low-level input current (SCL, SDA)			−10			µA
$V_{(POR)}$	Power on reset supply voltage		Threshold of supply voltage between reset and operation mode	2.1	2.8	3.5	V
$V_{(ASH)}$		High	0.9 V_{CC} ~ V_{CC}	4.5		5	
$V_{(ASM)}$	Address select input voltage (AS)	Mid	0.4 V_{CC} ~ 0.6 V_{CC}	2		3	V
$V_{(ASL)}$		Low	0 V_{CC} ~ 0.1 V_{CC}			0.5	
$I_{(ASH)}$	Address select input current (AS)	High				10	µA
$I_{(ASL)}$		Low		−10			
$V_{(ADC)}$	ADC input voltage		See Table 9	0		V_{CC}	V
$I_{IL(ADH)}$	ADC high-level input current		$V_{(ADC)}$ = V_{CC}			10	µA
$I_{IL(ADL)}$	ADC low-level input current		$V_{(ADC)}$ = 0 V	−10			µA
$f_{(SCL)}$	Clock frequency (SCL)				100	400	kHz
$t_{h(HLD)}$	Data hold time		See timing chart, Figure 1	0			µs
V_{OL}	Low-level output voltage (SDA)		V_{CC} = 5 V, I_{OL} = 3 mA			0.4	V
$I_{lkg(SDA)}$	High-level output leakage current (SDA)		$V_{(SDA)}$ = 5.5 V			10	µA

PLL and band switch (V_{CC} 4.5 V to 5.5 V, T_A = −20°C to 85°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
N	Divider ratio	14-bit frequency word	256		16383	
		15-bit frequency word	256		32767	
$F_{(XTAL)}$	Crystal oscillator	R_{XTAL} = 25 Ω to 300 Ω		4		MHz
$Z_{(XTAL)}$	Crystal oscillator input impedance			1.6		k
$V_{(VTUL)}$	Tuning amplifier low-level output voltage	R_L = 27K, $V_{(TU)}$ = 33 V	0.2	0.3	0.46	V
$I_{(VTUOFF)}$	Tuning amplifier leakage current (OFF)	OS = 1, $V_{(TU)}$ = 33 V			10	µA
$I_{(CPH)}$	Charge pump high-level input current	CP = 1		280		µA
$I_{(CPL)}$	Charge pump low-level input current	CP = 0		60		µA
$V_{(CP)}$	Charge pump output voltage	In-lock		1.95		V
$I_{(CPOFF)}$	Charge pump leakage current	T2 = 0, T1 = 1, V_{CP} = 2 V, T_A = 25°C	−15		15	nA
$I_{(BS)}$	Band switch driver output current				10	mA
$V_{(SBS1)}$		$I_{(BS)}$ = 10 mA	3			
$V_{(SBS2)}$	Band switch driver output voltage	$I_{(BS)}$ = 10 mA, V_{CC} = 5 V, T_A = 25°C	3.5	3.9		V
$I_{lkg(BSOFF)}$	Band switch driver leakage current	$V_{(BS)}$ = 0 V			3	µA

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electrical characteristics (continued)

mixer, oscillator, IF amplifier (V_{CC} 5 V, T_A = 25°C, measured in reference measurement circuit at 50 W system, IF filter characteristics: f_{peak} = 43 MHz) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$G_{(c1)}$	Conversion gain (mixer ~ IF amplifier, VHF-low	f_{in} = 59 MHz (see Note 2)	20	23	26	dB
$G_{(c3)}$		f_{in} = 130 MHz	20	23	26	
$G_{(c4)}$	Conversion gain (mixer ~ IF amplifier, VHF-high	f_{in} = 136 MHz (see Note 2)	20	23	26	dB
$G_{(c6)}$		f_{in} = 364 MHz	20	23	26	
$G_{(c7)}$	Conversion gain (mixer ~ IF amplifier, VHF-UHF	f_{in} = 370 MHz (see Note 2)	22	25	28	dB
$G_{(c9)}$		f_{in} = 804 MHz	20	23	26	
NF_1	Noise figure VHF-low	f_{in} = 55.25 MHz		9.5		dB
NF_3		f_{in} = 127.25 MHz		9.5		
NF_4	Noise figure VHF-low	f_{in} = 133.25 MHz		10		dB
NF_6		f_{in} = 361.25 MHz		10		
NF_7	Noise figure UHF	f_{in} = 367.25 MHz		9		dB
NF_9		f_{in} = 801.25 MHz		10		
CM_1	1% cross modulation distortion VHF-low	f_{in} = 55.25 MHz (see Note 3)		91		dBμV
CM_3		f_{in} = 801.25 MHz		91		
CM_4	1% cross modulation distortion VHF-high	f_{in} = 133.25 MHz (see Note 3)		91		dBμV
CM_6		f_{in} = 361.25 MHz		91		
CM_7	1% cross modulation distortion UHF	f_{in} = 367.25 MHz (see Note 3)		88		dBμV
CM_9		f_{in} = 801.25 MHz		88		
$V_{(IFO1)}$	IF output voltage VHF-low	f_{in} = 55.25 MHz (see Note 4)		117		dBμV
$V_{(IFO3)}$		f_{in} = 127.25 MHz		117		
$V_{(IFO4)}$	IF output voltage VHF-high	f_{in} = 133.25 MHz (see Note 4)		117		dBμV
$V_{(IFO6)}$		f_{in} = 361.25 MHz		117		
$V_{(IFO7)}$	IF output voltage UHF	f_{in} = 367.25 MHz (see Note 4)		117		dBμV
$V_{(IFO9)}$		f_{in} = 801.25 MHz		117		
	Prescaler beat (see Note 5)				25	dBμV

NOTES: 2. IF = 43 MHz, RF input level = 80 dB μV
   3. $f_{(undes)}$ = $f_{(des)}$ ±6 MHz, pin = 80 dBμV, AM 1 kHz, 30%, DES/CM=S/I=46 dB
   4. IF = 45.75 MHz
   5. Design parameter, not tested

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POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

function description

The device can be controlled according to the I^{2}C bus format.

Table 1. Serial Interface Function

PIN	PIN NAME	FUNCTION
17	SCL	Clock input
18	SDA	Data input/output
19	AS	Address selection input
20	ADC	ADC input/test output

I^{2}C bus mode

I^{2}C write mode (R/W = 0)

Table 2. Write Data Format

	MSB							LSB	ACKNOWLEDGE
Address byte (ADV)	1	1	0	0	0	MA1	MA0	R/W 0	A
Divider byte 1 (DB1)	0	N14	N13	N12	N11	N10	N9	N8	A
Divider byte 2 (DB2)	N7	N6	N5	N4	N3	N2	N1	N0	A
Control byte (CB)	1	CP	T2	T1	T0	RSA	RSB	OS	A
Band switch byte (BB)	X	X	X	X	BS4	BS3	BS2	BS1	A

Table 3. Description of Data Symbol

SYMBOL	DESCRIPTION		DEFAULT
MA1, MA0	Address set bits (see Table 4)		
N14...N0	Programmable counter set bits	$N = N14*2^{14} + N13*2^{13} + ... + N1*2 + N0$	Nn = 0
CP	Charge pump current set bit	60 μA (CP=0) 280 μA (CP=1)	CP = 1
T2, T1, T0	Test bits (see table 5)	Normal Mode: T2=0, T1=0, To=1/0	T2=0, T1=0, T0=1
RSA, RSB	Reference divider ratio selection bits (see Table 6)		RSA=0, RSB=1
OS	Tuning amplifier control bit	Tuning voltage on (OS=0) Tuning voltage off, high impedance (OS=1)	OS=0
BS4...BS1	Band switch ports control bits BSn=0:OFF BSn=1:ON Band selection by BS1,2,4 (X = don't care) BS1 BS2 BS4 VHF-LO 1 0 0 VHF-HI X 1 0 UHF X X 1		BSn=0
X	Don't care		

Table 4. Address Selection

VOLTAGE APPLIED ON CE INPUT	MA1	MA0
0 V to 0.1 V_{CC}	0	0
Always valid	0	1
0.4 V_{CC} to 0.6 V_{CC}	1	0
0.9 V_{CC} to V_{CC}	1	1

I²C bus mode (continued)

Table 5. Test Bits (see Note 7)

T2	T1	T0	FUNCTION	
0	0	0	Normal operation	
0	0	1	Normal operation	Default
0	1	X	Charge pump off	
1	1	0	Charge pump sink	
1	1	1	Charge pump source	
1	0	0	Reference counter output is available on ADC pin.	Not available ADC
1	0	1	Main counter output is available on ADC pin (see Note 7).	Not available ADC

NOTES: 6. Not used for other bit-patterns.
7. Main counter input is bypassed 1.8 and 1.32, 1/33 prescaler from oscillator, at this mode. ($F_{OSC} \leq 4$ MHz)

Table 6. Ratio Select Bits

RSA	RSB	REFERENCE DIVIDER RATIO
X	0	640
0	1	1024
1	1	512

I²C read mode (R/W = 1)

Table 7. Read Data Format

	MSB						LSB	ACKNOWLEDGE
Address byte (ADB)	1	1	0	0	0	MA1	MA0	R/W=1	A
Status byte (SB)	POR	FL	1	1	1	A2	A1	A0	A

Table 8. Description of Data Symbol

SYMBOL	DESCRIPTION		DEFAULT
MA1, MA0	Address set bits (see Table 4)		
POR	Power-on reset flag	POR set: power on POR reset: end-of-data transmission procedure	POR = 1
FL	In-lock flag	PLL lock (FL = 1) Unlock (FL = 0)	
A2...A0	Digital data of ADC (see Table 9)		

Table 9. ADC Level

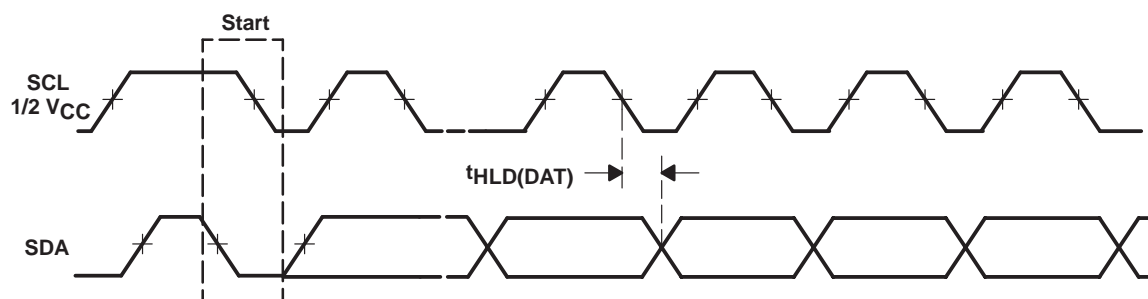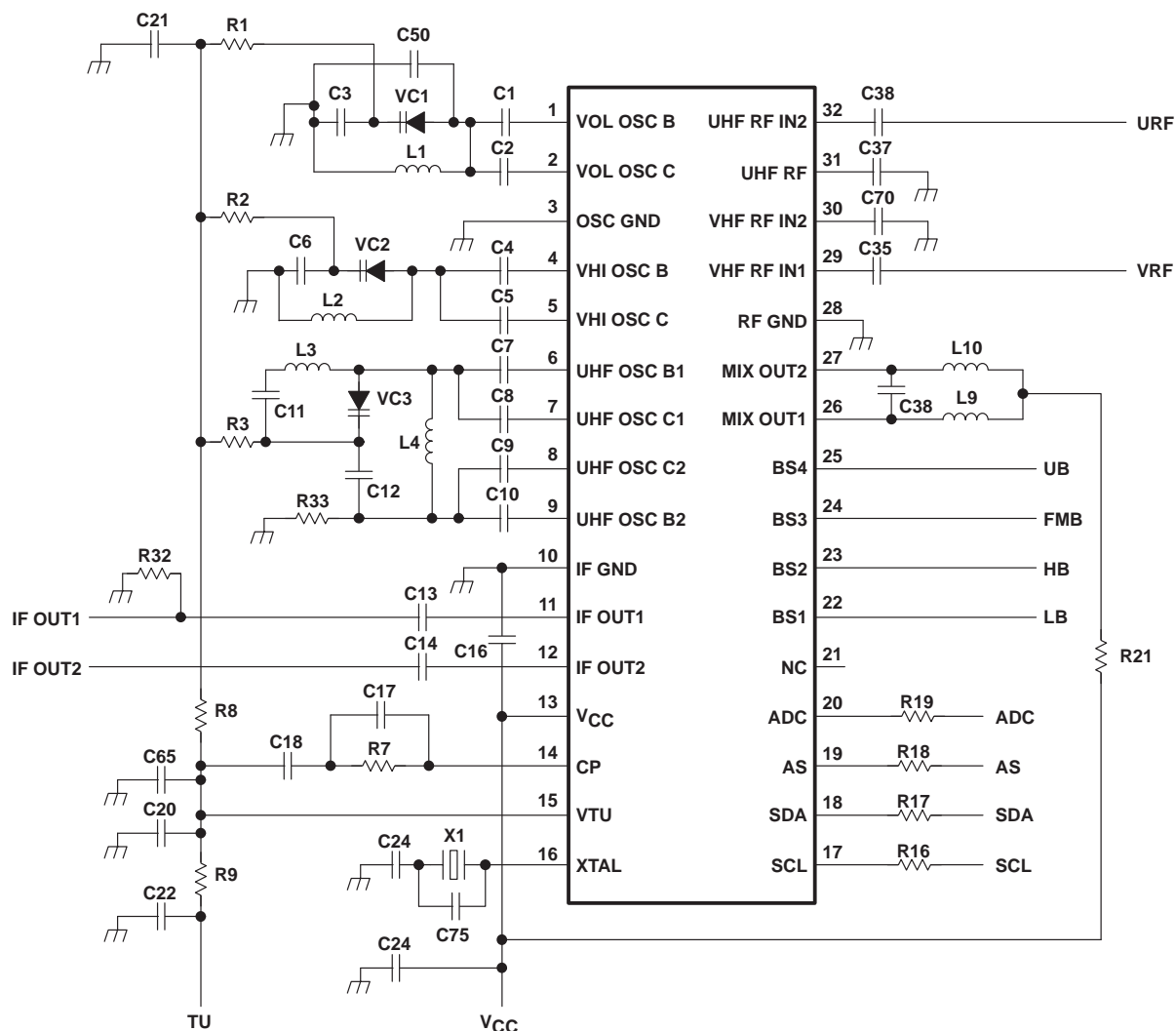| VOLTAGE APPLIED ON ADC INPUT	A2	A1	A0
0.6 V to V_{CC}	1	0	0
0.45 V_{CC} to 0.6 V_{CC}	0	1	1
0.3 V_{CC} to 0.45 V_{CC}	0	1	0
0.15 V_{CC} to 0.3 V_{CC}	0	0	1
0 V_{CC} to 0.15 V_{CC}	0	0	0

I²C read mode (R/W = 1) (continued)

Figure 12. I²C Timing Chart

APPLICATION INFORMATION

NOTE 8: This application information is advisory and performance-check is required at actual application circuits.

Figure 13. Reference Measurement Circuit

APPLICATION INFORMATION

component values for measurement circuit

PARTS NAME	VALUE	PARTS NAME	VALUE
U1	SN761672A	C1	1 pF
VC1	1T363A	C2	1 pF
VC2	1T363A	C3	47 pF
VC3	1T363A	C4	2 pF
L1	Diameter 3.0 mm 8T	C5	3 pF
L2	Diameter 2.4 mm 4T	C6	86 pF
L3	Diameter 3.0 mm 2T	C7	1.5 pF
L4	Diameter 2.0 mm 3T	C8	1.5 pF
L9	Diameter 2.4 mm 15T	C9	1.5 pF
L10	Diameter 2.4 mm 15T	C10	1.5 pF
X1	X'tal 4 MHz	C11	100 pF
R1	33 kΩ	C12	12 pF
R2	33 kΩ	C13	2.2 nF
R5	33 kΩ	C14	2.2 nF
R7	22 kΩ	C16	2.2 nF
R8	33 kΩ	C17	2.2 nF
R9	22 kΩ	C18	0.1 µF
R16	330 Ω	C20	2.2 nF
R17	330 Ω	C21	2.2 nF
R18	330 Ω	C22	2.2 nF
R21	0 Ω	C24	5 pF
R19	330 Ω	C33	27 pF
R32	56 Ω	C35	2.2 nF
R33	22 kΩ	C37	2.2 nF
		C38	2.2 nF
		C39	2.2 nF
		C50	3 pF
		C65	2.2 nF
		C70	2.2 nF
		C75	10 pF

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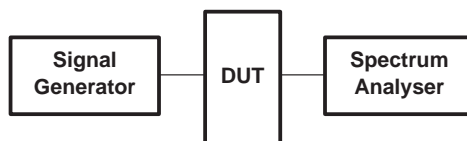## APPLICATION INFORMATION

test circuit

Figure 14. Measurement Circuit of Conversion Gain
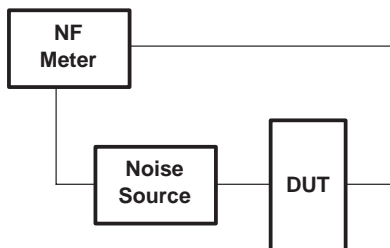
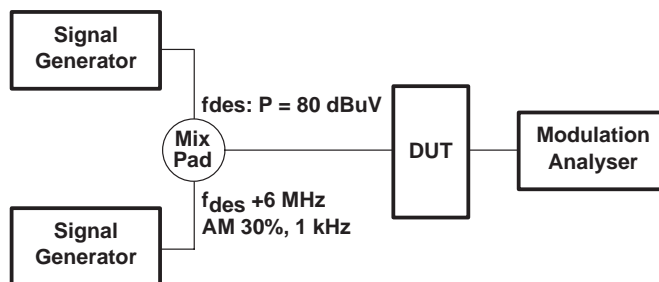**Figure 15. Noise Figure Measurement Circuit**

Figure 16. 1% Cross Modulation Distortion Measurement Circuit

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TYPICAL CHARACTERISTICS

S-parameter

VHF-Input

400MHz

50MHz

Figure 17

UHF-Input

900MHz

350MHz

Figure 18

IF-Output

60MHz

30MHz

Figure 19

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TYPICAL CHARACTERISTICS

**SUPPLY VOLTAGE
vs
BS CURRENT**
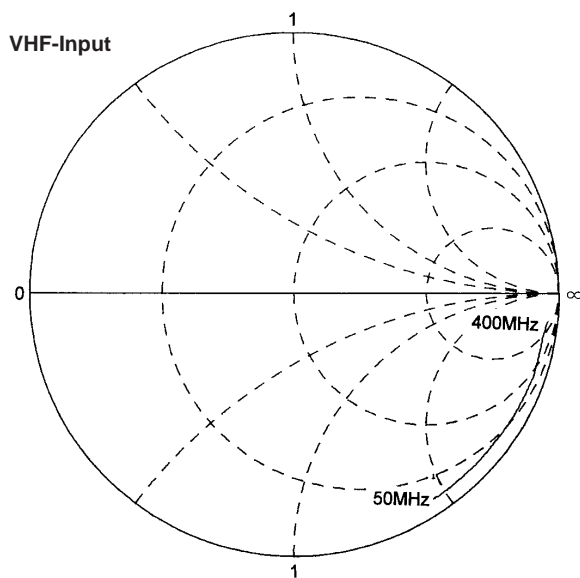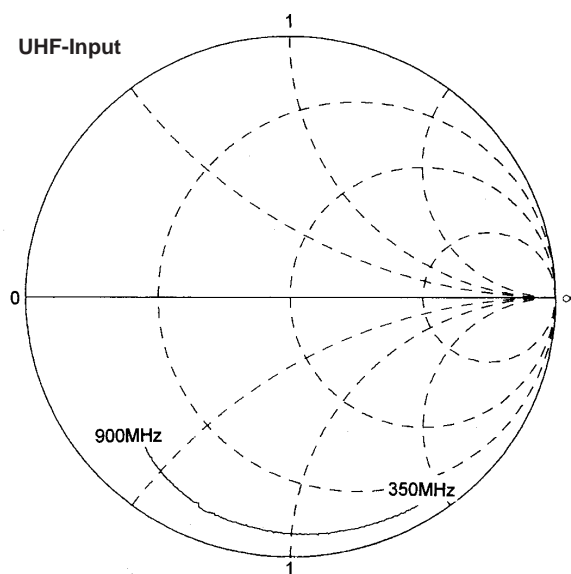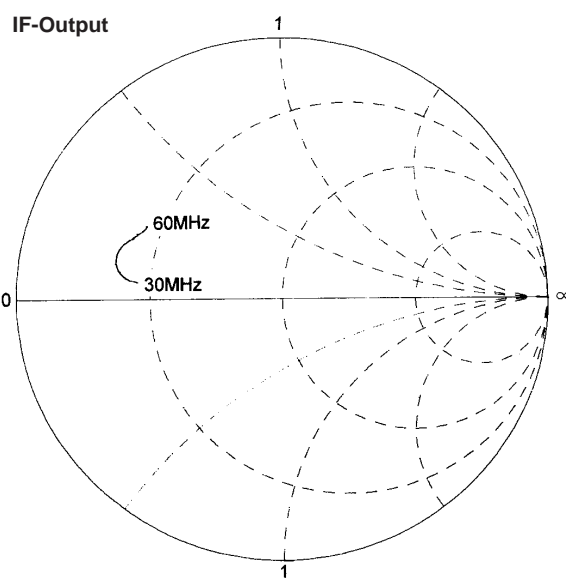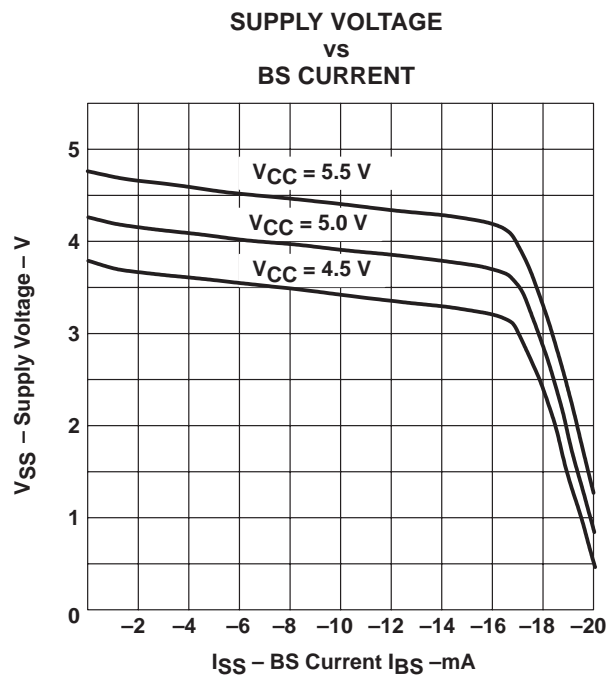
Figure 20. Band Switch Driver Output Voltage

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MECHANICAL DATA

DA (R-PDSO-G**)
PLASTIC SMALL-OUTLINE

38 PINS SHOWN

| PINS ** | 30 | 32 | 38 |
DIM			
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40

4040066 / D 11/98
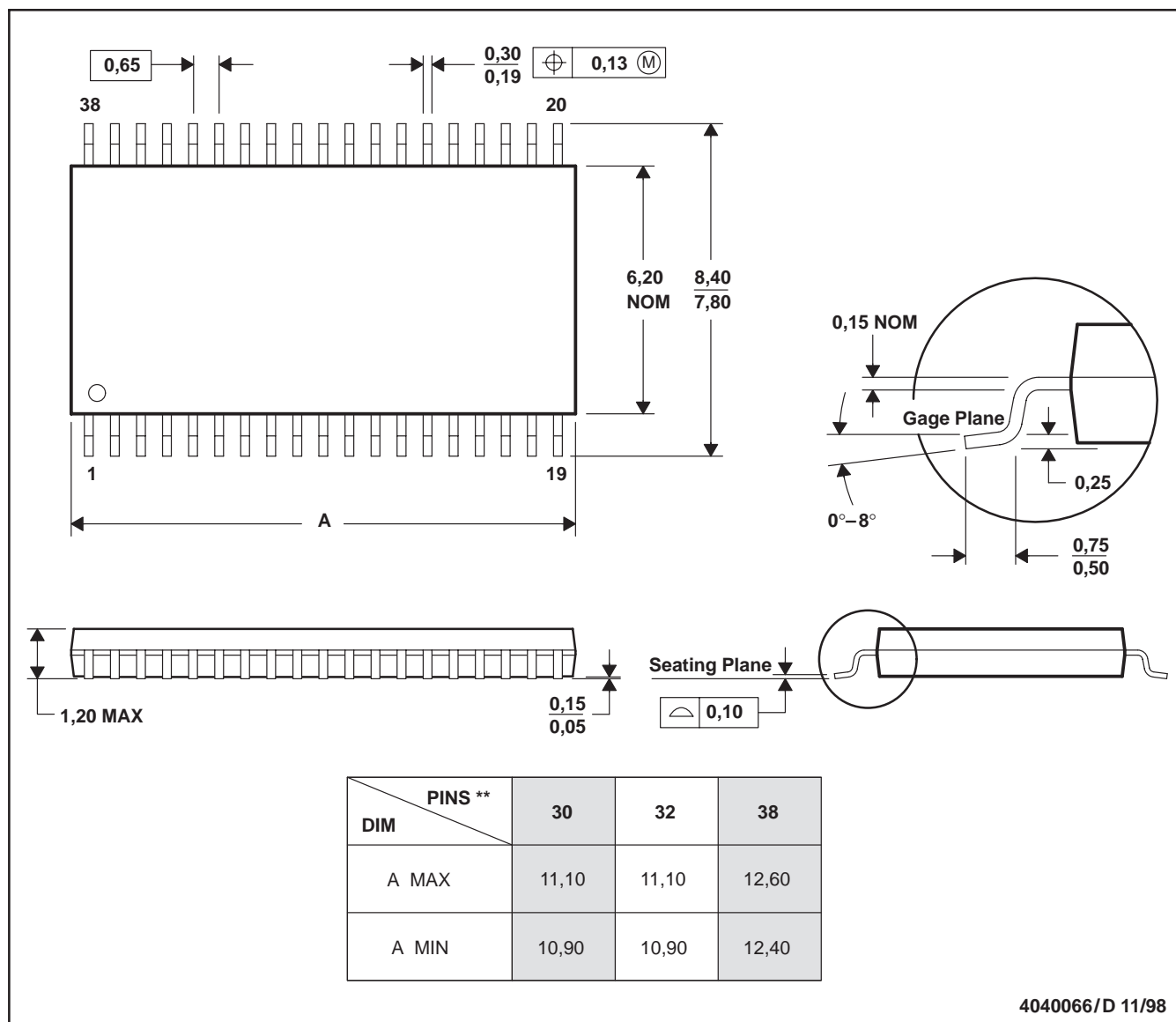
NOTES: A. All linear dimensions are in millimeters.
       B. This drawing is subject to change without notice.
       C. Body dimensions do not include mold flash or protrusion.
       D. Falls within JEDEC MO-153

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