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A low-profile three-dimensional neural probe array using a silicon lead transfer structure

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Abstract
This paper presents a microassembly method for low-profile three-dimensional probe arrays for neural prosthesis and neuroscience applications. A silicon (Si) lead transfer structure, Si interposer, is employed to form electrical connections between two orthogonal planes—the two dimensional probes and the dummy application-specific integrated circuit (ASIC) chip. In order to hold the probe array and facilitate the alignment of probes during assembly, a Si platform is designed to have through-substrate slots for the insertion of probes and cavities for holding the Si interposers. The electrical interconnections between the probes and the dummy ASIC chip are formed by solder reflow, resulting in greatly improved throughput in the proposed assembly method. Moreover, since the backbone of the probe can be embedded inside the cavity of the Si platform, the profile of the probe array above the cortical surface can be controlled within 750 μm. This low-profile allows the probe array not to touch the skull after it is implanted on the brain. The impedance of the assembled probe is also measured and discussed.

(Some figures may appear in colour only in the online journal)

1. Introduction

Millions of people worldwide are unable to move due to paralysis, a debilitating disease of the neuromuscular system identified by partial or complete loss of motor functions. A potential treatment for paralysis is to route control signals from the brain around the injury by artificial connections. The brain–machine interface system provides a communication bridge between paralytic human and the physical environment. Recent studies [1, 2] have shown that quadriplegic patients or monkeys can consciously control the activity of neurons in the motor cortex responsible for upper limb movements, even after several years of paralysis.

The neural probe is a key component of the brain–machine interface system and it is employed for the recording or stimulation of neurons in the cerebral cortex. In recent decades, wire electrodes have been used as neural probes to record the activity of neurons [3]. Although the wire electrodes can provide good recording capabilities, the wire electrodes have significant variations in their electrical characteristics as they are fabricated by hand. In order to obtain the well-defined electrode impedance characteristics and electrode size of probes, neural probes have been fabricated by microelectromechanical system (MEMS) technologies.

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Two-dimensional (2D) probes are frequently fabricated by MEMS technologies [4, 5]. However, the recording zone is restricted due to the limited brain region covered by 2D probes. High recording density and three-dimensional (3D) implant region of the 3D probe arrays are more desirable for neural prosthesis and neuroscience applications [6–12].

One of main challenges is to develop a low-profile probe array which does not touch the skull when it floats along with the brain to minimize trauma of brain cells after implantation. The Utah electrode array is fabricated by directly bulk-micromachining the silicon (Si) wafer, and this unique fabrication process makes it easy to implement a low-profile neural probe array microsystem [6, 7]. Since the connection pads of the fabricated electrode array are placed in the same plane as the pads in the application-specific integrated circuit (ASIC) chip containing complementary metal-oxide-semiconductor (CMOS) electronics for neural recording, the integration is straightforward. The electrode array and the ASIC are simply flip-chip bonded by using AuSn reflow soldering, which results in a slim profile of the electrode array microsystem, as thin as 750 μm [7]. However, the chosen fabrication method also poses significant limitations. Since the probe length is determined by the thickness of the wafer used in the fabrication, the maximum probe length is limited to a few millimeters. In addition, each neural probe can carry only one recording electrode located at its tip.

The Michigan electrode array is free from these disadvantages due to differences in fabrication process. Unlike the Utah process, 2D neural probes are fabricated first using planar surface-micromachining, and then the 2D probes are assembled using a Si-based platform to form a 3D probe array [8]. The probe length is easy to define, and multiple electrodes can be formed at any location(s) along the probe shank. However, the Michigan probe array microsystem does not have its recording circuits in a separate ASIC, but in the probe backbone. Thus the profile of the probe array microsystem is high and the device can touch the skull and cause tissue injuries when it moves due to brain micromotion. In order to mitigate this issue, the probe backbone containing CMOS circuitry can be bent horizontally with respect to the Si platform [9]. However, the achievable profile is still limited. Moreover, the fabrication process for modern CMOS integrated circuits is much more sophisticated and expensive than the process for probe micromachining. Implementing the probe and the CMOS electronics using the same fabrication process leads to either unnecessary cost overhead or non-optimal electronics in terms of its performance, size and power consumption.

In order to avoid fabricating the CMOS electronics on the backbone of probes, while maintaining the advantages of surface-micromachined probes, several groups have fabricated the 2D planar probes and the ASIC separately and assembled them later by using the lead transfer technique [10–13]. In the assembly process, the main challenge is making connections between probe pads and ASIC pads that are placed orthogonal to each other, and this bonding plane mismatch is resolved by the lead transfer technique. In [10], an individual 2D probe is bonded with ribbon cable directly, and then two assembled probe/cable pairs are bonded rear-to-rear to form a 3D probe array. The cables are connected to the ASIC later on. Aarts *et al* [11] proposed to use overhanging gold clips which are bent and squeezed between the cavity wall of the Si platform and the side wall of the probe. However, the backbone thickness of probes must be precisely controlled to have a perfect fit between the carrier and the probes during assembly process. The backbone thickness of probes is difficult to be precisely controlled by deep reactive ion etching (DRIE) and the lapping process. Therefore, Aarts *et al* [12] proposed a compressible biocompatible interconnect using a thin film transfer process to get an elastic behavior of the interconnect.

This paper presents a microassembly method of a low-profile probe array for chronic implantation. 2D multi-electrode probes [14] are fabricated and assembled into the slim Si platform [15, 16] to implement a 3D probe array. As a Si lead transfer structure, a Si interposer is introduced to overcome the bonding plane mismatch between the probe array and the ASIC. The fabrication process details of the probe, Si platform and Si interposer are provided in this paper. The proposed assembly method allows the ASIC to be directly bonded onto the probe array by reflow soldering. Therefore, the final size of the integrated probe array microsystem can be minimized. The complete assembly and packaging processes of 3D probe array are also presented. Finally, the impedance of the assembled probe and the interconnect reliability are measured and discussed.

2. Design and concept

2.1. Implantable probe array

Figure 1(*a*) shows the schematic of a 3D probe array implanted into a human brain. The probe array is implanted in a narrow space (subarachnoid space) between the pia mater and dura mater. In general, the subarachnoid space of the human brain is around 1–2.5 mm [17, 18]. Therefore, the probe array with a profile that is too high will touch the skull and damage the tissue when relative micromotion occurs between the brain tissue and the probes. To avoid this issue, the probe array profile should be kept as thin as possible to ensure that the probe array freely floats along with the brain after implantation on the cortex. Figure 1(*b*) shows the expanded view of the proposed low-profile probe array which consists of a probe array, a Si platform, and a neural recording ASIC. In this work, a dummy ASIC is used to simulate the interconnection between a real ASIC and a probe array. The dummy ASIC can be electrically connected to the probe through a Si interposer, which is used as a lead transfer structure in our design. The thicknesses of the Si platform and the dummy ASIC are 450 μm and 300 μm, respectively. Therefore, the whole thickness of the assembled probe array can be controlled within 750 μm, which guarantees that the probe array does not touch the skull.

2.2. Lead transfer technique

Lead transfer is critical when implementing a 3D probe array using 2D probes. Since the dummy ASIC pads are located in plane and the probe pads are in out of plane, it is difficult to form electrical connections between these

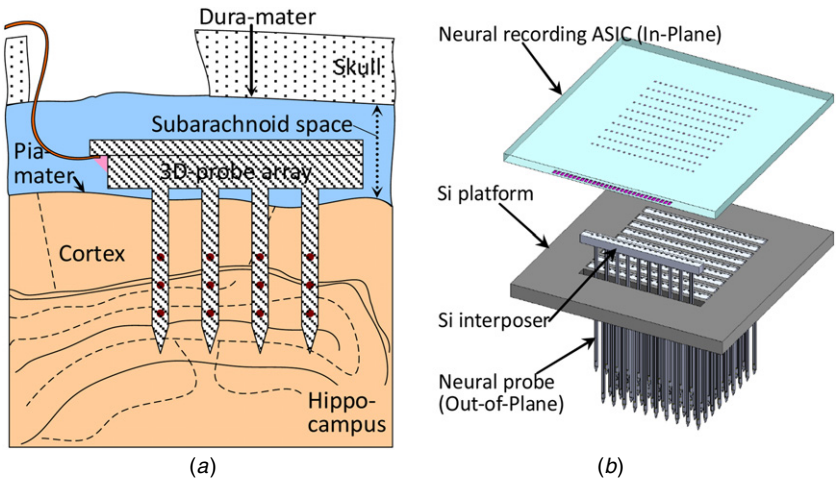

Figure 1. (*a*) Schematic of the probe array implanted into human brain. This figure is not to scale. (*c*) Exploded schematic of the proposed low-profile probe array.

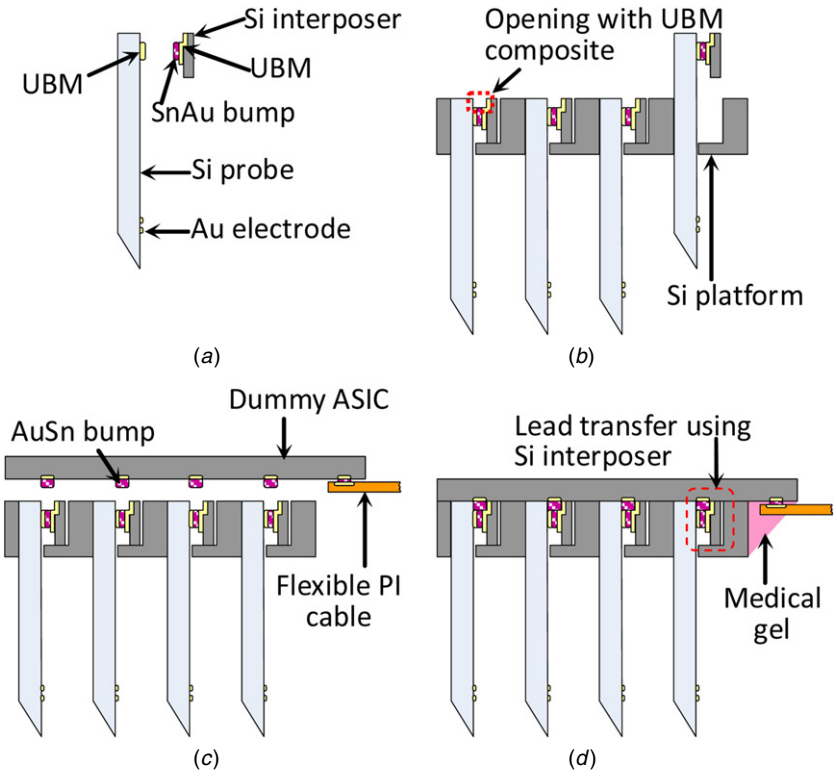

Figure 2. Schematics of the proposed lead transfer process for implementing a 3D probe array. (*a*) Probe and Si interposer. (*b*) Probe inserted into the Si platform. (*c*) Dummy ASIC with AuSn bumps. (*d*) Reflow soldering process.

perpendicular conductors, as shown in figure 1(*b*). The concept of lead transfer is described in figure 2. Firstly, the 2D multi-electrode probes and the Si interposers are realized by MEMS technologies, as shown in figure 2(*a*). The Si interposer with AuSn bumps is employed to connect out-of-plane probe pads and in-plane dummy ASIC pads. The under-bump metallization (UBM, Ti/Pt/Au) pads of the probe are designed for flip-chip bonding with the Si interposer. In figure 2(*b*), the Si interposer is bonded with the probe, and then the openings with the UBM composite are formed at the probe backbone for electrical connection with the dummy ASIC pads. The probes are precisely aligned and inserted into the through-substrate slots in the Si platform. In figure 2(*c*), the flexible polyimide (PI) cable is bonded on the dummy ASIC first. Then, the dummy ASIC with the PI cable is bonded on the Si platform. In order to make connections with the openings of the probes assembled with the Si interposers, the AuSn bumps are formed on top of the dummy ASIC pads. The AuSn flip-chip bonding techniques are used [19, 20], since they require lower mechanical force during assembly which minimizes stress on the probe array. Finally, as shown in figure 2(*d*), after solder reflow, the AuSn bumps on the dummy ASIC pads are soldered with the UBM composites in the openings, completing the formation of electrical connections using the

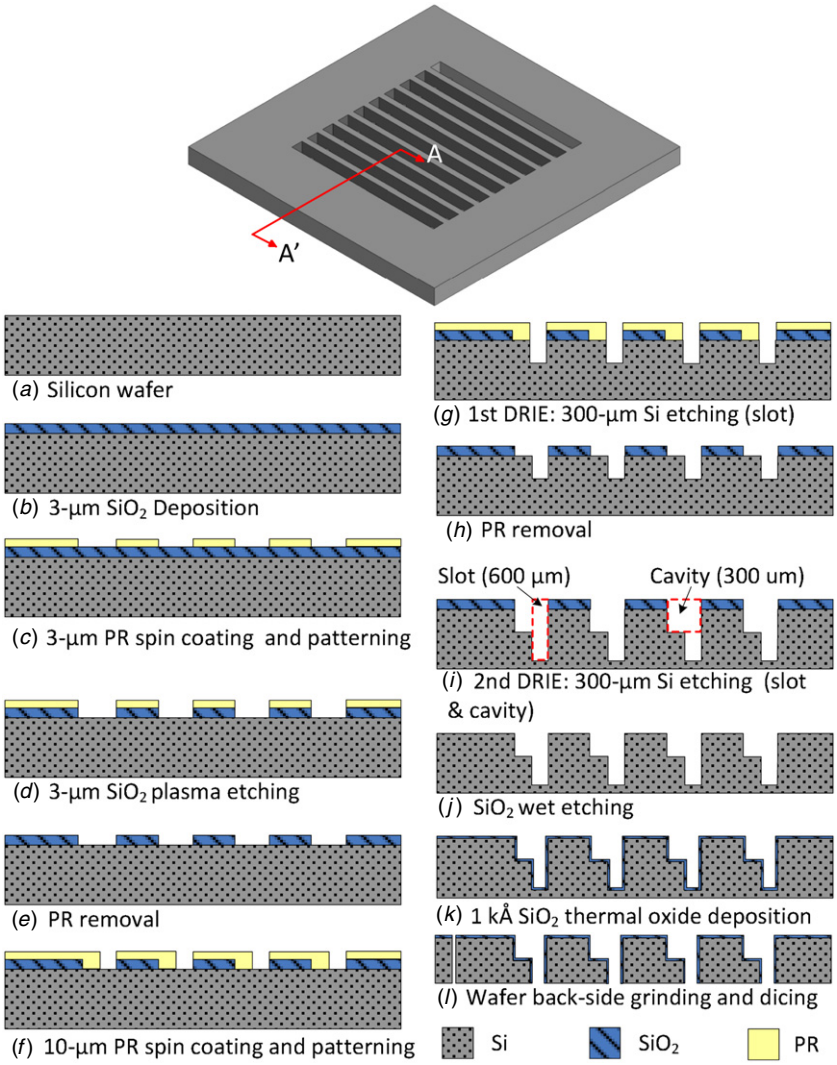

Figure 3. Fabrication process of the Si platform. The cross section AA' is shown in different stages of the process.

Si lead transfer structure. The medical epoxy is applied to enhance the bonding strength of the PI cable, dummy ASIC and Si platform, as shown in figure 2(*d*). In the proposed design, the flexible PI cable is only attached with the dummy ASIC and not sandwiched between the dummy ASIC and Si platform, so that the profile of the probe array is not increased due to the integration of the flexible PI cable.

For the Michigan probe array [8, 9], in order to hold Michigan probes orthogonal to the platform and support the CMOS circuitry fabricated on the backbone of probes, micromachined spacers have to be implemented during assembly. In 2011, a folded Michigan probe array was developed using planar fabrication and platform-gate latch structure to prevent the implant from contacting with the skull [21]. On the contrary, the backbone of neural probe is totally inserted into the slot of Si platform in our design. Therefore, the probes can be held by Si platform without additional spacers and the profile of the probe array can be strictly minimized. The profile of the 3D probe array assembled with the recording dummy ASIC can be kept within 750 μm above the cortical surface after implantation, as in the Utah probe array [6, 7]. Also, the unrestricted freedom in 2D probe layout and the multiple electrodes per shaft are available, as in the Michigan probe array.

3. Fabrication and assembly

3.1. Si platform

In the proposed design, the Si platform is employed to align and support the array of 2D probes during the assembly process. Figure 3 shows the fabrication process of the Si platform, which is mainly based on DRIE of Si. Firstly, a 3 μm SiO_2 layer is deposited on a Si wafer by using plasma-enhanced chemical vapor deposition (PECVD), as shown in figures 3(*a*) and (*b*). Then, a 3 μm photoresist (PR), PFI-26A from Sumitomo Chemical Co., Ltd, Japan is coated and patterned on the wafer (figure 3(*c*)). Then, the SiO_2 layer is patterned by reactive ion etching (RIE) process using Advanced Vacuum RIE Vision 300 MK II Versatile Plasma System, Sweden (figure 3(*d*)). A RIE recipe optimized for SiO_2 etching with a platen power of 300 W; a process pressure of 100 mTorr; and gas flows of 45 sccm and 5 sccm for fluoroform (CHF_3) and oxygen (O_2), respectively,

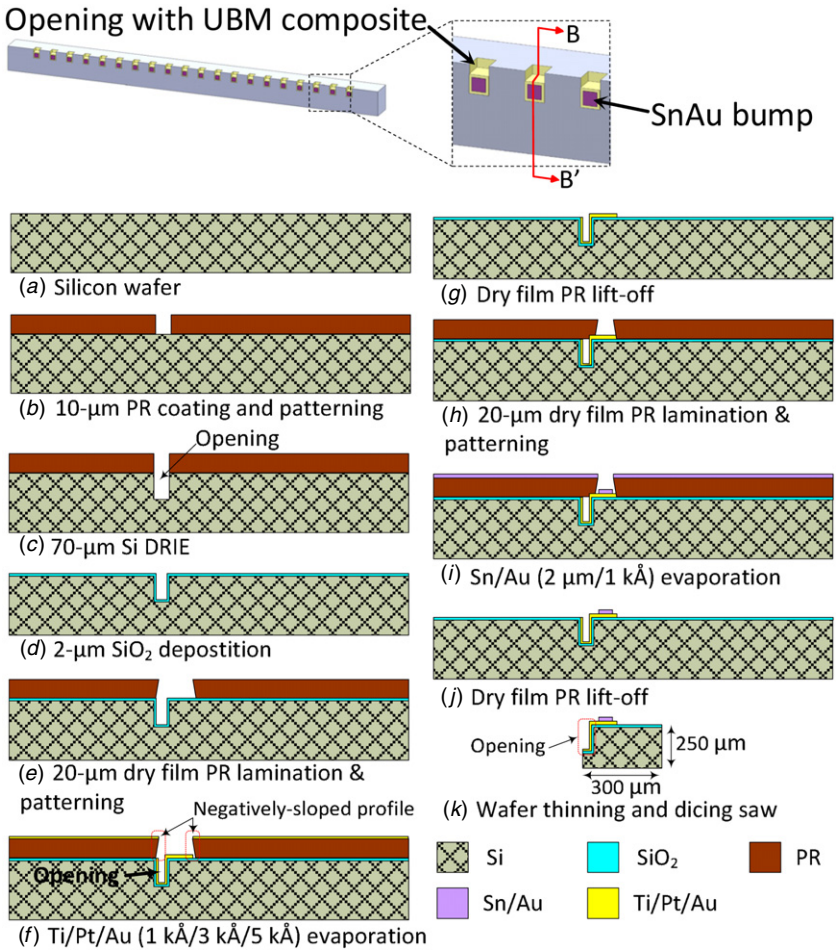

Figure 4. Fabrication process of the Si interposer. The cross section BB′ is shown in different stages of the process.

is applied. The dry etching rate of SiO_2 is 330 Å min^{-1}. After plasma etching of SiO_2 (figure 3(*d*)) and PR removal using PRS3000 PR stripper from Avantor Performance Materials, US (figure 3(*e*)), the patterned SiO_2 layer serves as an etch mask later for the second DRIE step to define the cavity shape of the Si platform. Next, in order to perform 300 μm DRIE process effectively, a 10 μm thick PR layer AZ5214 is coated and patterned (figure 3(*f*)) to be an etch mask for the following first DRIE step. The slot depth and the cavity geometry defined from the DRIE step using STS ICP multiplex etcher from the Surface Technology Systems, UK. A DRIE recipe optimized for Si etching with a coil power of 600 W; and gas flows of 130 sccm, 13 sccm and 110 sccm for sulfur hexafluoride (SF_6), oxygen (O_2) and octofluorocyclobutane (C_4F_8), respectively, is applied. The dry etching rate of Si is about 2.08 μm min^{-1}. By the first DRIE process, slots with a depth of 300 μm are defined (figure 3(*g*)). After that, the PR was stripped by PRS-3000 PR stripper (figure 3(*h*)) and the SiO_2 etch mask is exposed for the following second DRIE step. The slots and cavities are formed by the second DRIE process, as illustrated in figure 3(*i*). The SiO_2 mask layer is removed by buffered oxide etch solution (NH_4F: HF = 6: 1) (figure 3(*j*)). Then, a 1 kÅ SiO_2 layer is formed by thermal oxide deposition and serves as an insulating layer (figure 3(*k*)). After that, the wafer is thinned to 450 μm using back-side grinding machine [14], DGP8761HC from DISCO Corporation, Japan and then the through-substrate slots are exposed to the back-side of the wafer (figure 3(*l*)). Finally, the Si platform is obtained after dicing process using dicing machine DFD 6361 from DISCO Corporation, Japan.

3.2. Si interposer

The Si interposer is a key component for lead transfer when implementing the 3D probe array. Figure 4 shows the fabrication process of Si interposer. As shown in figures 4(*a*) and (*b*), a 10 μm PR layer as an etch mask is coated and patterned on a Si wafer. Next, the opening of Si interposer is formed by DRIE process with the etch depth of 70 μm (figure 4(*c*)). After that, the PR is removed by PR stripper, and then a 2 μm SiO_2 layer as an insulating layer is deposited on the Si wafer by PECVD (figure 4(*d*)). In order to avoid PR filling in the deep opening, 20 μm negative dry film PR (MX-5020, DuPont Electronic Technologies [21]) is laminated and patterned with 30 μm feature size on the Si wafer (figure 4(*e*)). After that, the UBM composite layers are deposited by evaporation process (figure 4(*f*)) and the dry film PR (figure 4(*g*)) is lifted off. The PR stripper solvent, Atotech Resiststrip RR-3, is used to dissolve the PR. To guarantee

the successful UBM lift-off process, the PR side wall should have a negatively-sloped profile [23], as shown in figure 4(*f*). The negatively-sloped PR side wall ensures that the UBM film deposition is not continuous, allowing the stripper solvent to dissolve the PR. The PR should be at least twice thicker than the deposited UBM layers for more effective lift-off process. The UBM consists of evaporated Ti, Pt and Au thin films in thicknesses of 1 kÅ, 3 kÅ and 5 kÅ, respectively. The dimensions of UBM pad are 70 μm $\times$ 70 μm. The Ti layer is used as an adhesion layer while the Pt layer is a diffusion barrier. The Au layer is a wettable metallization compatible with the soldering process. In order to realize reliable flip-chip bonding, the UBM is required to provide good adhesion with bonding structure [7]. After the UBM deposition, 20 μm dry film PR was laminated and patterned to fabricate AuSn solder bumps (figure 4(*h*)). The Sn and Au thin films in thicknesses of 2.0 and 0.1 μm are deposited on the UBM pad (figure 4(*i*)) and then the PR is lifted off (figure 4(*j*)). After the wafer is thinned to 250 μm, the wafer is diced and the Si interposer is obtained (figure 4(*j*)). The dimensions of the Si interposer are 4.50 mm $\times$ 0.30 mm $\times$ 0.25 mm. The UBM thin films are deposited in the opening, which are used for solder bonding with the dummy ASIC.

3.3. Neural probe

2D neural probes are fabricated and microassembled to implement a 3D probe array. Figure 5 shows the fabrication process of the 2D probe. Each 2D probe is composed of ten shafts and the tip of each shaft has two recording electrodes in this design. Similar to the Si interposer design, the UBM pads are patterned at the backbone of probes to achieve reliable flip-chip bonding with the Si interposer later. Firstly, a 4 kÅ SiO_2 layer is deposited as an insulating layer on a Si wafer by PECVD (figures 5(*a*) and (*b*)). Ti and Au thin films in thicknesses of 1 kÅ and 1 μm are deposited on the wafer by evaporation (figure 5(*c*)). The electrode, traces, and bonding pads are defined by Ti/Au wet etching (figures 5(*d*) and (*e*)). The Au and Ti films are removed by gold etchant (HNO_3 : HCl : H_2O = 1 : 3 : 4) and titanium etchant (NH_4OH : H_2O_2 : H_2O = 1:1:3), respectively. As shown in figure 5(*f*), a 2 μm SiO_2 layer as an insulating layer is deposited on the wafer using PECVD. Next, a 2 μm PR layer is coated and patterned to define the electrodes and bonding pads of the probe. Then, the deposited SiO_2 on the electrodes and bonding pads is removed by plasma etching process, and the PR is removed by PR stripper. After that, the UBM thin films are evaporated on the bonding pads of the probe (figures 5(*g*)–(*j*)). The evaporated film thicknesses of the UBM composite are indicated in figure 5(*i*). Then, a 10 μm PR layer used as an etch mask for SiO_2 etching is coated and patterned to define the shape of the neural probe (figure 5(*k*)). SiO_2 is removed using plasma etching, and then Si is etched 80 μm in depth by DRIE, as shown in figures 5(*l*) and (*m*), respectively. Next, the ultraviolet (UV) tape is attached to the front side of the wafer for back-side grinding after PR removal (figures 5(*n*) and (*o*)). By back-side grinding, the wafer is thinned down to 70 μm in thickness. Finally, the thinned wafer is exposed to UV light and the probes are released (figure 5(*p*)).

3.4. Assembly process

The assembly process of the low-profile probe array is illustrated in figure 6. Firstly, the 2D neural probes and Si interposers are fabricated using micromachining technologies, as shown in figures 6(*a*) and (*b*), respectively. The assembly pins formed in the 2D probes (figure 6(*a*)) are used later to fit into the fixing slots in the Si platform to hold the pieces of the 3D structure together for convenience in the following assembly process steps. The UBM bonding pads at the probe backbone and the AuSn bumps of the Si interposer are used for the flip-chip bonding process. As shown in figure 6(*c*), the Si interposer is bonded onto the probe backbone by the SET FC150 flip-chip bonder from Smart Equipment Technology, France with applying a 150 g compression force and heating at 260 °C for 3 min. The openings with UBM composite are formed after flip-chip bonding of the probe and the Si interposer. The dimensions of the openings with UBM composite are 70 μm $\times$ 70 μm $\times$ 40 μm. Then, the probe assembled with the Si interposer is inserted into the slot of the Si platform (figure 6(*d*)) with the assistance of a 3-axis micromanipulator. The Si platform with the 2D probes slotted in is supported by an assembly jig, as shown in figure 8(*c*).

During the probe insertion process, the cavity of Si platform provides room to hold the Si interposer. The backbone of the probe bonded with the Si interposer is embedded into the Si platform. Consequently, the slim backbone of the 3D probe array can be obtained, as shown in figure 6(*e*). In order to bond with the UBM composites in the openings of the probe, AuSn solder bumps are fabricated on the bottom surface of the dummy recording ASIC(DRA), as shown in figure 6(*f*). The dimensions of the AuSn solder bump are 60 μm $\times$ 60 μm $\times$ 50 μm. As shown in figure 6(*g*), the micro-fabricated flexible PI cable [24] is used to exchange the recorded neural signal and the power supply voltages between two ASIC chips. The thickness and length of the PI cable are 10 μm and 20 mm, respectively. The flexible PI cable is flip-chip bonded onto the DRA with applying a 300 g compression force and heating at 280 °C for 2 min (figure 6(*h*)). Then, the AuSn solder bumps of the DRA are aligned with the openings in the probe by the flip-chip bonder with applying a 100 g compression force and heating at 260 °C for 1 min. To prevent electrical shorts between bonding pads, a solvent-free liquid underfill encapsulant (UFR115VL, Nagase ChemteX Corp.) is applied on the dummy ASIC before flip-chip bonding (figure 6(*i*)). Then, the electrical connections are formed between the DRA and the probe. After that, a 184 silicone elastomer (Dow Corning Corp.) is applied between the DRA, PI cable and Si platform to increase the bonding strength, as shown in EE' section of figure 6(*i*). In addition, the side-walls of the DRA, Si interposer and Si platform are insulated from physiological medium by this silicone elastomer. The DRA with the PI cable is firmly secured on the Si platform after thermal curing at 100 °C for 35 min. Finally, the dummy wireless ASIC (DWA) is bonded onto the PI cable with applying a 300 g compression force and heating at 280 °C for 2 min (figure 6(*j*)).

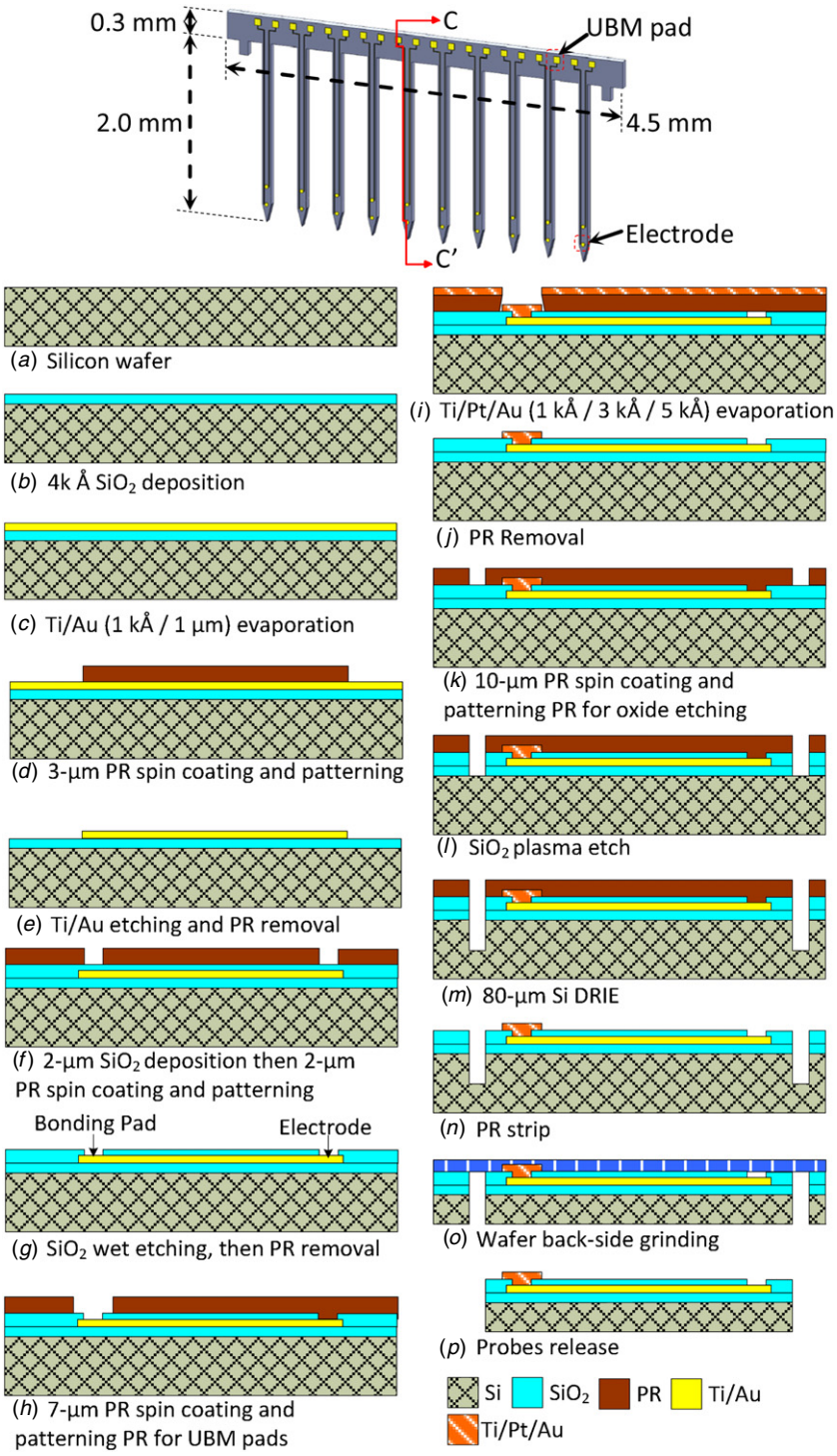

Figure 5. Fabrication process of the neural probe. The cross section CC′ is shown in different stages of the process.

4. Results and discussions

4.1. Fabricated device

The fabrication and assembly of the low-profile neural probe array has been successfully demonstrated. The performance of the probe array has also been characterized. Figure 7 shows the fabrication results. The fabricated 2D probe with ten shafts is shown in figure 7(*a*). The thickness, width and length of each shaft are 70 μm, 100 μm and 2 mm, respectively. Two assembly pins at the probe backbone for easier assembly are also indicated in the figure. As shown in the top photo of figure 7(*b*), the UBM pads are formed at the probe backbone and used for flip-chip bonding with the Si interposer. The magnified view of a shaft tip is shown in the bottom photo of figure 7(*b*). Each shaft has two electrodes with a diameter of 20 μm for neural signal recording. Each recording electrode is electrical connected with an UBM pad at the backbone of the

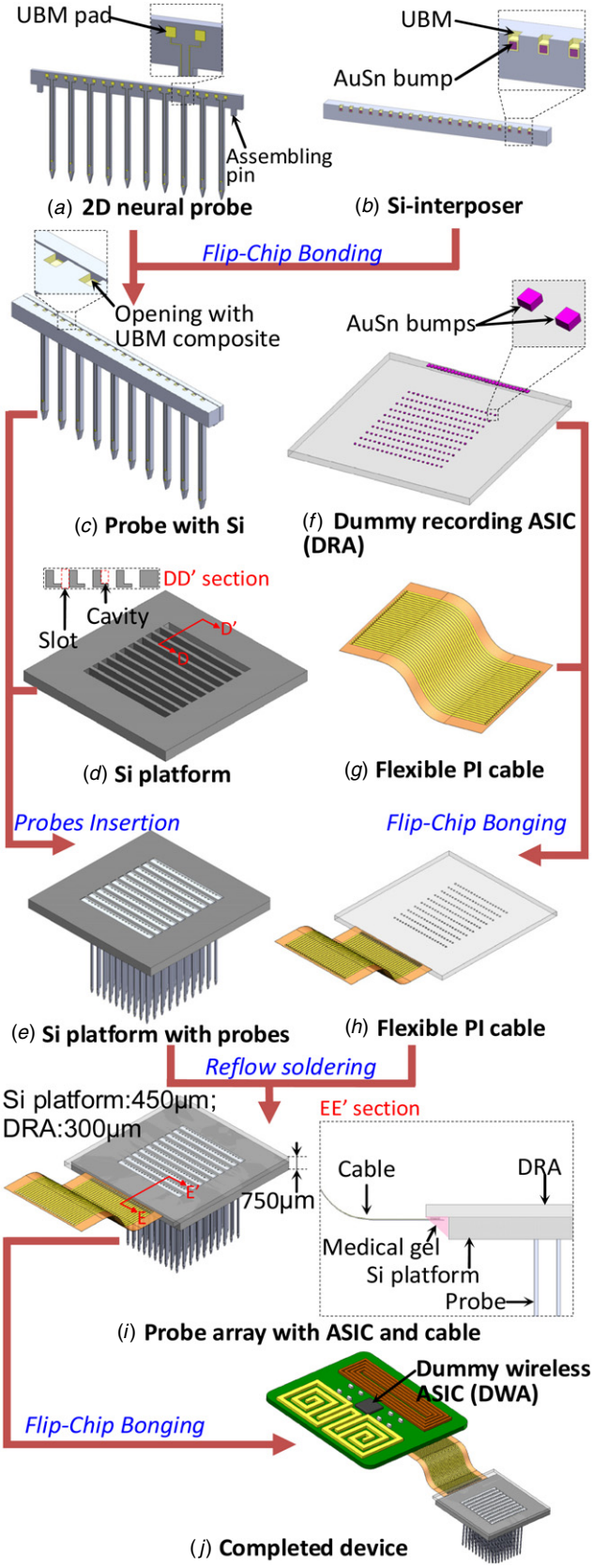

Figure 6. Assembly process of the low-profile probe array.

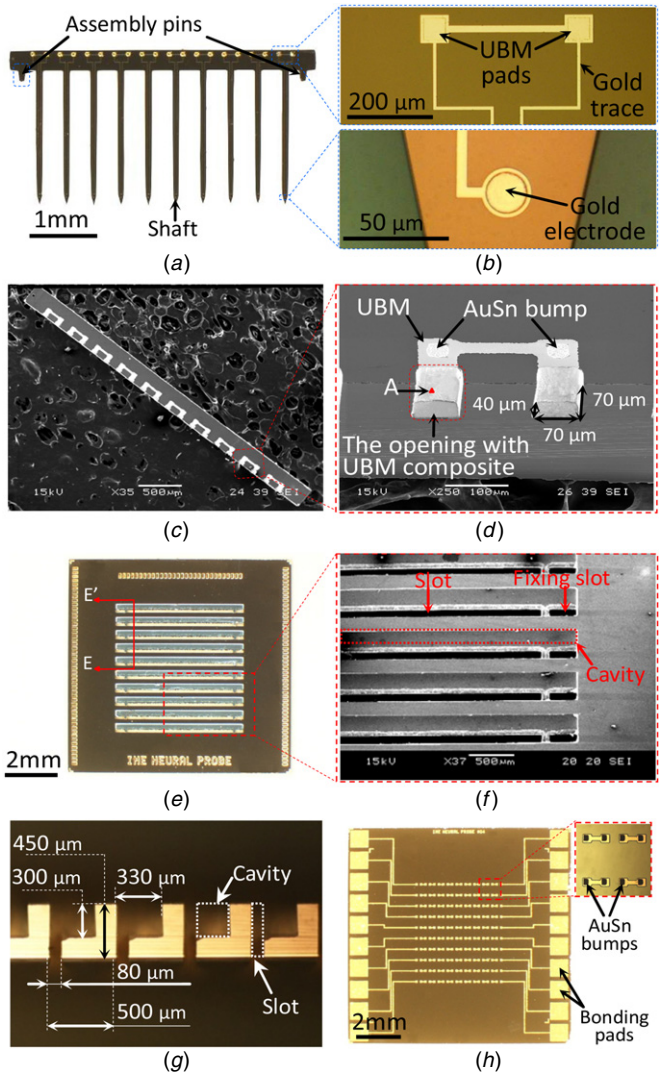

Figure 7. Fabrication results. (*a*) 2D neural probe with ten shafts. (*b*) Magnified views of the probe: the probe backbone (top photo) and the probe tip (bottom photo). (*c*) Si interposer. (*d*) UBM in the opening of the Si interposer. (*e*) Si platform. (*f*) Slot and cavity of the Si platform. (*g*) Cross section EE' of the Si platform shown in 7(*e*). (*h*) Dummy ASIC.

probe. In order to facilitate the electrical characterization after assembly, each pair of UBM pads are electrically connected together. In figure 7(*c*), the fabricated Si interposer as the lead transfer structure is shown. The magnified view of the Si interposer is shown in figure 7(*d*). The UBM layer is obviously deposited in the opening of the Si interposer. Therefore, the UBM in the opening can provide an electrical connection interface between the neural probe and the recording dummy ASIC after solder bonding. The dimensions of the opening are 70 μm $\times$ 40 μm $\times$ 70 μm. The AuSn bump with the diameter of 60 μm on the Si interposer is used for flip-chip bonding with the probe. The fabricated Si platform with ten slots for ten probes is shown in figure 7(*e*). Figure 7(*f*) shows the magnified view of the slot, cavity and fixing slot of the Si platform. During the probe array assembly, the probes are inserted into the slots with the width of 80 μm and the Si interposers fit into the cavities of the Si platform. In order to firmly hold the probes inside the slots, the assembly pins of the probe are locked by the fixing slots of the Si platform, as indicated in

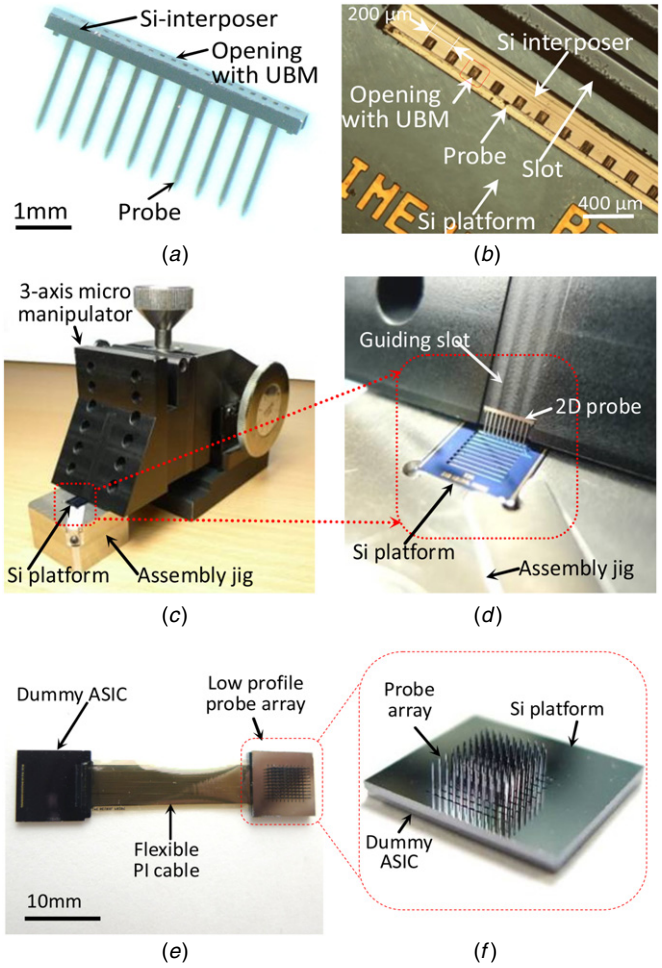

Figure 8. Assembly results. (*a*) Probe bonded with the Si interposer. (*b*) Si platform with the probe and Si interposer inserted into its slot. (*c*) Probe array assembly process by using a 3-axis micromanipulator. (*d*) Magnified view of the 2D probe bonded with the Si interposer sliding into the slot of the Si platform. (*e*) Assembled 3D probe array integrated with the dummy wireless power/data ASIC and the PI cable. (*f*) Magnified view of the low-profile probe array.

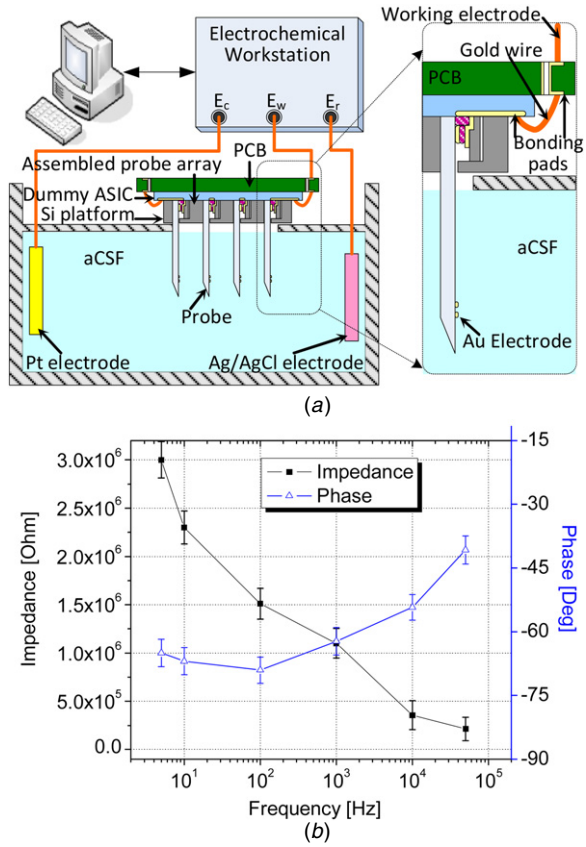

Figure 9. (*a*) Measurement setup for electrode impedance characterization. (*b*) Measured electrode impedance of the assembled probe.

figure 7(*f*). Therefore, the probes can be precisely aligned and fixed with the Si platform without any additional structures, such as spacers. The cross section of the Si platform (along the line EE' in figure 7(*e*)) is shown in figure 7(*g*) together with various dimensions of the cross section. Figure 7(*h*) shows the fabricated dummy ASIC.

Figure 8 illustrates the results of the 3D 10 × 10 probe array assembly. As shown in figure 8(*a*), the probe with ten shafts is bonded with the Si interposer by using the flip-chip bonder, and the UBM is formed in the opening of the probe for reflow soldering with the dummy ASIC. After that, the Si platform is clamped by an assembly jig and then the probe assembled with the Si interposer is inserted into the slot of the Si platform, as shown in figure 8(*b*). The pitch of the openings is 200 μm. The depth of the openings is 40 μm, as shown in figure 7(*d*). Figures 8(*c*) and (*d*) show the probe assembly process using a 3-axis micromanipulator. The minimum positioning resolution of the micromanipulator is 25 μm. The Si platform is clamped in the central cavity of assembly jig, and the guiding slot (figure 8(*d*)) is aligned by using the micromanipulator and microscope. Then, the 2D probe bonded with the Si interposer can easily slide into the slot of the Si platform. Figure 8(*e*) shows the picture of the integrated microsystem including a 3D 10 × 10 probe array with a dummy neural recording ASIC, a dummy wireless power/data link ASIC and a flexible PI cable. By using the flexible PI cable, the recorded neural signal and the extracted power supply can be exchanged between two ASICs, while keeping the recording ASIC together with the probe array for high-quality recording and placing the wireless link ASIC on the skull to minimize distance to the external unit. Figure 8(*f*) shows the zoomed-in view of the low-profile probe array bonded with the dummy recording ASIC.

4.2. Electrical characterization of the assembled neural probe array

The electrode impedance of the 3D probe array has been measured to evaluate its electrical characteristics. The three-electrode setup depicted in figure 9(*a*) is used to measure the impedance of the probe. For the assembled probe array, the Au electrodes at the probe tip are electrically connected to the bonding pads of the dummy ASIC using the Si interposer. In order to facilitate the experiment setup, the assembled probe array is glued onto the printed circuit board (PCB) and the bonding pads of the dummy ASIC are connected to the

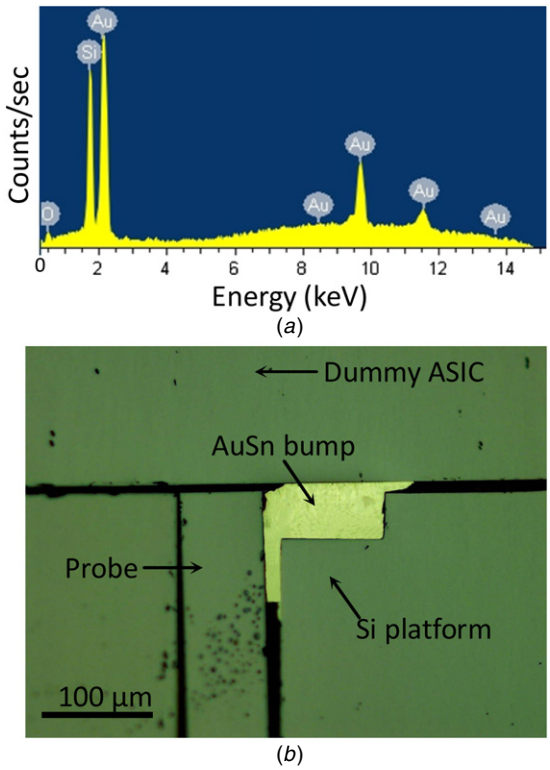

Figure 10. (*a*) EDX spectrum measured at the opening of the Si interposer. (*b*) Cross section of the probe array assembled with the dummy ASIC.

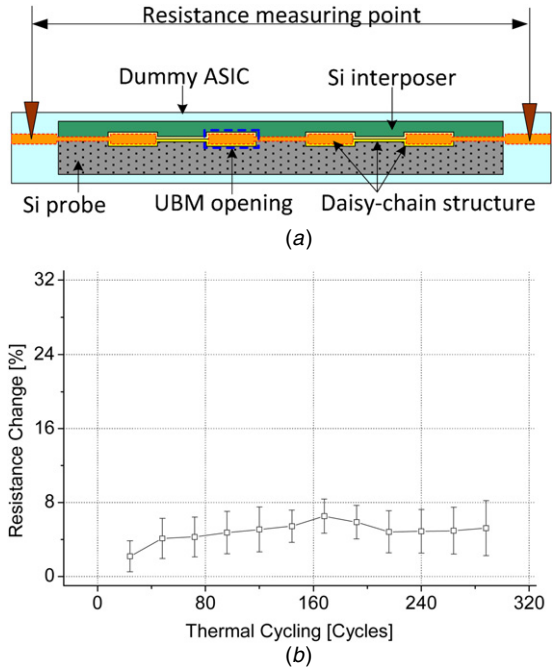

Figure 11. (*a*) Schematic of the daisy-chain structure for temperature cycling test. This figure is not to scale. (*b*) Resistance change of the assembled probe with the dummy ASIC when exposed to temperature cycles from −40 to 125 °C during a period of 288 h corresponding to 288 cycles.

pads on the PCB by wire bonding, as shown in figure 9(*a*). The magnitude and phase components of the probe electrode impedance are measured by the electrochemical workstation (CH Instruments Inc.). The working electrode (E_w) of the electrochemical workstation is soldered with the pad of the PCB. The working electrode is electrically connected to the probe electrode. In order to simulate the implantation conditions, the assembled probe array is immersed in the artificial cerebrospinal fluid (ACSF, consisting of 124 mM NaCl, 4.4 mM KCl; 1.2 mM $MgSO_4$, 1 mM NaH_2PO_4, 2.5 mM $CaCl_2$, 26 mM $NaHCO_3$, 10 mM glucose) during the measurement of the electrical characteristics. An Ag/AgCl wire is used as a reference electrode (E_r) and a platinum (Pt) electrode is used as a counter electrode (E_c). A sinusoidal AC voltage with a peak-to-peak amplitude of 10 mV was applied with varying the frequency from 5 Hz to 50 kHz to measure the impedance of the electrode on the assembled microprobe array. The impedance measurement results of 183 electrodes are shown in figure 9(*b*). The impedance is mainly capacitive and the magnitude of the average impedance measured at 1 kHz is about 1.1 MΩ. The measured impedance is somewhat high but acceptable for recording [25, 26]. The electrode impedance can be reduced by increasing the size of the active site or using lower-impedance electrode materials, such as Pt or IrO_x.

4.3. Testing of interconnection properties

Figure 10(*a*) shows the energy dispersive x-ray (EDX) spectrum of the gold in the opening of the Si interposer (measured at the spot 'A' indicated in Figure 7(*d*)). The EDX is used for qualitative and quantitative elemental analysis. Base on the measured EDX spectrum, the presence of gold is evidently indicated by two principal emission lines at about 2.12 and 9.71 keV. The gold has been completely deposited inside the opening of the Si interposer, and hence the electrodes of the probe can be successfully connected to the opening of the Si interposer after flip-chip bonding. Figure 10(*b*) shows the cross section of the assembled probe array. The overall bonding structure of the assembled probe array can be observed. The AuSn bump of the dummy ASIC is successfully soldered with the UBM in the opening of the probe bonded with the Si interposer after reflow soldering.

As shown in figure 7(*h*), a daisy-chain test structure is patterned on the dummy ASIC. The structure is designed for investigating resistance changes of the interconnection under thermal cycling condition. The electrical connection of the daisy-chain is completed through the Si interposer and dummy ASIC after the probe assembly and packaging, as shown in figure 11(*a*). The assembled probes are subjected to a JEDEC package-level reliability test with temperature cycling [27]. This thermal cycling test is conducted to determine the ability of the Si interposer and dummy ASIC to withstand mechanical stresses induced by alternating high and low temperature extremes. Figure 11(*b*) shows the average resistance change of the daisy-chain structure in the assembled probe with the dummy ASIC when exposed to temperature cycles from −40 to 125 °C. The thermal cycling test covers a period of 288 h corresponding to 288 temperature cycles. Twenty daisy-chain samples are taken after every 24 cycles to assess the reliability of interconnect. The initial resistances of twenty samples are measured from 11 to 31 Ω. Any daisy-chain with a resistance

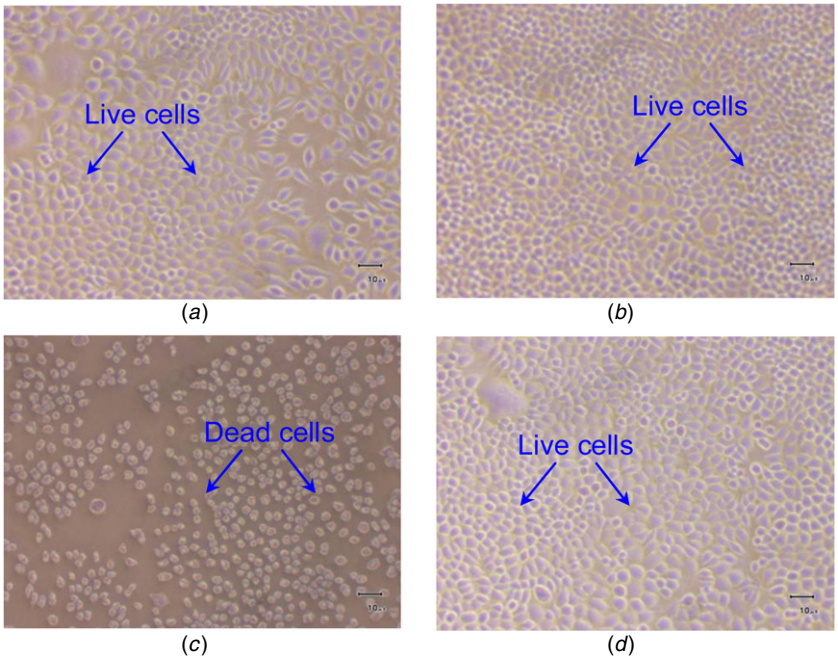

Figure 12. *In vitro* cytotoxicity results. (*a*) S1: AuSn, (*b*) S2: HDPE (negative control), (*c*) S3: zinc sulfate solution (positive control), and (*d*) S4: reagent blank.

of 20% deviation from the initial resistance value of that daisy-chain structure is considered as a failure. As shown in figure 11(*b*), resistance changes of all the test samples are less than 10% of their initial resistance values.

4.4. In vitro cytotoxicity test and in vitro signal acquisition

In order to evaluate the biocompatibility of AuSn bumps on Si interposers or dummy ASIC, *in vitro* cytotoxicity test subjected to ISO 10993–5 standards [28] has been conducted. Cell culture is used to evaluate the cytotoxic effect as per ISO 10993–5 recommendation. NCTC clone 929 mouse connective tissue cell line (ATCC No. CCL-1) is used in this study. Four samples, S1∼S4 (S1: AuSn, S2: high-density polyethylene (HDPE, negative control), S3: zinc sulfate solution (positive control), and S4: reagent blank) are used for the *in vitro* cytotoxicity test. These samples are subjected to an extraction condition at 37 °C for 72 h to evaluate their biocompatibility. Images of four cell samples for *in vitro* cytotoxicity test are shown in figure 12. For S1, S2 and S4, no cell lysis and no reduction of cell growth are observed in figures 12(*a*), (*b*) and (*d*), respectively. For S3, nearly complete destruction of cell layers and round-shaped dead cells are shown in figure 12(*c*).

To verify the functionality of the assembled probe array, *in vitro* signal acquisitions have been performed. Figure 13 shows the experiment results. Neural signal data which was pre-recorded from dorsal raphae nucleus of a rat brain [29] is used in the *in vitro* experiment. An arbitrary waveform signal generator is used to apply the pre-recorded neural signal to the ACSF and emulate the spontaneous neural firing using an arbitrary waveform signal generator. The assembled probe array connected with a neural recording amplifier is immersed in the ACSF. The recording amplifier successfully acquires the emulated neural signal in the fluid through the assembled probe array as shown in figure 13.

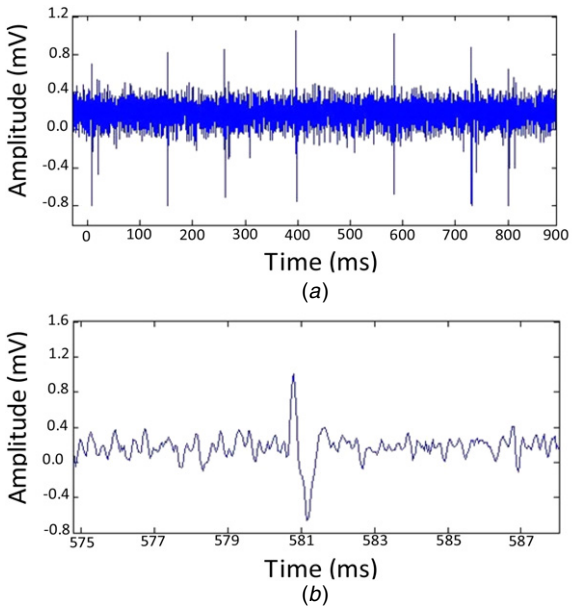

Figure 13. *In vitro* signal acquisition testing. (*a*) Pre-recorded neural signal acquisition using the assembled probe array connected with a neural recording amplifier. (*b*) Zoomed-in single spike signal.

5. Conclusions

In this paper, a microassembly method for low-profile 3D probe arrays using the silicon-based lead transfer structure has been proposed and demonstrated. The predefined slots and cavities in the Si platform are used to minimize the profile of the probe array after assembly. The slots and cavities are

designed in such a way that the probes bonded with the Si interposers can be precisely aligned and fixed with the Si platform without any additional structures, such as spacers. The profile of the assembled probe array is controlled within 750 μm above the pia mater. The Si interposer provides an effective interconnect transfer means by using standard micromachining processes and overcomes the bonding plane mismatch issue during 3D probe array assembly. The electrical interconnections between the probe and the dummy ASIC chip are formed using a reflow soldering process. In order to verify the electrical connection between the probe and the dummy ASIC, the cross section of the bonding structure has been carefully observed and discussed. The measured impedance electrode on the assembled probe array is about 1.1 MΩ at 1 kHz.

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