Homework-4

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1 Area I want to study

Area I want to explore the area under the heading " Parameterized system verification ".

2 How this area fits in "Formal Methods in Software Engineering".

How this area fits in "Formal Methods in Software Engineering". A broad area of research in computer science is known as formal verification which addresses the verification problem. Formal verification provides a mathematical reasoning and justification about a given system that whether it satisfies certain property and does what it was designed to do. It satisfies safety and liveness property. Many hardware and software systems are very large. Such systems are error prone due to complexity. Formal verification techniques like model checking can help us to explore possible behavior of the system and hence find bugs in the model. Many real-world examples consist of many concurrent components. Such examples are designed to be correct no matter how many processes are there in the system. Parameterized system is a system in which number of processes in the system is the parameter. So verification of a complex system can be decomposed into smaller system. Model checking helps to do this formal verification. A system has various states which basically represents the instance of the system at some point of time. So a system can be modelled as a set of states and transitions which describes how the system changes from one state to another in response to transition. So model checking tools can be used to verify that a desired property hold in the system or not. One alternate way to verify parameterized system can be to use theorem provers. In this technique people can write lemmas about the system and prove them using theorem proving technique.

3 How this area relates to topic covered in class

How this area relates to topic covered in class A model or system under consideration for model checking can be represented by Kripke structure. The mathematical assertion of the states of the system over time can be represented by temporal logics. The temporal logics CTL is widely used to represent properties of a system in terms of set of atomic steps taken by the system. Binary decision diagrams can be also used to represent state-transition relation of a system under consideration.

References

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