
Superconducting Coplanar Waveguide Resonators as a Diagnostic Tool for Quantum Circuits

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Quantum Information and Integrated Nanosystems Group



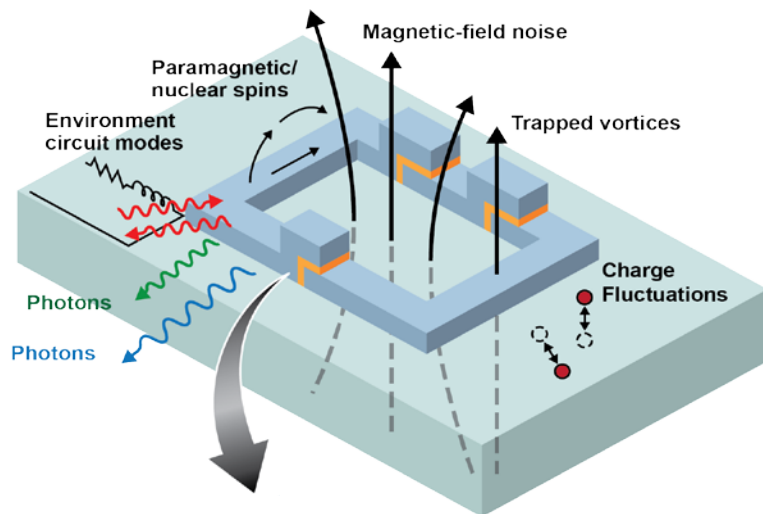
Boulder, CO

February 8, 2018



Noise and Loss in Superconducting Quantum Circuits

Sources of Noise and Loss

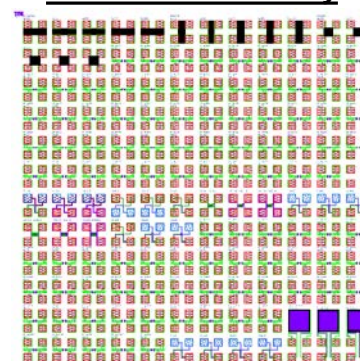


Oliver and Welander, MRS Bulletin 38, 816 (2013)

**Wanted:
Diagnostic tools
for studying
sources of noise
and loss**

Analogous to...

CAD of JJ Test Array



RT Electrical Testing



<u>Challenge</u>	<u>Requirement</u>
Fab, measurement time + resources	Need surrogate device/probe
Device-to-device variability	Statistical measurement and analysis
Low T, vacuum, "quiet" EM environment	Realistic operating conditions
Competing signals/behavior	Model or mitigate other mechanisms

Goal: Use statistical device testing of superconducting CPW resonators to perform quantitative analysis of TLS losses at interfaces



Outline

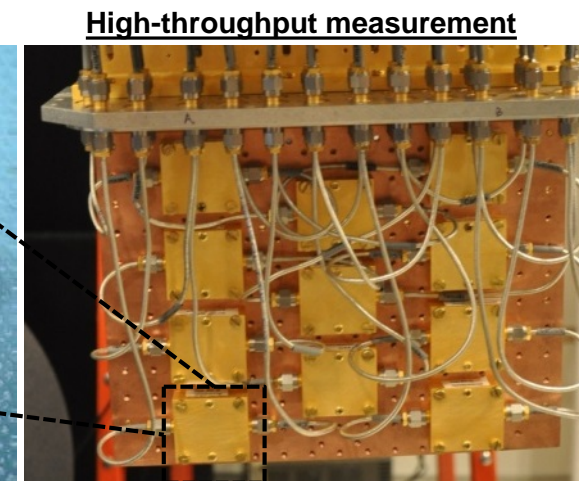
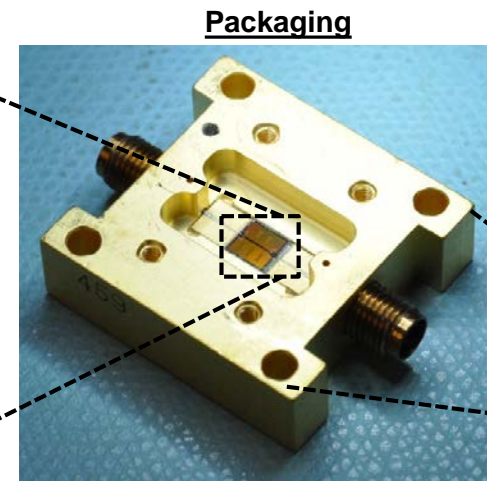
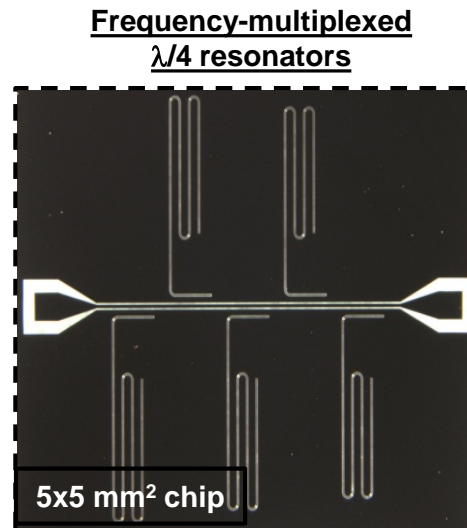
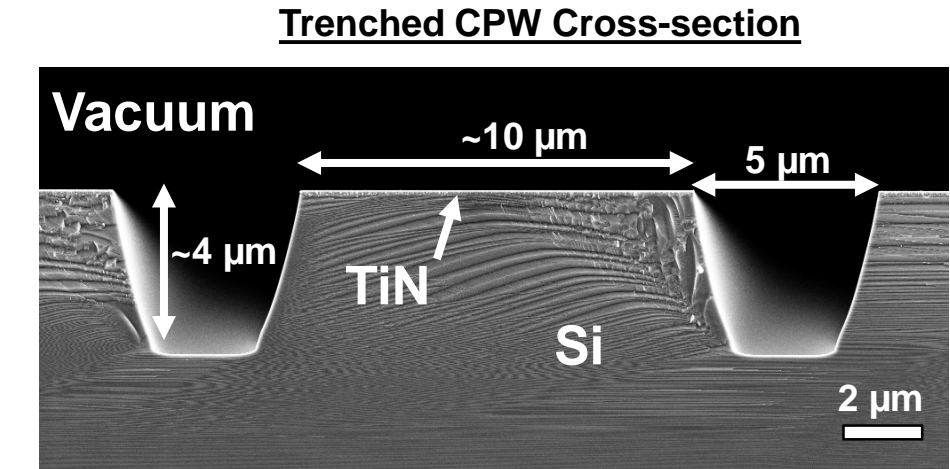
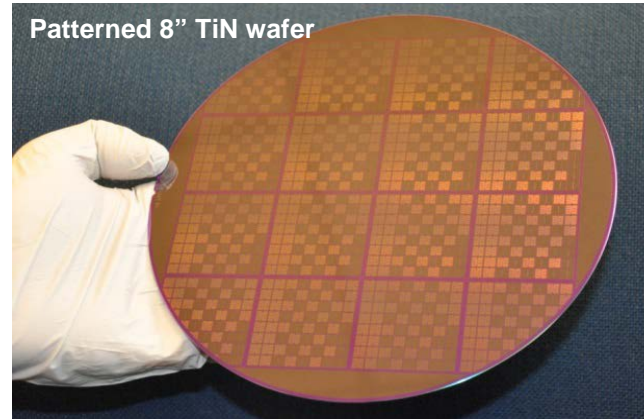
- ➔ • **A/B Testing**
- **Characterizing 3D integration**
- **Surface Loss Extraction (SLE)**
- **Sources of device-to-device variability**



High-throughput Fabrication and Testing

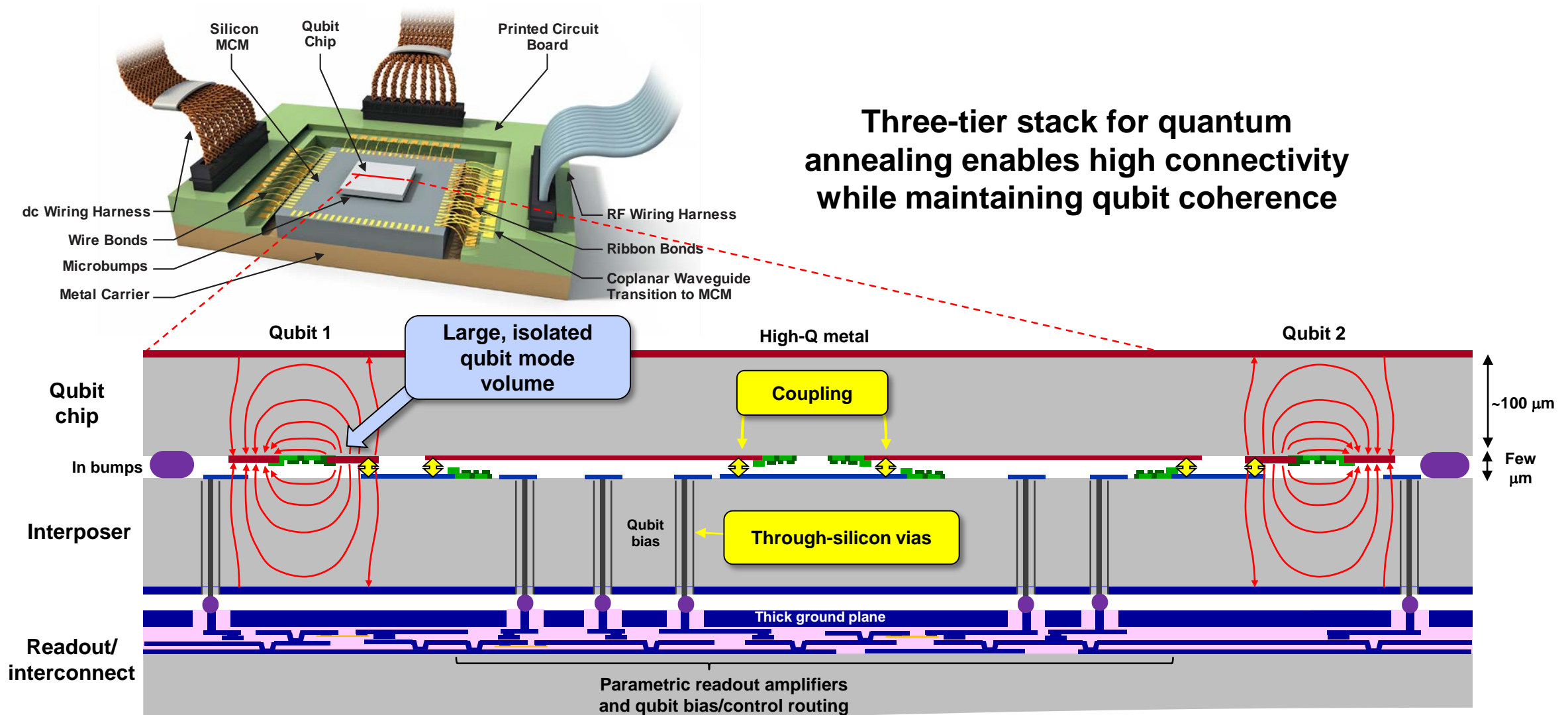
- **Fabrication**
 - 8-inch toolset
 - In-house process characterization and analysis
- **Measurement**
 - Automated device characterization and statistical analysis
 - 2 banks x 6 chips x 5 resonators → 60 per DR cooldown
- **Best process: mean Q_i ~2.2 million**

Established, highly reproducible
high-Q TiN process
& high-throughput statistical
device characterization



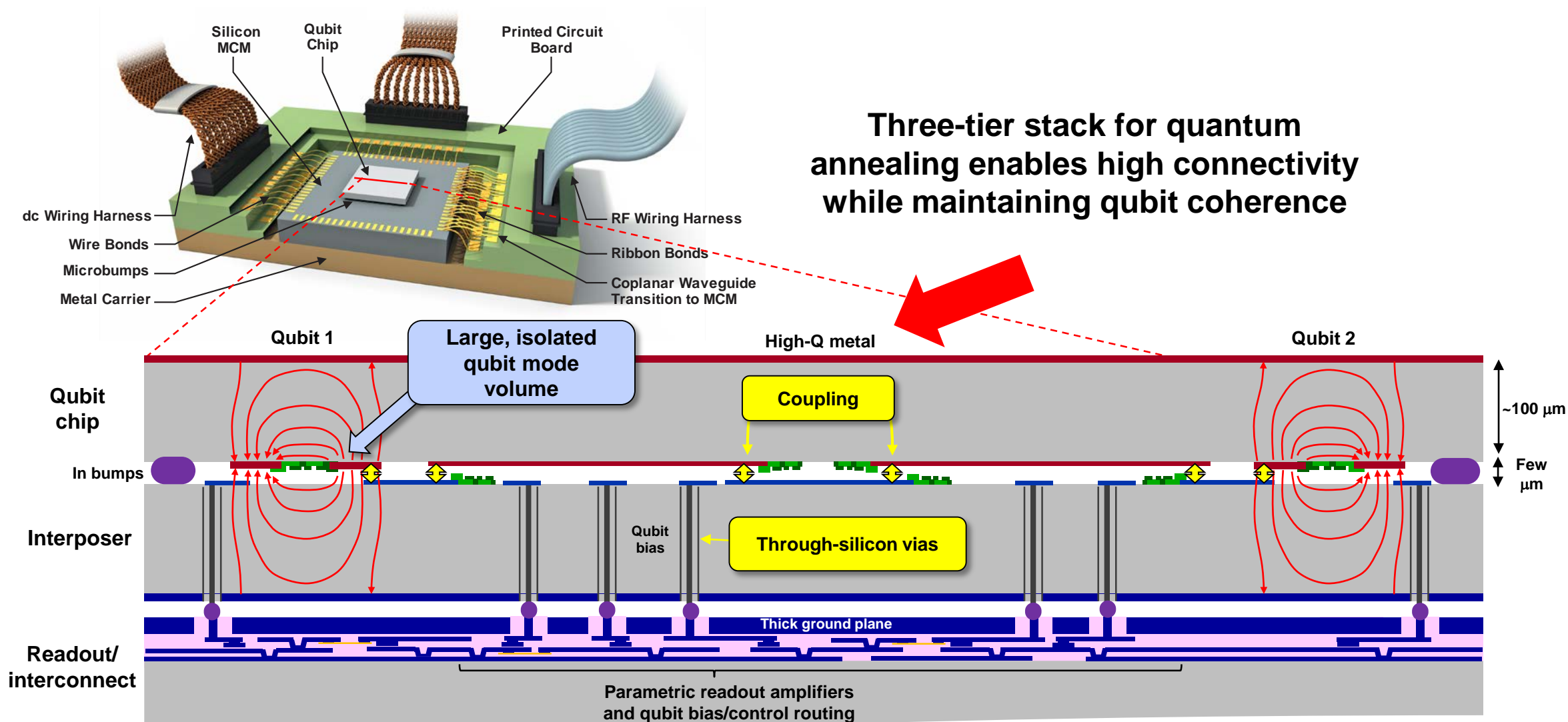


Can we use resonators to qualify new chip fab/materials,...?



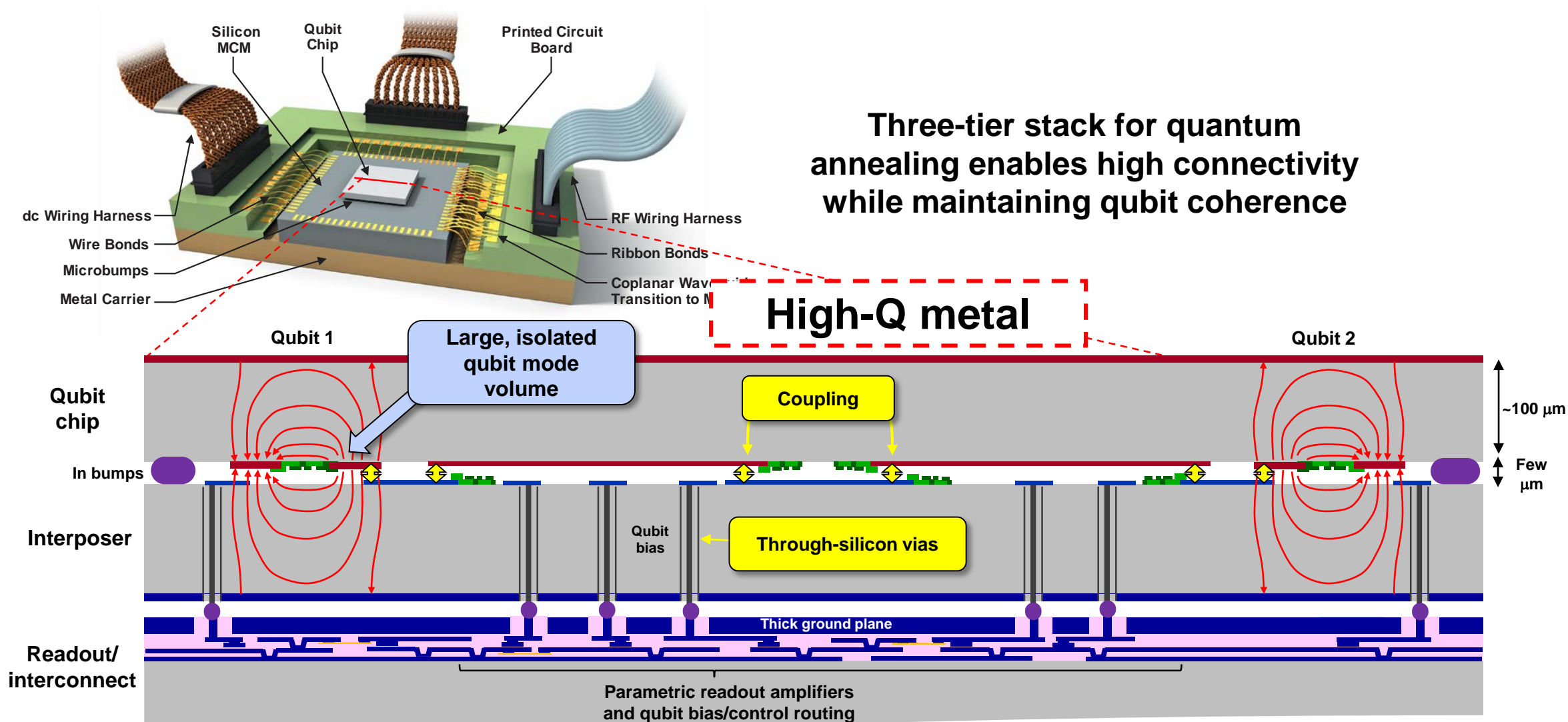


Can we use resonators to qualify new chip fab/materials,...?





Can we use resonators to qualify new chip fab/materials,...?





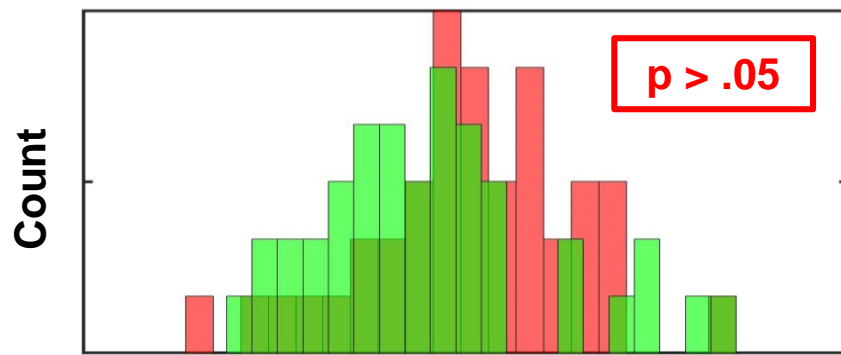
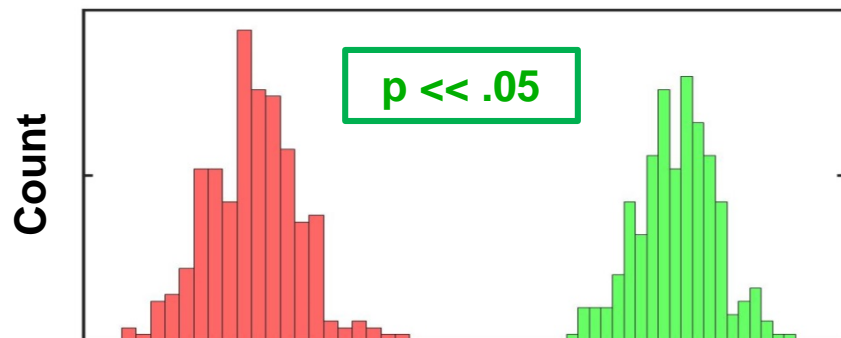
A/B Testing, or “The Canary in the Coal Mine”

How do we decide if two sampling distributions are different?

Statistical hypothesis testing: Welch’s t-test

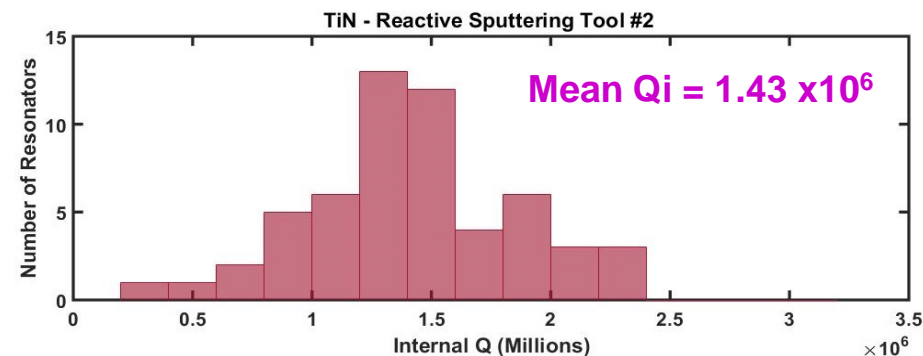
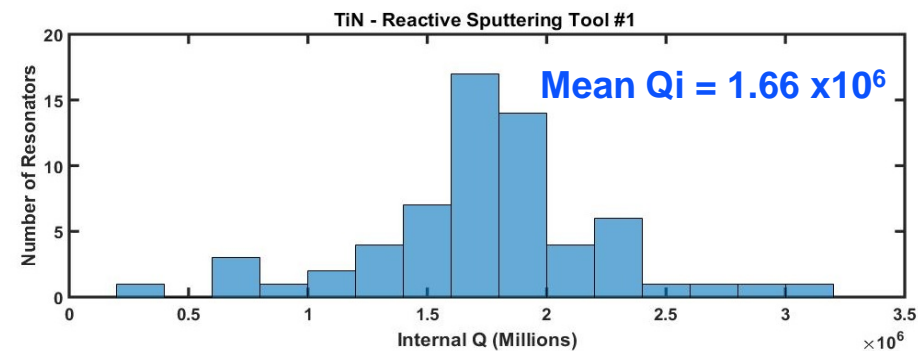
p-value: the statistical probability that the measured sample originate from the same parent distribution

Standard threshold for significance: $p = .05$



Sampling Metric

Example: Sputtered TiN films



TiN Sputtering Tool #1
~ 50 resonators

TiN Sputtering Tool #2
~ 50 resonators


Mean Qi = 1.66×10^6

Mean Qi = 1.43×10^6

$p < .0057 \rightarrow$ statistically significant

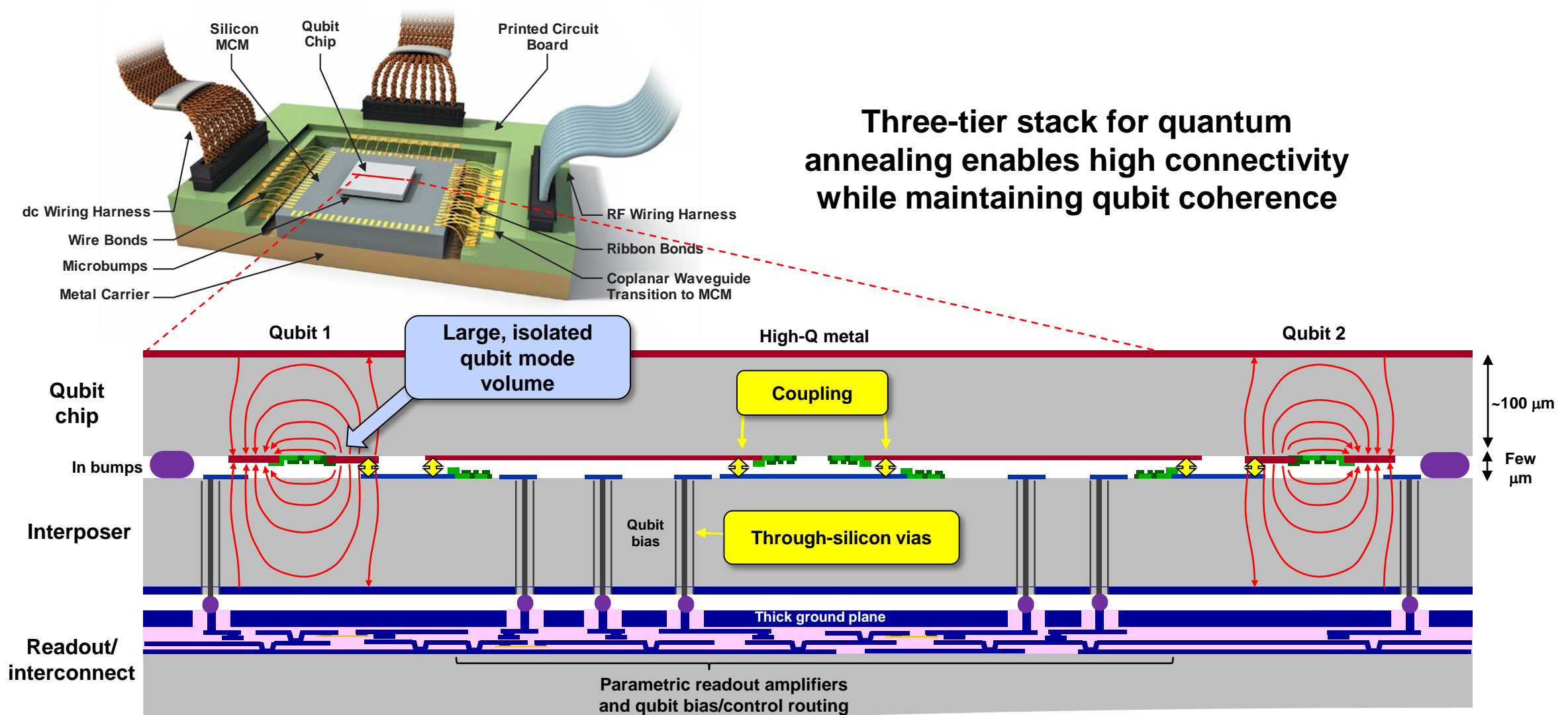


Outline

- **A/B Testing**
-  • **Characterizing 3D integration**
- **Surface Loss Extraction (SLE)**
- **Sources of device-to-device variability**

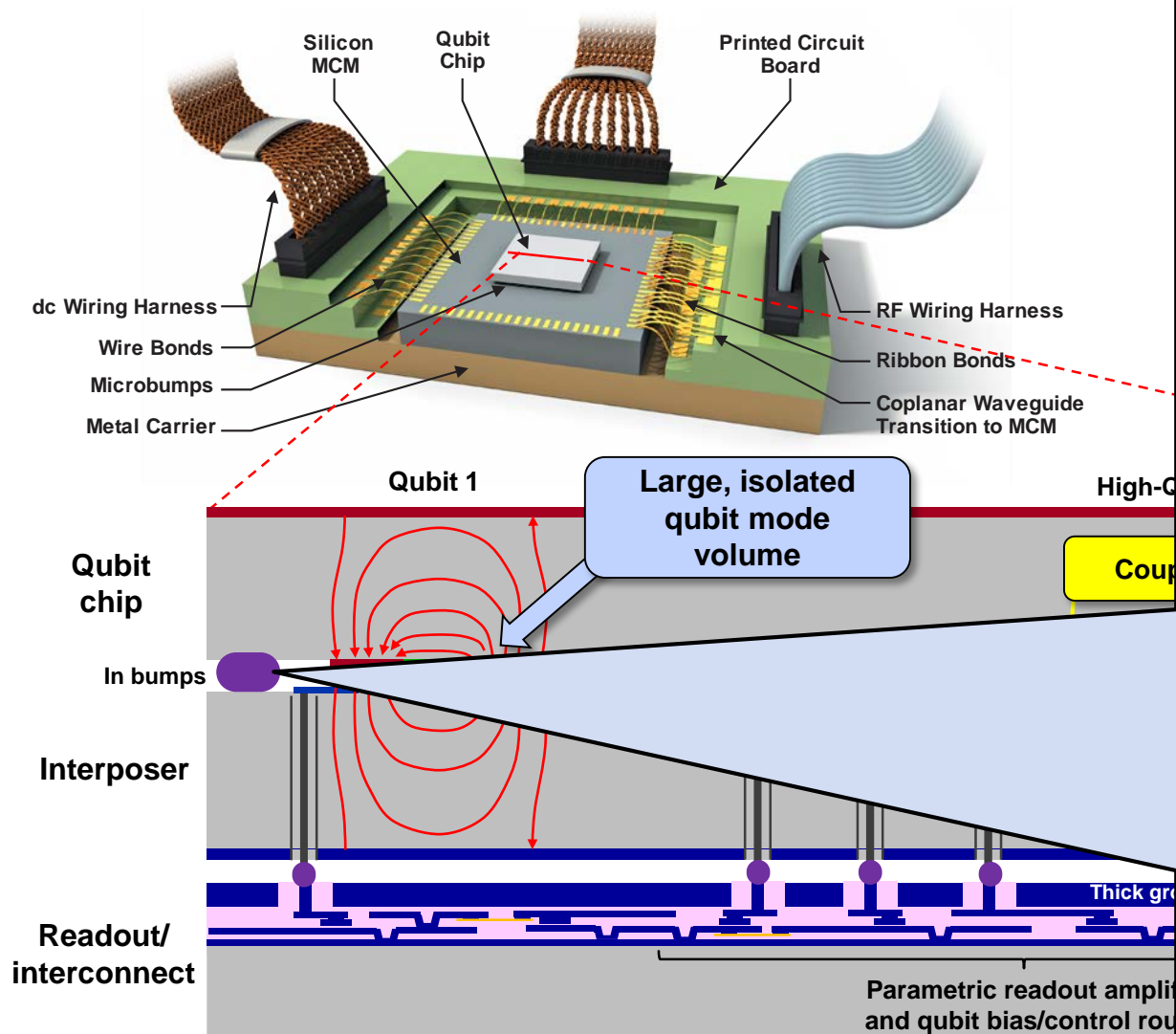


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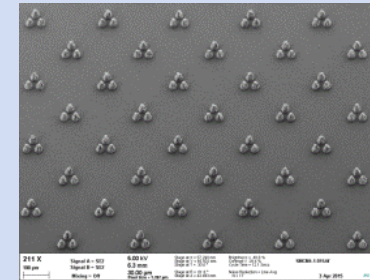


Can we use resonators to qualify new chip fab/materials,...?



Indium bumps connect chips and provide mechanical support

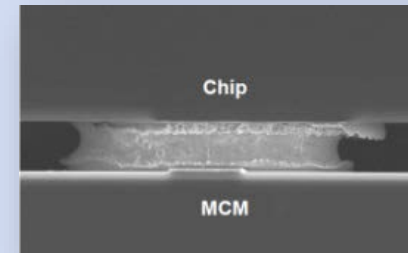
Fabricated In bumps



Confocal image of indium bumps on TiPtAu



Cross-section of bump-bonded chips



IR image of bump-bonded chips

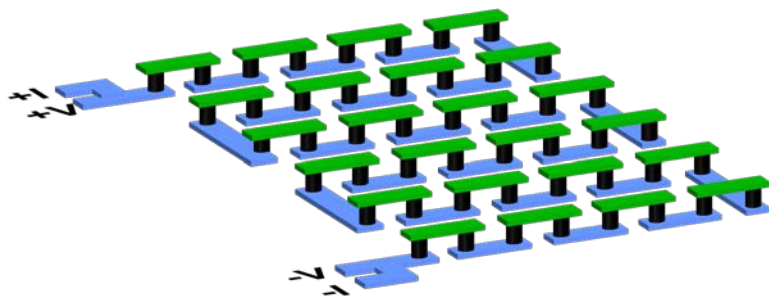


Alignment $\sim 1 \mu\text{m}$

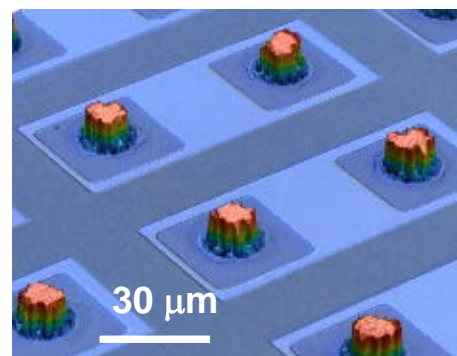


Electrical Properties of Bump Path

Schematic of test structure for DC resistance

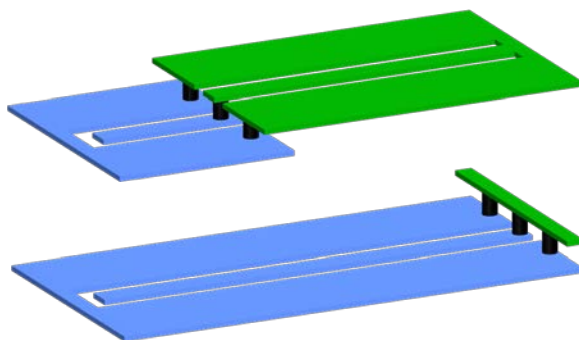


Confocal image of indium bumps on underbump metallization

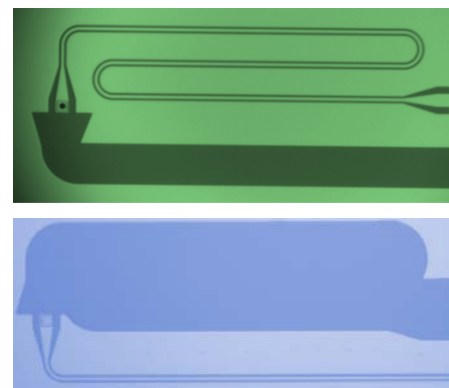


- 2,704 indium bumps in series
- Base metal Al
- TiPtAu underbump metal

Schematic of quarter wave resonators with bump interconnects



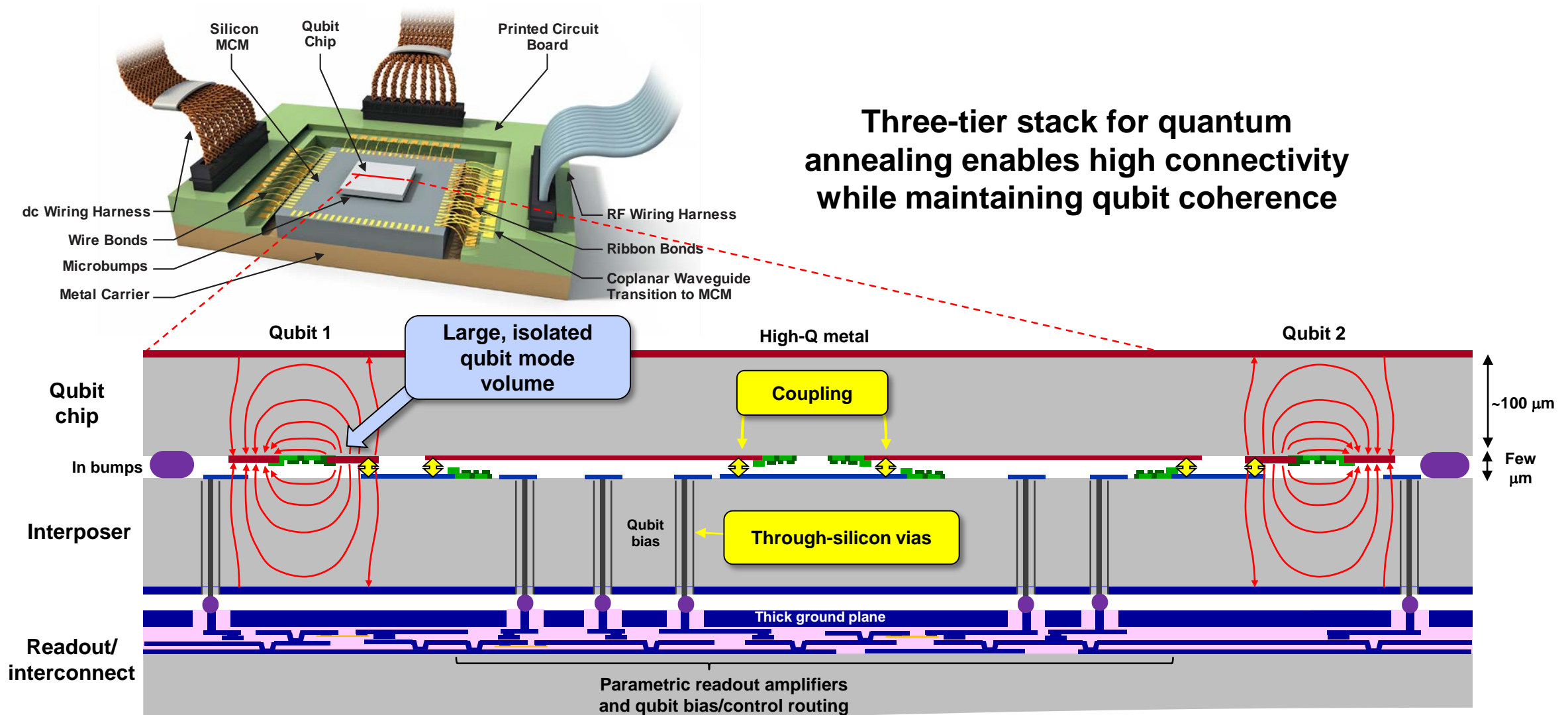
Fabricated resonator with bump interconnects



- Bump-interrupted resonators with ~50-100k internal Q
- Effective microwave loss of 100's of μohm

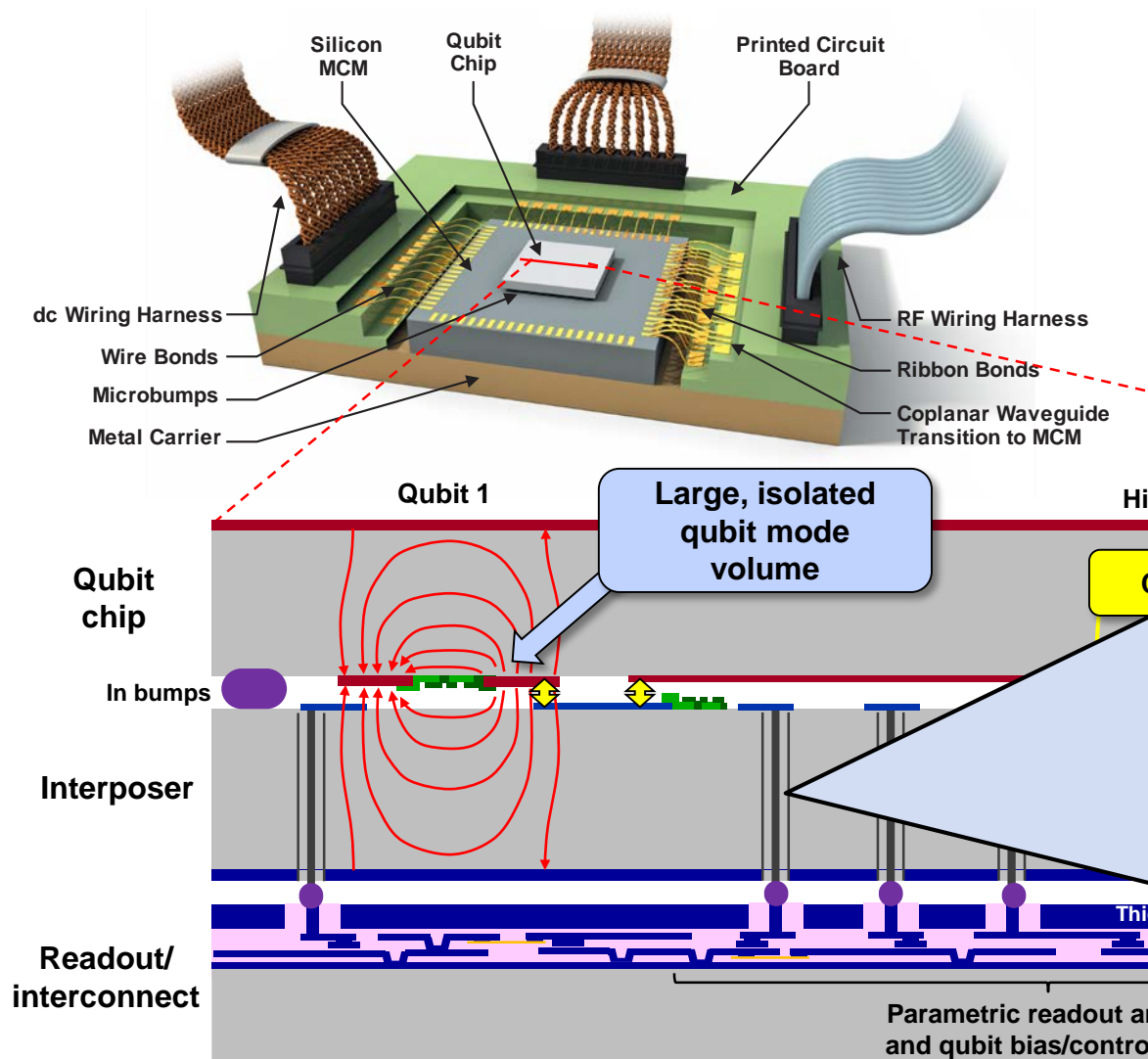


Can we use resonators to qualify new chip fab/materials,...?

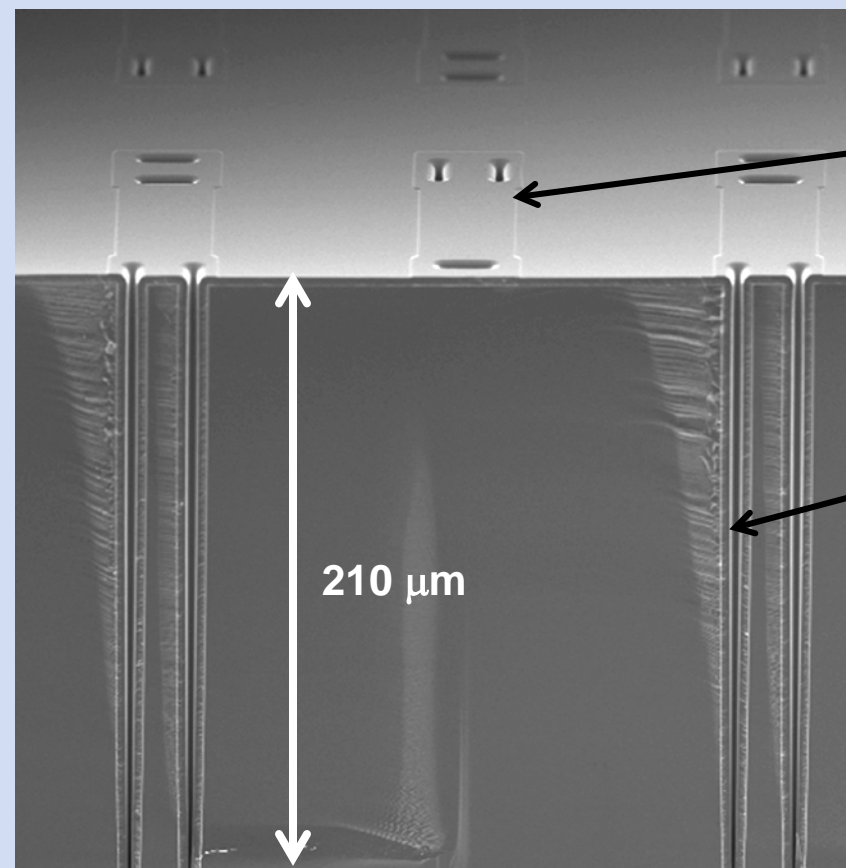




Can we use resonators to qualify new chip fab/materials,...?



Interposer separates qubit from readout/interconnect layer

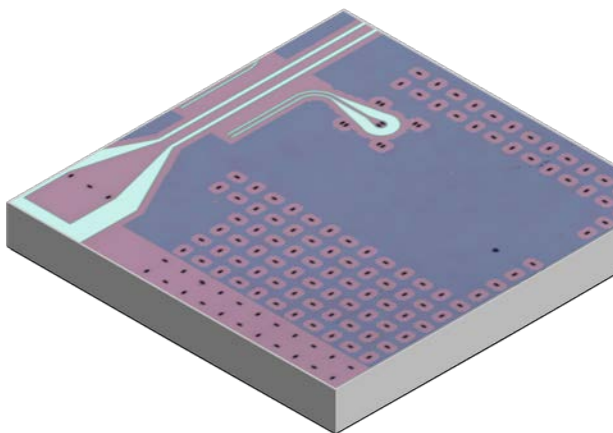
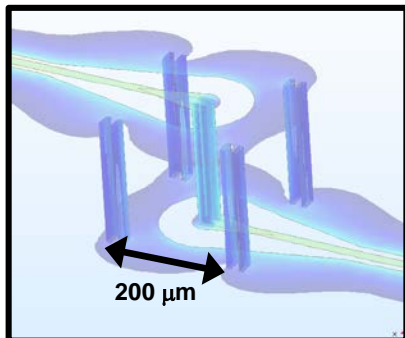


Superconducting through-silicon vias provide connectivity between top and bottom layers

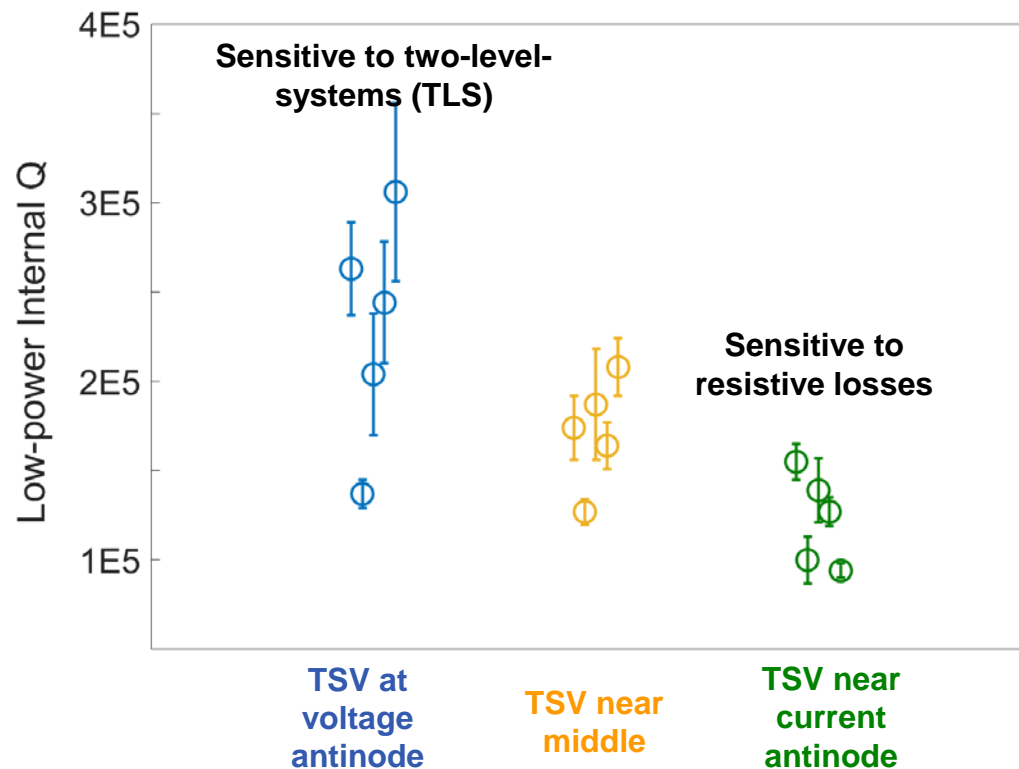


Resonators with TSV interconnects

Simulation of TSV transition




Dependence of internal Q on position of TSV transition



Resonator measurements indicate high-bandwidth, low-loss TSV transitions



Outline

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- **Sources of device-to-device variability**



COMSOL: FEM Mesh



- **MS: metal-to-silicon**
- **SA: substrate-to-air**
- **MA: metal-to-air/vacuum**
- **Si: silicon substrate**

Matrix Representation

$$\begin{bmatrix} \frac{1}{Q_1} \\ 1 \\ \frac{1}{Q_2} \\ 1 \\ \frac{1}{Q_3} \\ \vdots \end{bmatrix} = \begin{bmatrix} P_{MS_1} & P_{SA_1} & P_{MA_1} & P_{Si_1} \\ P_{MS_2} & P_{SA_2} & P_{MA_2} & P_{Si_2} \\ P_{MS_3} & P_{SA_3} & P_{MA_3} & P_{Si_3} \\ \vdots & \vdots & \vdots & \vdots \end{bmatrix} \begin{bmatrix} x_{MS} \\ x_{SA} \\ x_{MA} \\ x_{Si} \end{bmatrix}$$

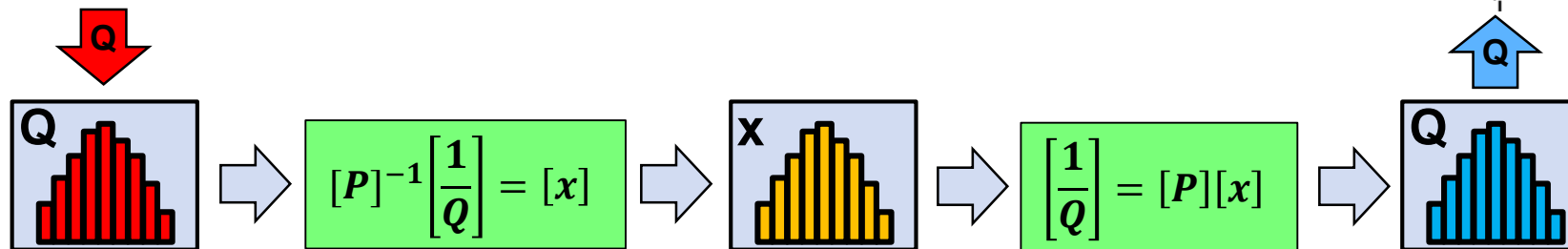
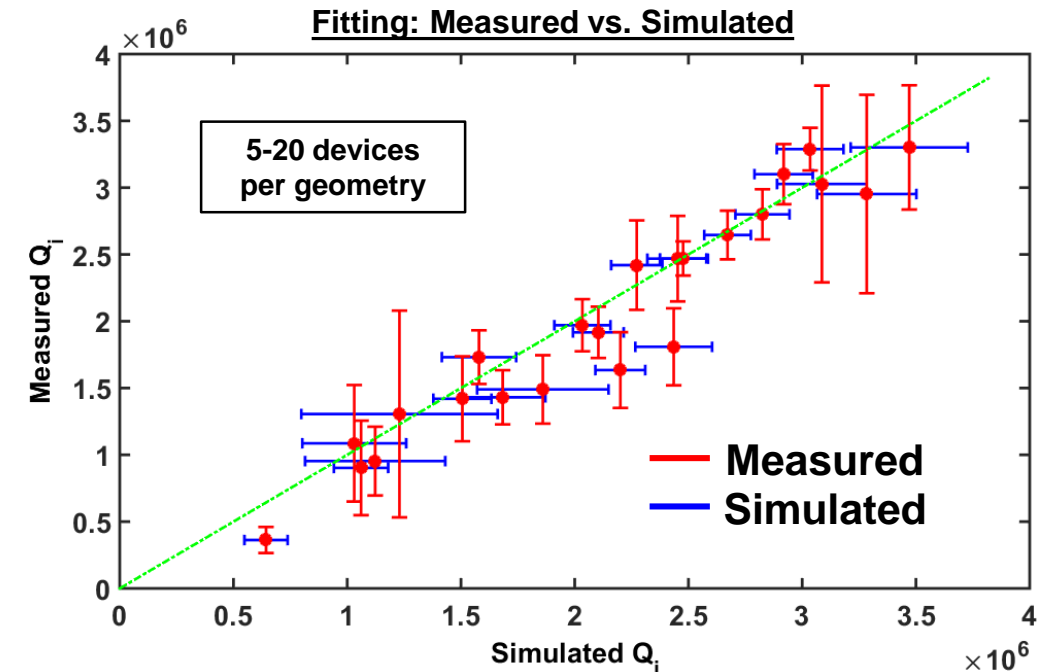
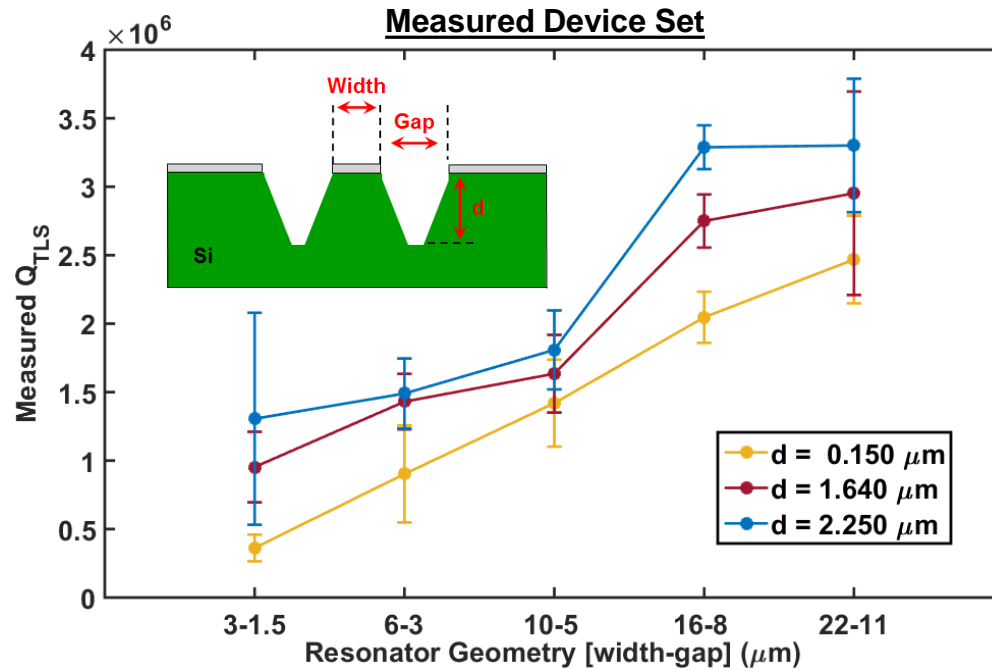
← Measured
Solve for →

From EM simulation

Loss-factors (tangents) can be extracted directly from TLS-limited Q_i



Device Loss Modeling

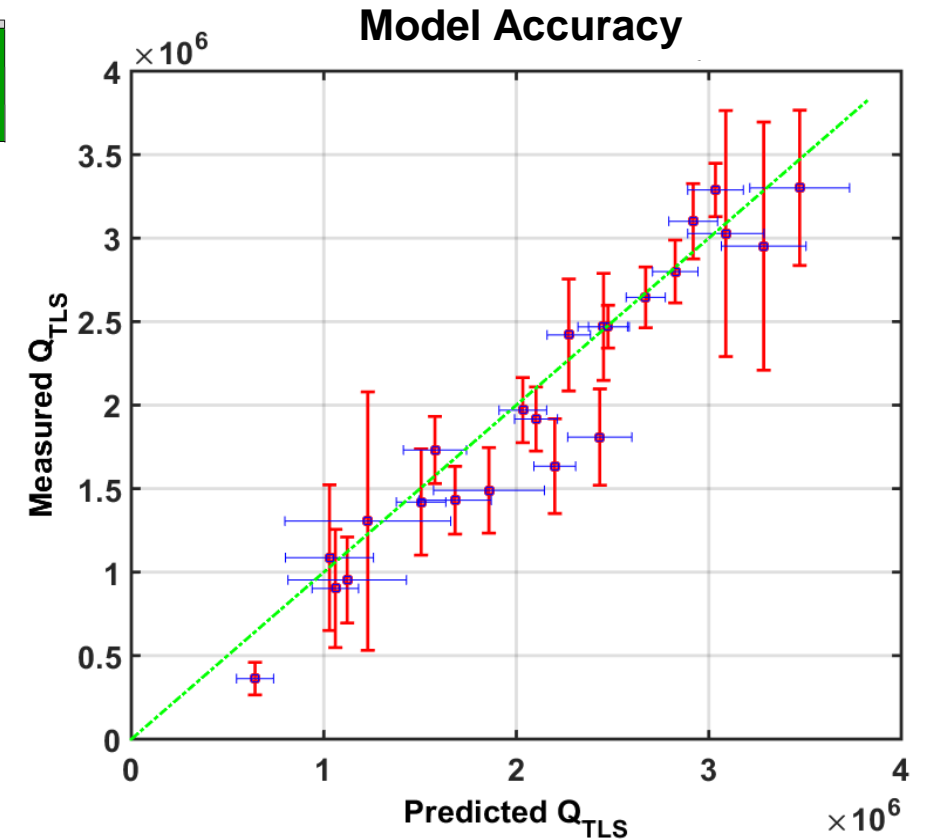
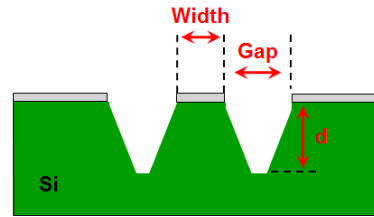
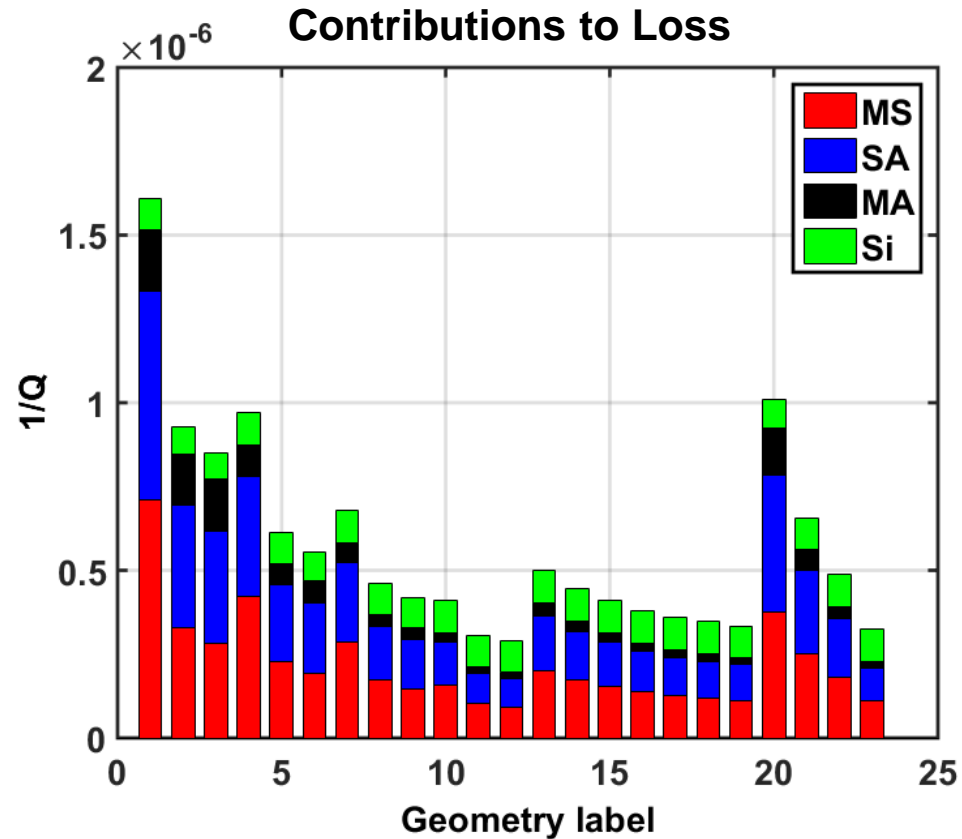


- Monte Carlo analysis estimates uncertainty in extracted losses

- Uncertainty contributions: singularity of participation matrix, variation in measured Q , inaccuracy of model assumptions....



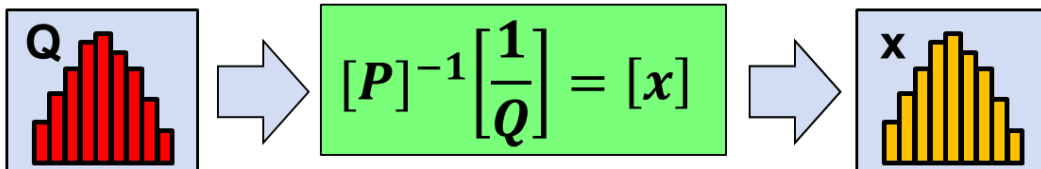
Limits of Anisotropic Trenching



Participation ratios proportional across all geometries,
(some) predictive power still possible



Improving Matrix Condition Number



Ideal $[P]$

$$P = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

$$\text{condition}(P) = 1$$

$$\frac{\sigma(X)}{\mu(X)} \approx \frac{\sigma\left(\frac{1}{Q}\right)}{\mu\left(\frac{1}{Q}\right)}$$

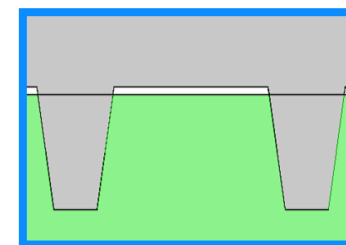
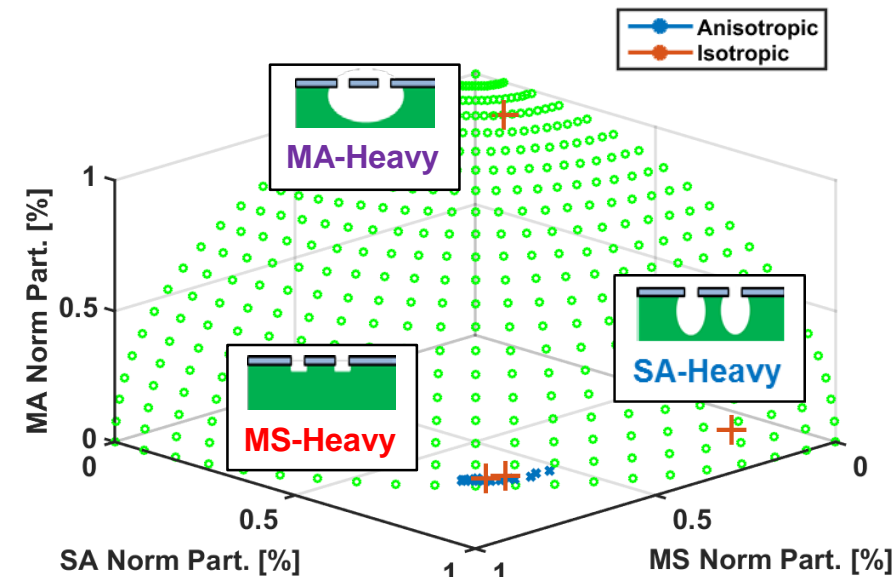
Anisotropic Trenching Example $[P]$

$$P = \left(\frac{1}{100} \right) \begin{bmatrix} 0.1694 & 0.1607 & 0.0048 & 90.8956 \\ 0.3069 & 0.4136 & 0.0272 & 69.8413 \\ 0.2488 & 0.2841 & 0.0109 & 82.7197 \\ 0.1001 & 0.1066 & 0.0029 & 87.6096 \end{bmatrix}$$

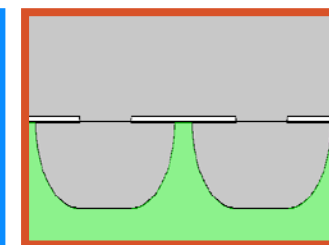
$$\text{condition}(P) = 61937$$

$$\frac{\sigma(X)}{\mu(X)} \gg \frac{\sigma\left(\frac{1}{Q}\right)}{\mu\left(\frac{1}{Q}\right)}$$

Resonators: normalized (MS,SA,MA) participation vectors:



Anisotropic trenching



Isotropic trenching

Condition number of $[P]$: how sensitive is $[X]$ to changes in $[1/Q]$

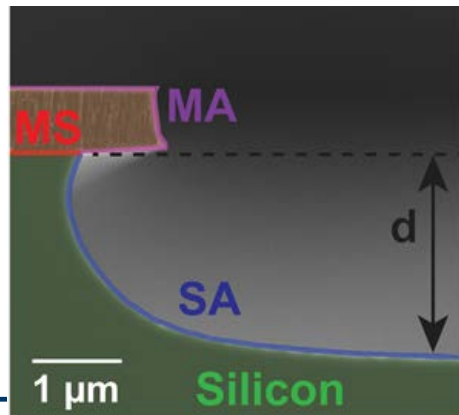
Planar, anisotropic trenching \rightarrow large condition # \rightarrow large uncertainty

Isotropic trenching \rightarrow reduced condition # ($\sim 30\times$)



Targeting Dielectric Loss

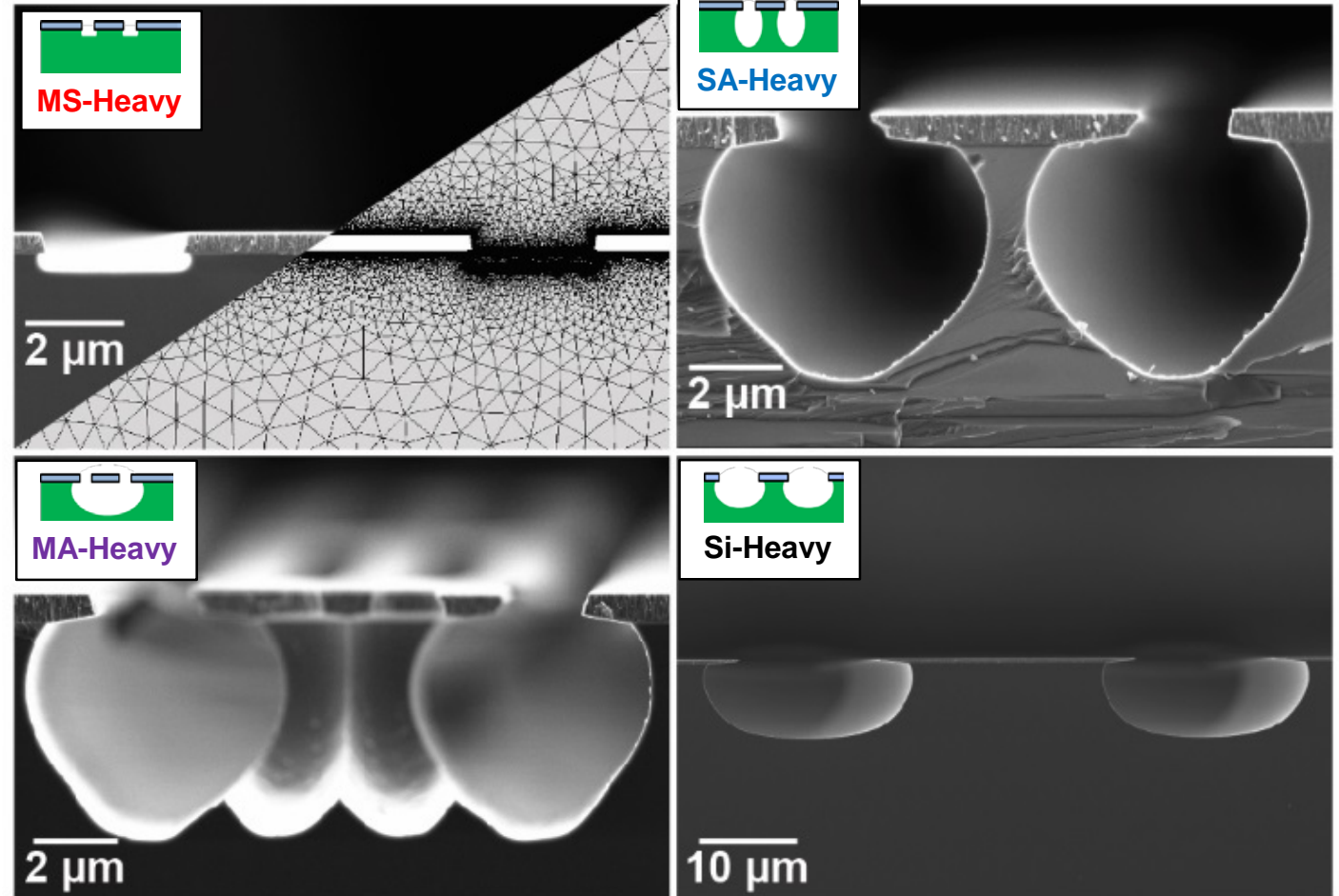
- Isotropic etched resonators
- COMSOL estimated participation vectors
- Four optimal resonators identified
 - Over a range of geometries considered
 - Produced participation matrix with lowest condition number



TLS-containing interfaces:

- MS: metal-to-silicon
- SA: substrate-to-air
- MA: metal-to-air/vacuum
- Si: silicon substrate

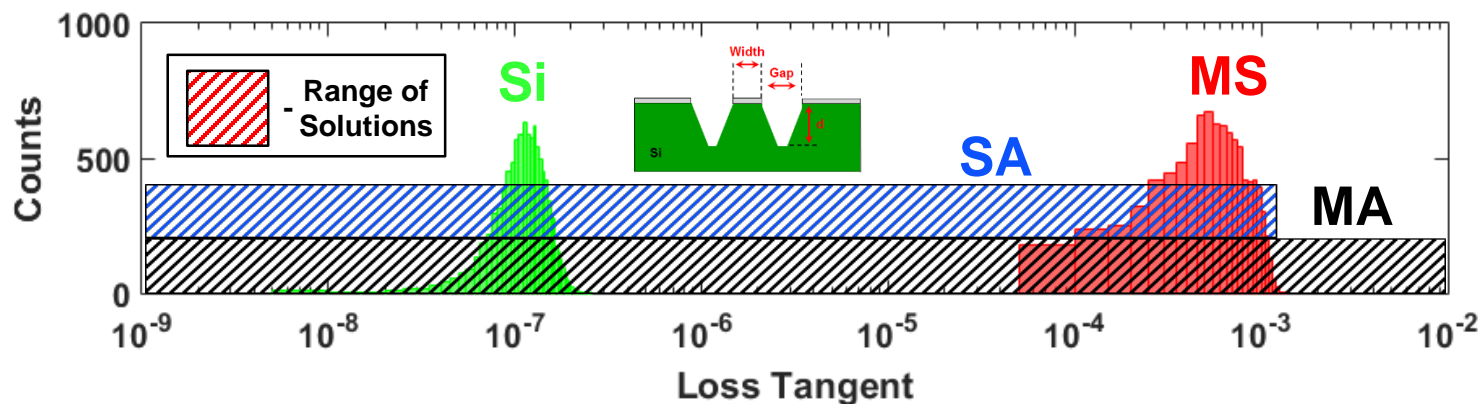
SEM Cross-sections of Optimal 4 Cross-Sections



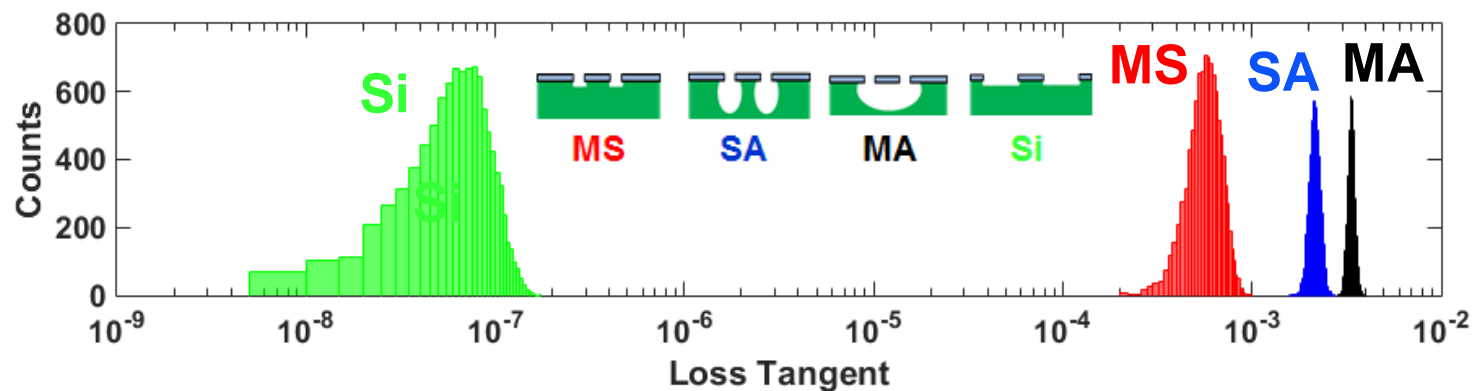


Surface Loss Extraction

Anisotropic



Isotropic



tan δ assumes:

$$t_{MS} = 2 \text{ nm}, \epsilon_{MS} = 11.35\epsilon_0$$

$$t_{SA} = 2 \text{ nm}, \epsilon_{SA} = 4\epsilon_0$$

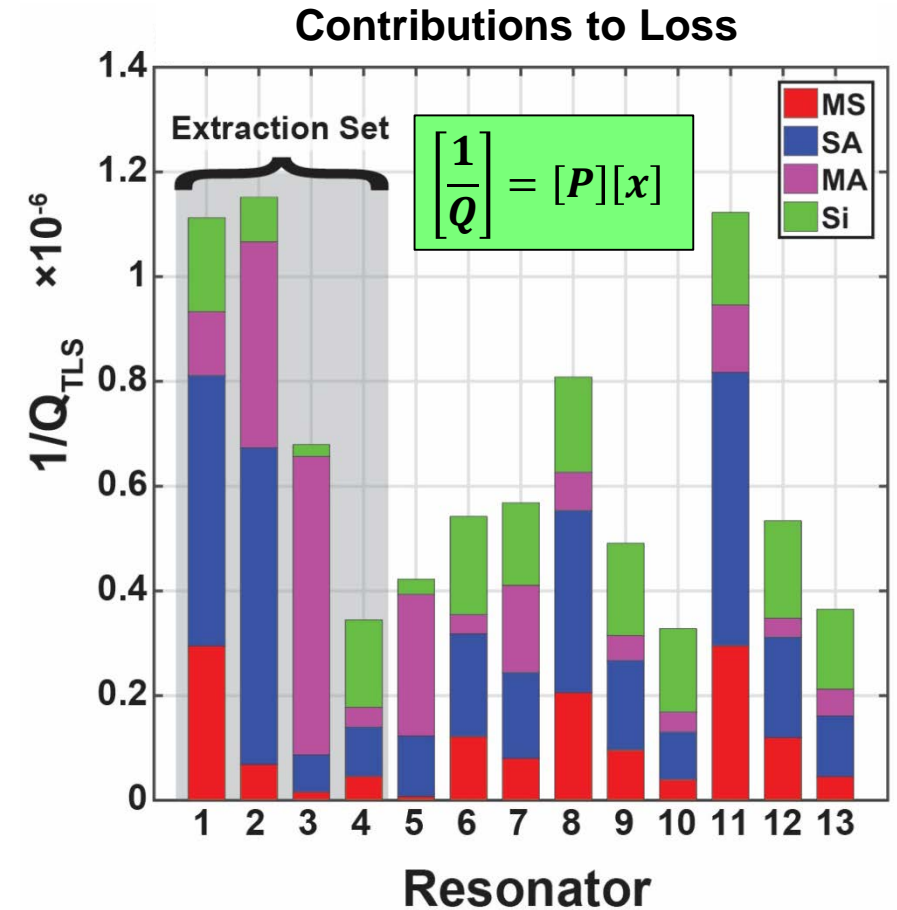
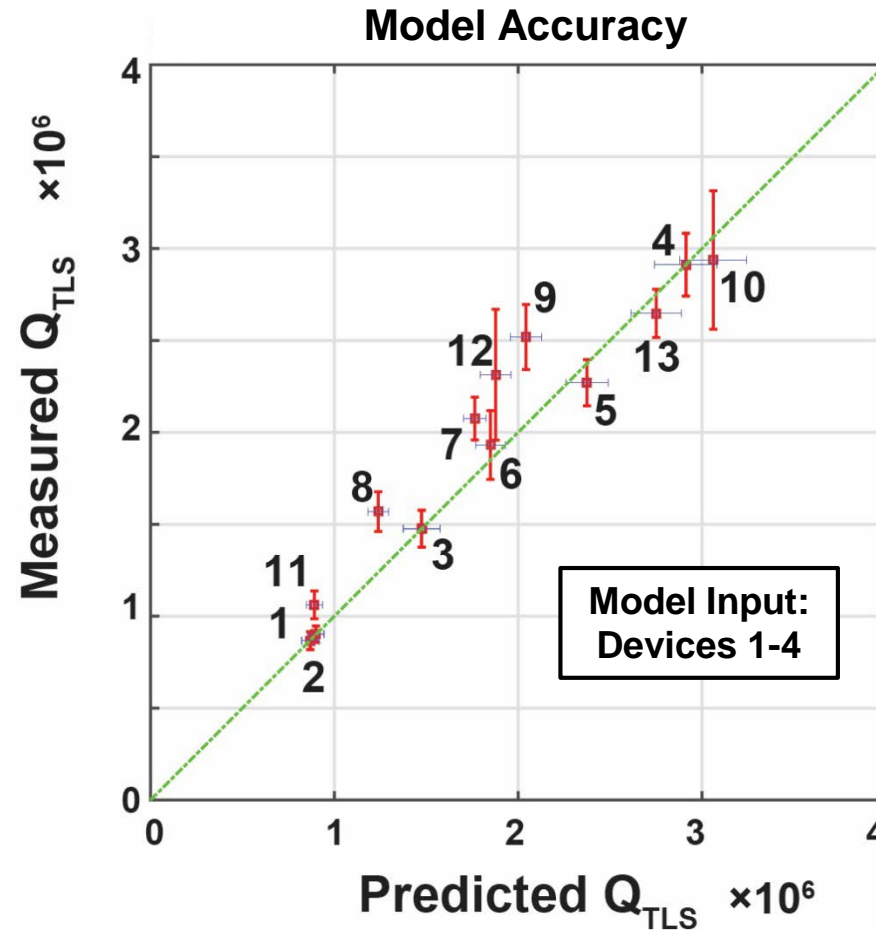
$$t_{MA} = 2 \text{ nm}, \epsilon_{MA} = 10\epsilon_0$$

Isotropically trenched geometries: unique estimation of X_{MS} , X_{SA} , X_{MA} , X_{Si}



Verification and Loss Contributions

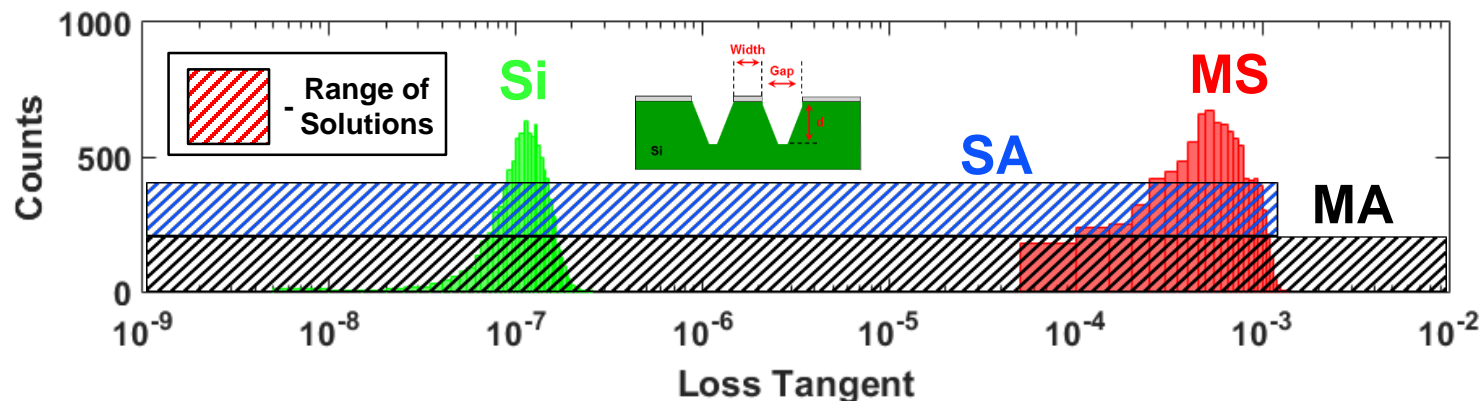
- **Model verification:**
“Training set” predicts Q_{TLS} ’s
for range of participations
- Can now determine loss for
each interface
- **Question:** What is the ‘bad’
interface?
- **Answer:** For most ‘typical’
device (#12), SA is largest
contribution



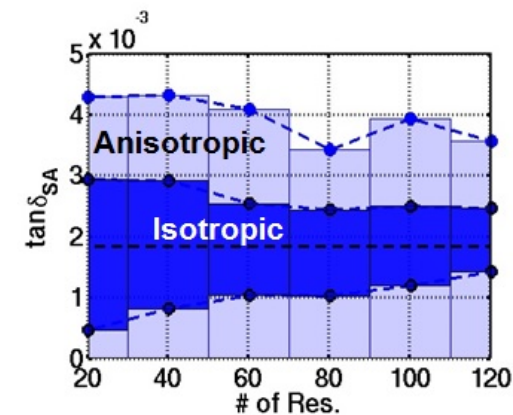
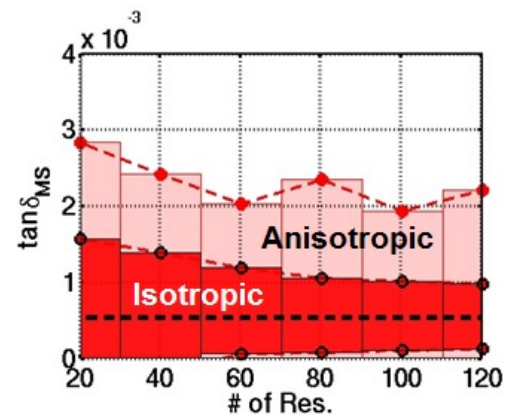


Anisotropic vs. Isotropic Trenching

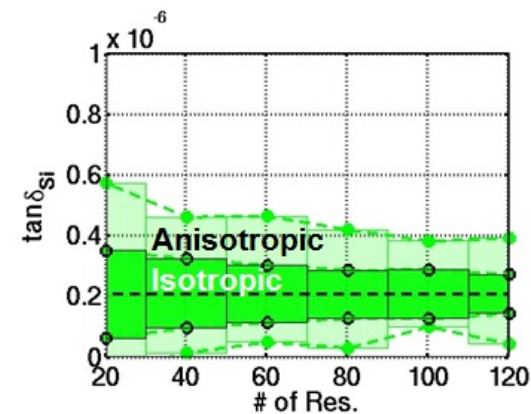
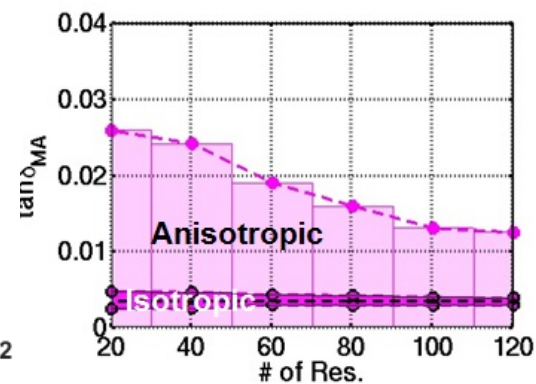
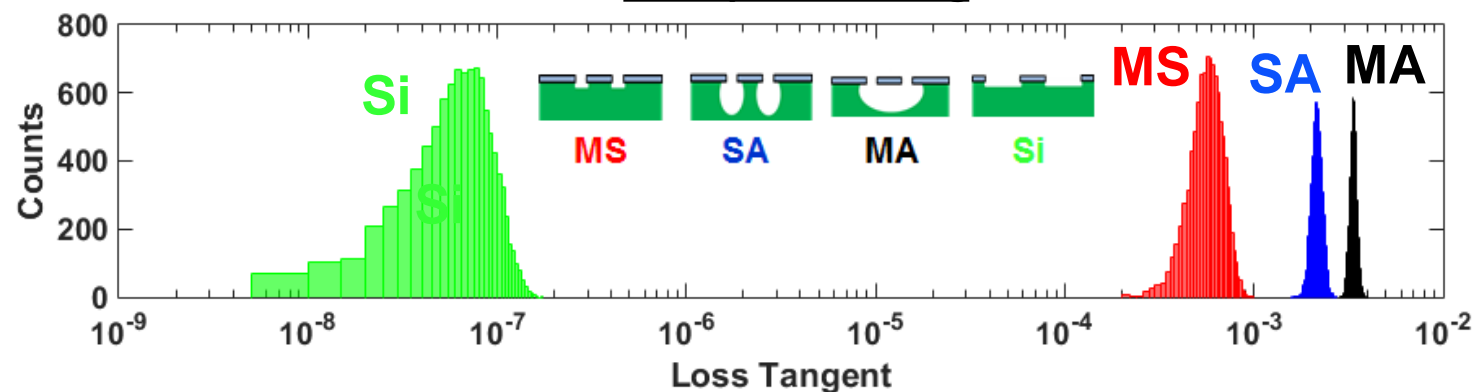
Anisotropic Trenching



Surface Loss Extraction - Simulated Experiment



Isotropic Trenching

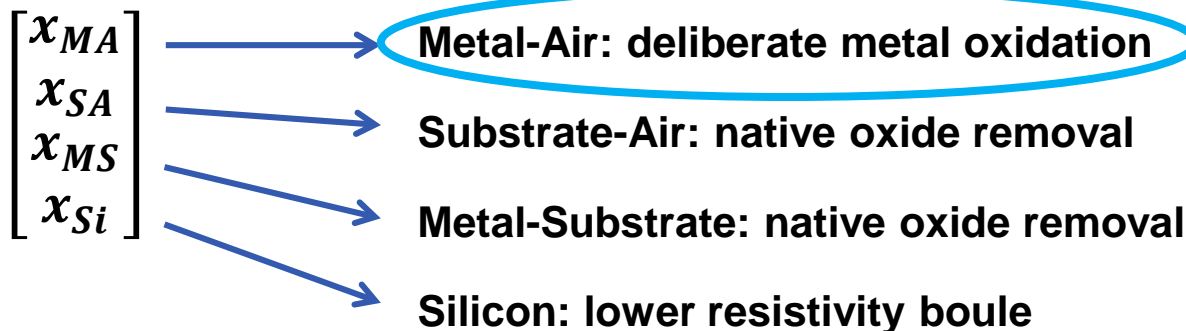


**Isotropic trench geometry improves accuracy
and/or reduces measurement resource requirements**



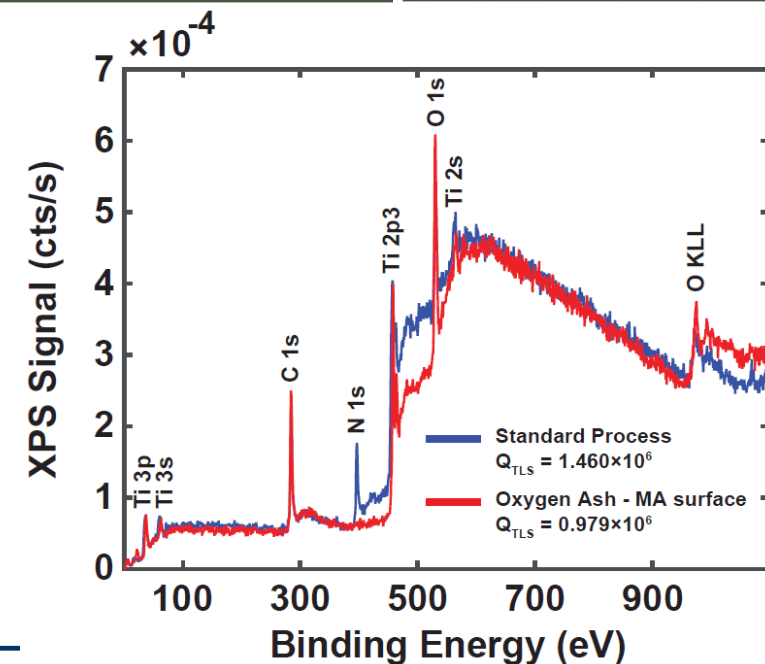
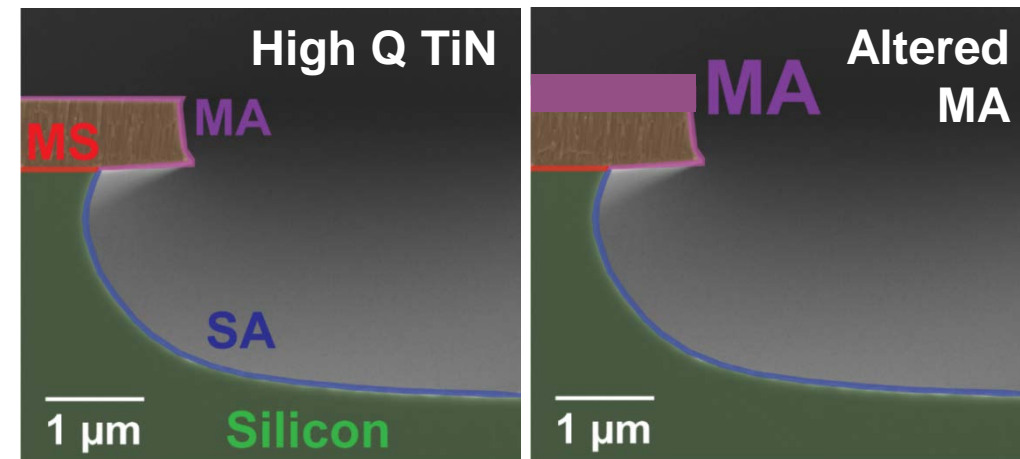
Application/Verification: Surface Modification

Examples of Deliberate Process Changes



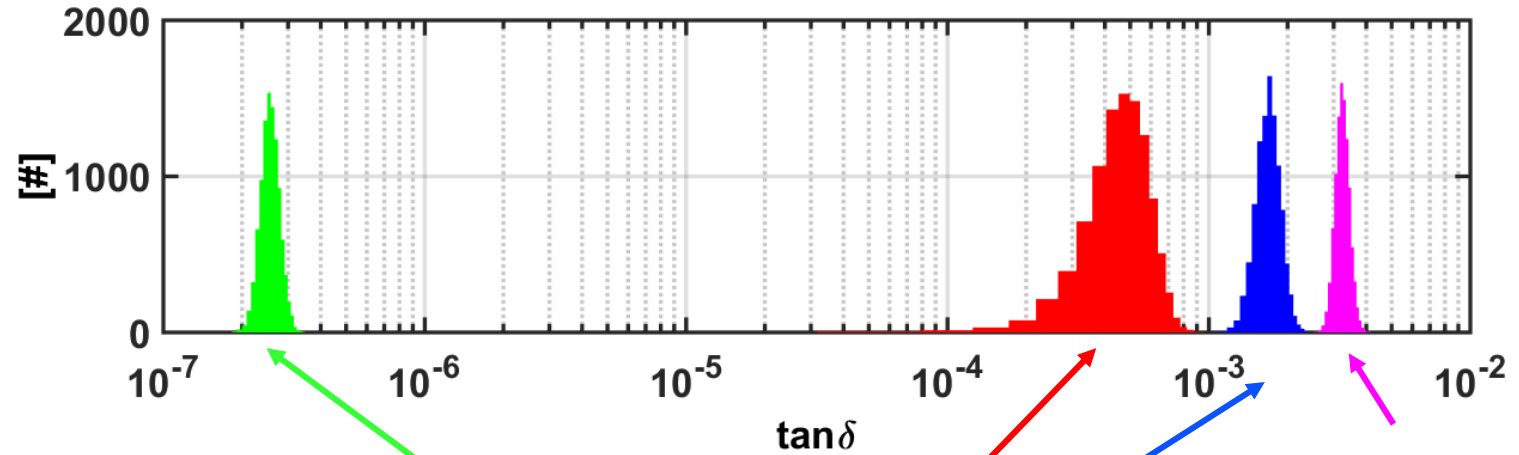
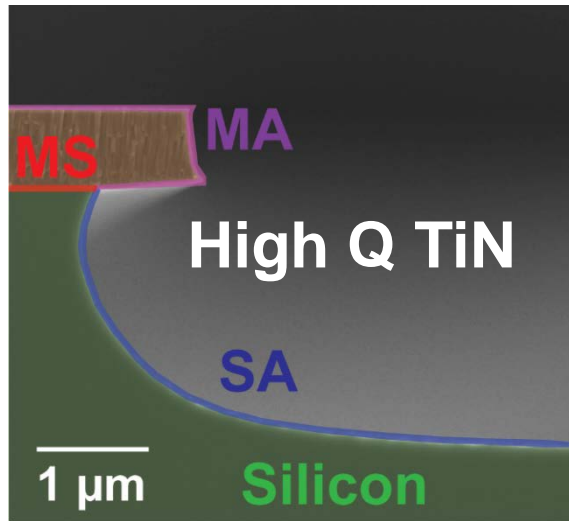
Dielectric Region	High Q TiN (before)	Modified MA TiN (after)
Si	High resistivity	High resistivity
MS	Pre-deposition clean Sputtered TiN	Pre-deposition clean Sputtered TiN
MA	Plasma etch	Additional O₂-based plasma ash Plasma etch
MA, SA	Plasma etch Plasma ash/PR strip Wet PR strip	Plasma etch Plasma ash/PR strip Wet PR strip

Introduce deliberate fabrication change to ONE region to observe effect on loss factor

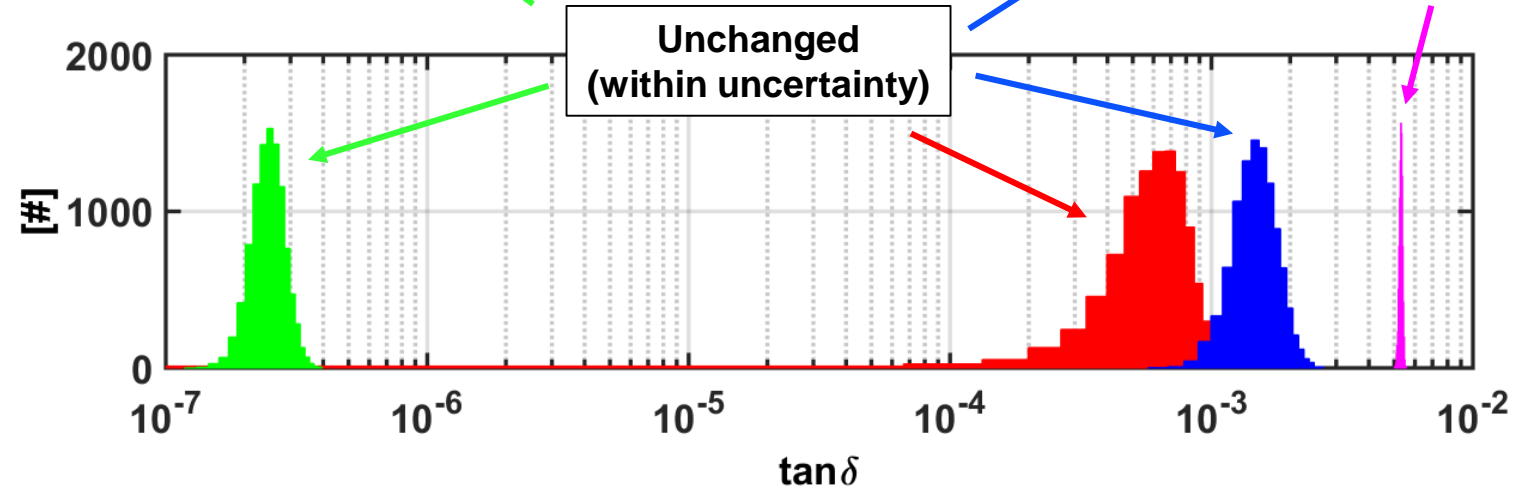
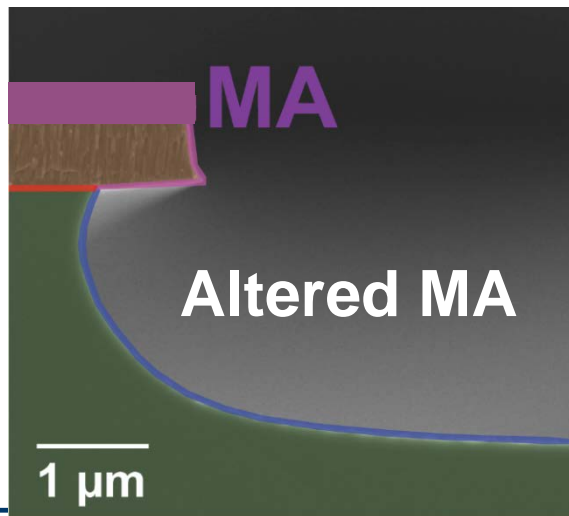




Application/Verification: Surface Modification



~60% increase in MA



ONLY changed MA → ONLY saw x_{MA} change



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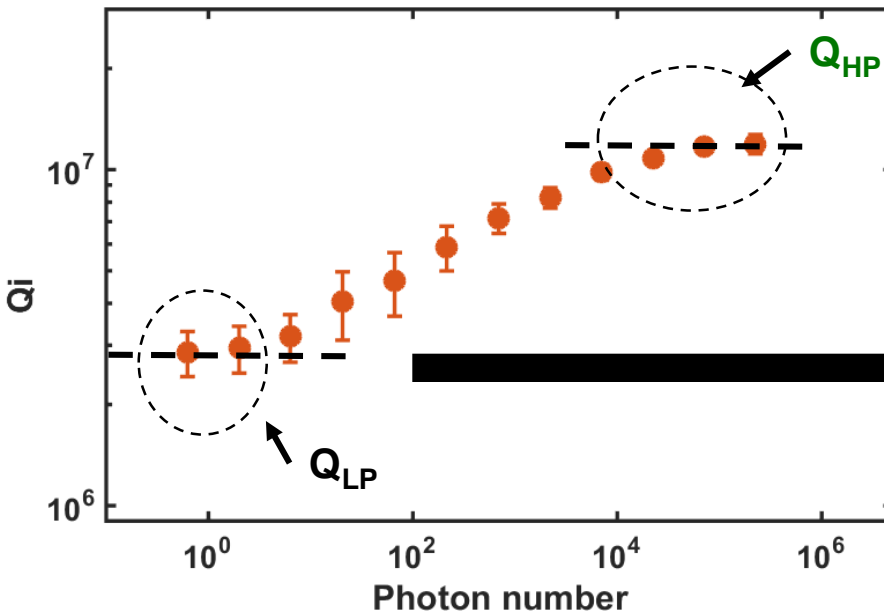


Resonator Background Losses

Q_{LP} : Power-Dependent (TLS) & Power-Independent Mechanisms

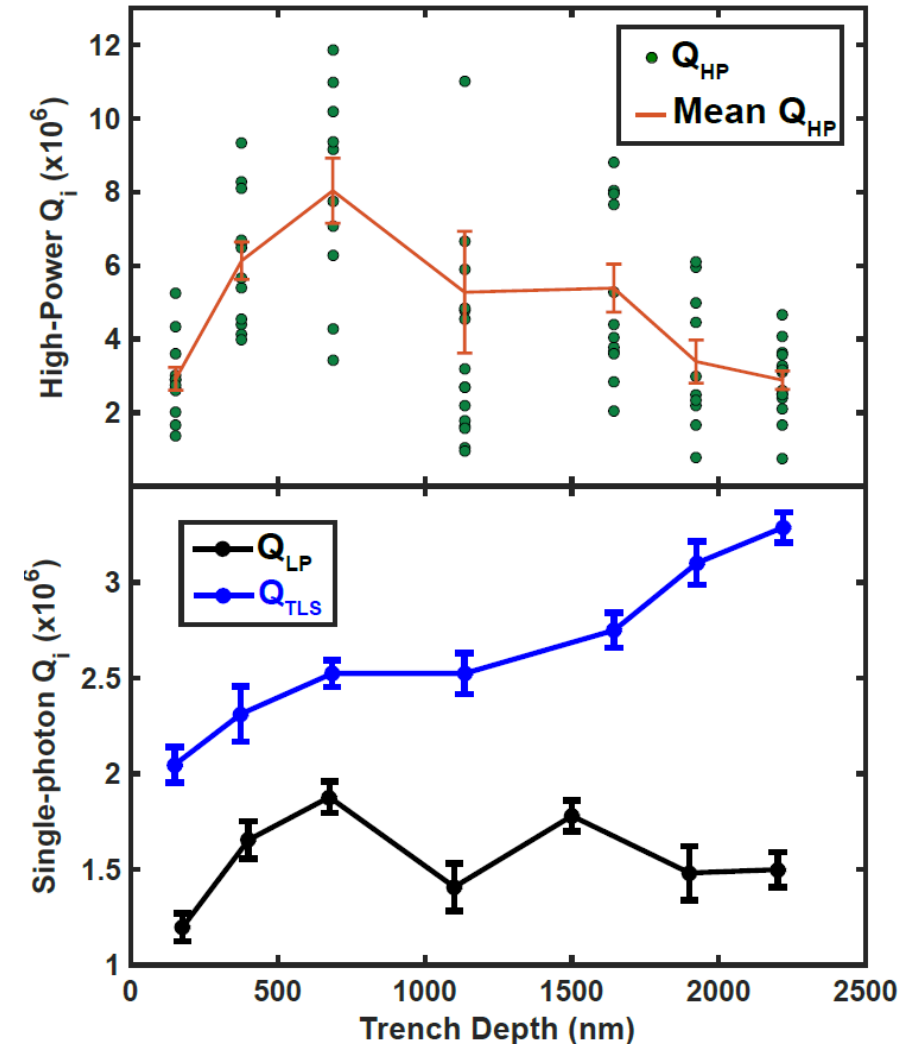
Q_{HP} : Power-Independent Losses
e.g., vortices, quasiparticles,
radiation/packaging, ...

Q vs. Photon Number



$$1/Q_{TLS} = 1/Q_{LP} - 1/Q_{HP}$$

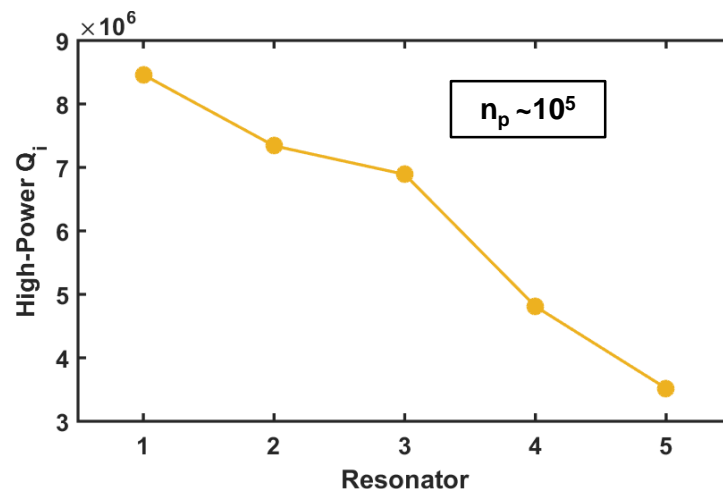
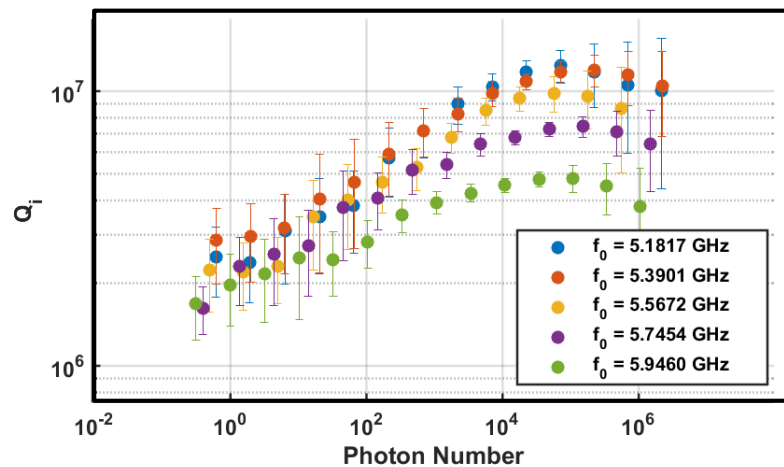
Q vs. Trench Depth



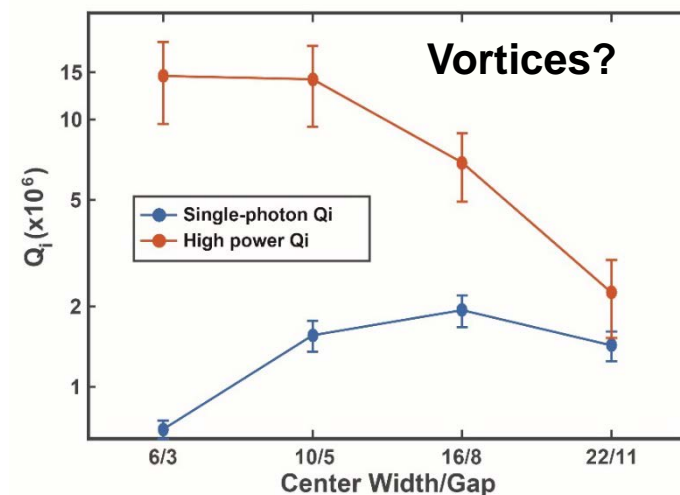


Properties of Background Losses

Clue #1: Frequency dependence



Clue #2: Geometric dependence



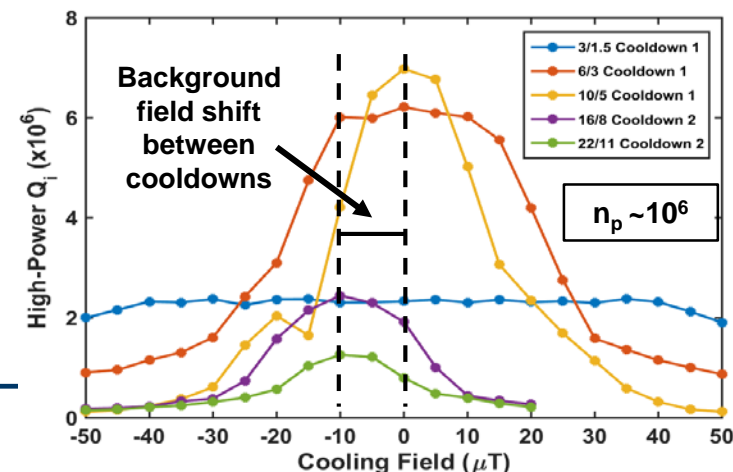
Strong frequency dependence \rightarrow package mode?

...none visible in transmission spectrum

What mechanism explains “background” losses?

$$1/Q_{\text{TLS}} = 1/Q_{\text{LP}} - 1/Q_{\text{HP}}$$

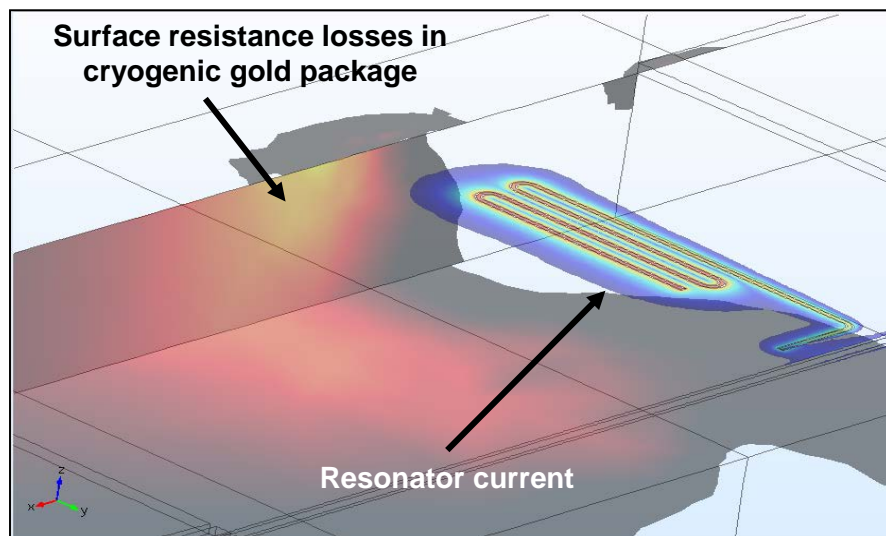
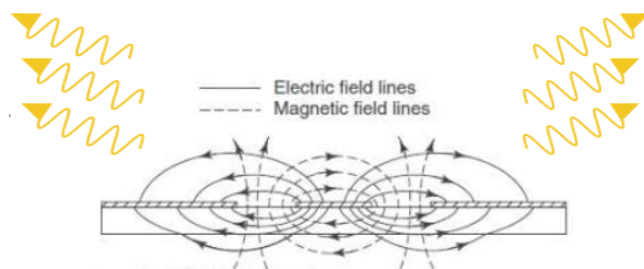
...too small of a contribution



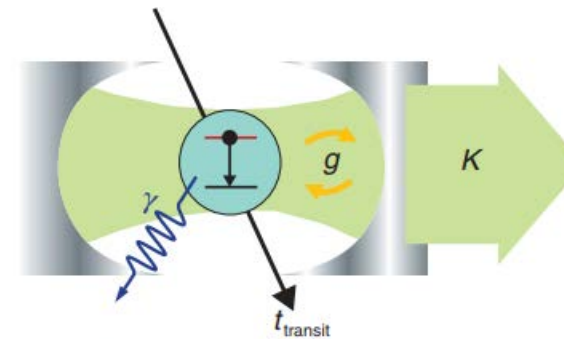


Coupling to Device Packaging

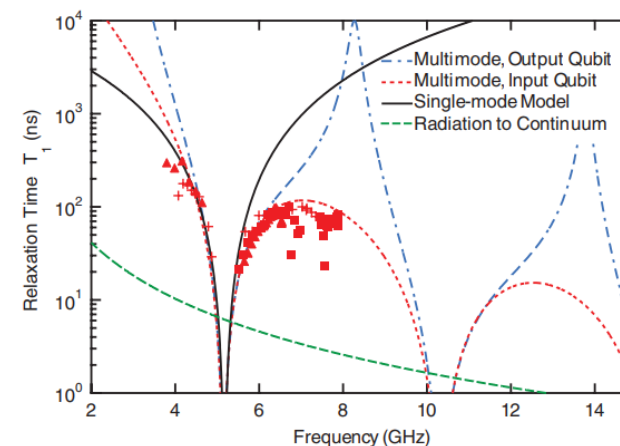
Resistive Metal Losses



Purcell Decay



$$\hat{H}_{JC} = \frac{1}{2} \hbar \omega \hat{\sigma}_z + \hbar \omega_0 \hat{a}^\dagger \hat{a} + \hbar g (\hat{\sigma}_+ \hat{a} + \hat{\sigma}_- \hat{a}^\dagger)$$



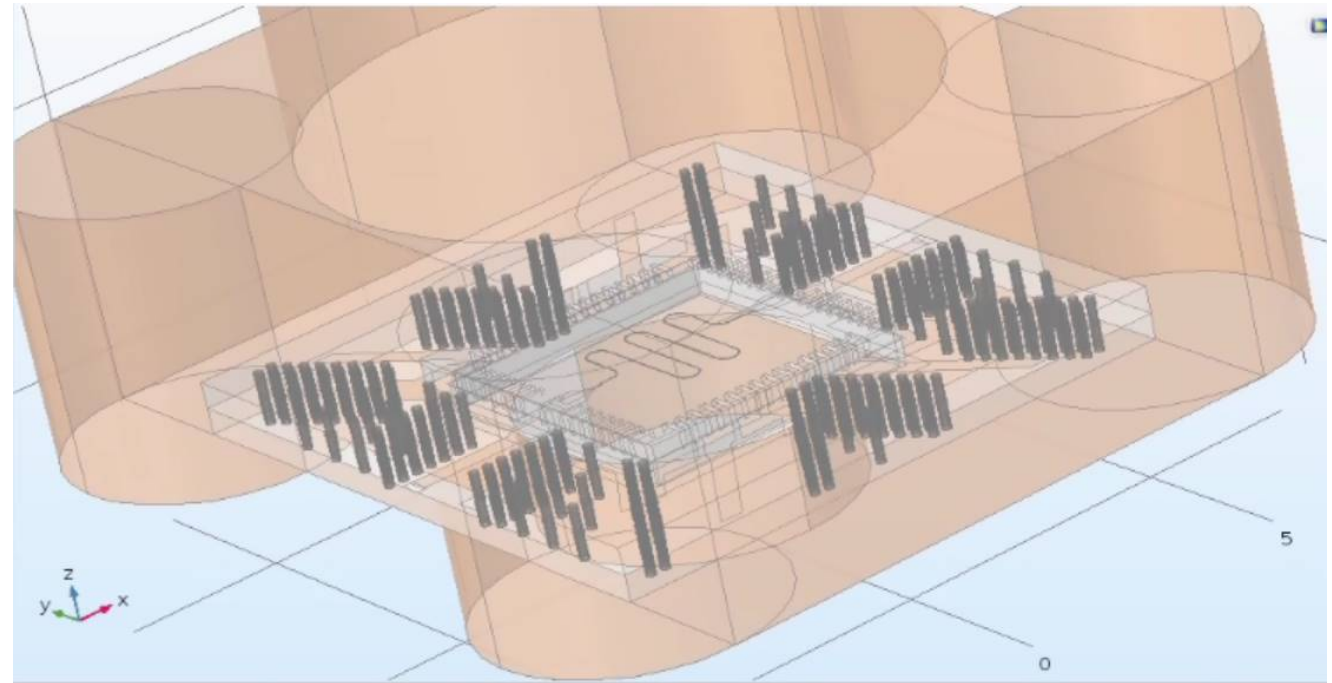
Houck, et al., PRL, 2008



EM Package Modeling

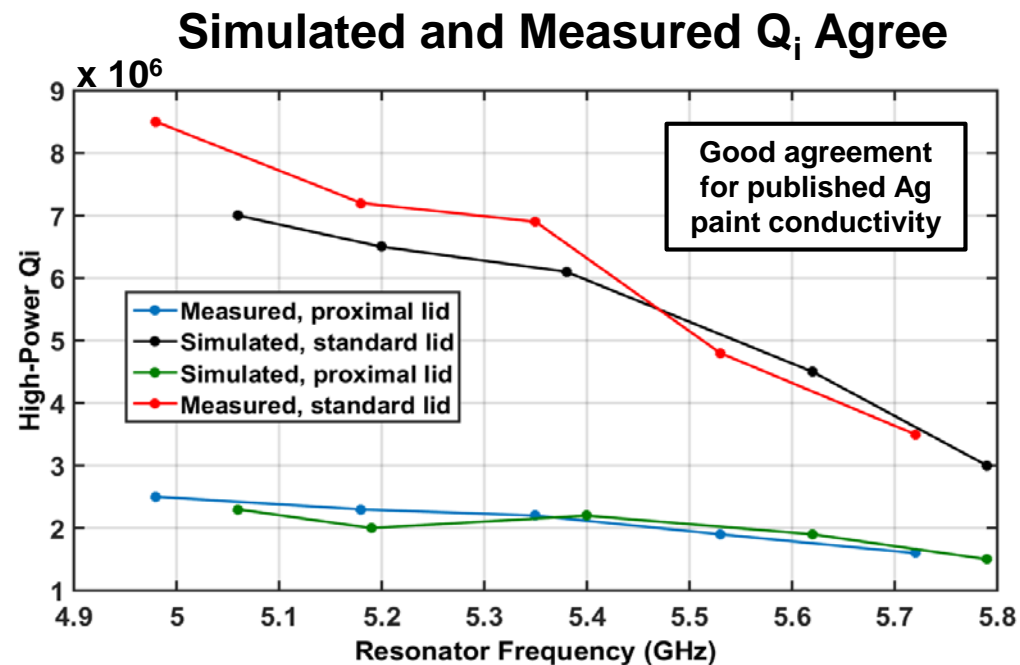
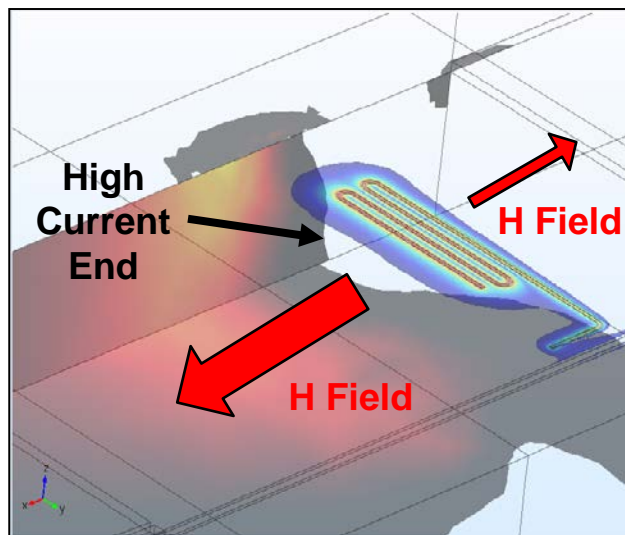
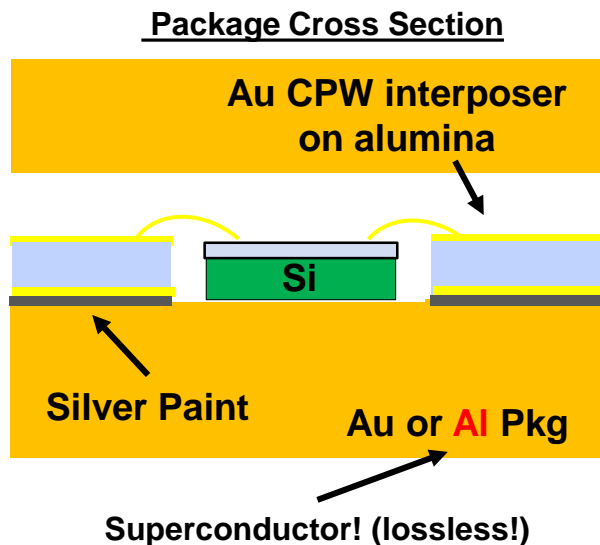
- **Goals: identify...**
 - Package mode spectrum
 - Package mode field profile
 - Resistive metallic losses
 - Dielectric losses
- **COMSOL: include “everything”**
 - Resonators, wirebonds, interposer dielectrics, vias, silicon chip, resistive metals,
- **Match simulation and measurement**
 - Broadband transmission spectrum
 - Fit narrowband resonator Q_i

Standard Qubit Package, Interposer, and Chip



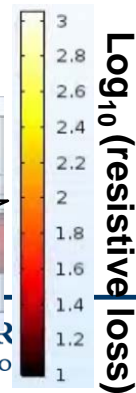
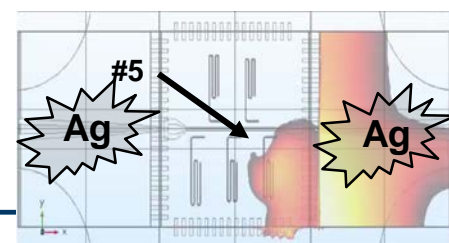
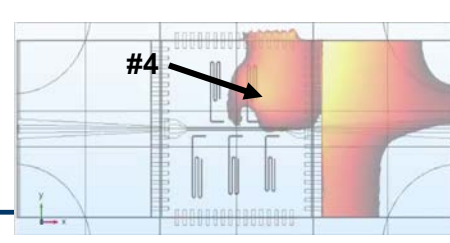
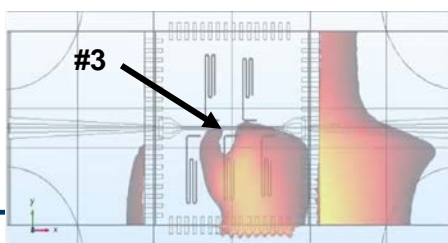
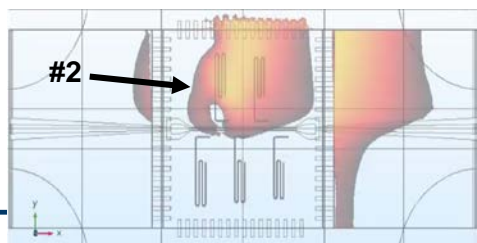


Packaging-induced Losses



Culprit: far away (~ 1-5 mm) lossy adhesives

Increasing frequency, increasing resistive losses at interposer AND side resonator is shorted (high current)

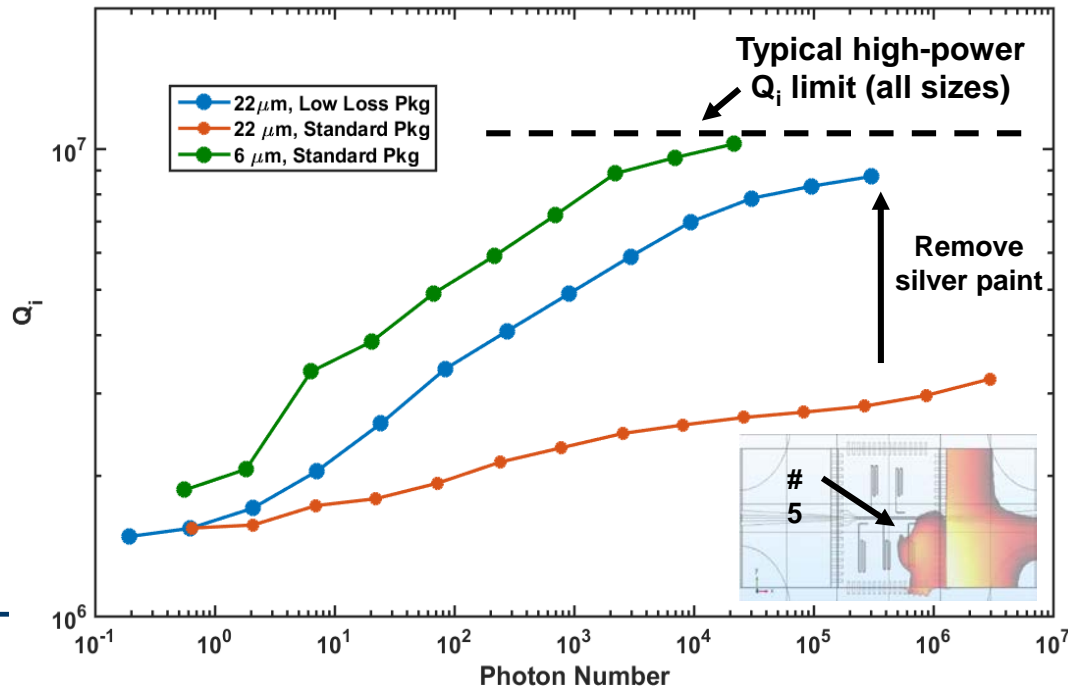
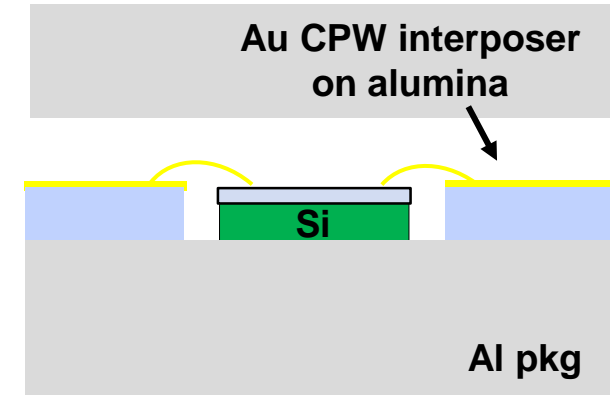




Low-Loss Resonator Packaging

- **Solution**: Remove as much lossy material as possible (no matter how far from chip!)
- **Confirm**: Use wide trace resonators (largest mode volume \rightarrow most sensitive to package losses)

Al Package



- 22 μm high-power Q_i improved from 1-3M to $\sim 10\text{M}$
- No frequency dependence
- High-power Q_i similar to small mode volume devices
- **Outlook**: High single photon Q_i , less variation (better SLE!)



Outline

- **A/B Testing**
- **Characterizing 3D integration**
- **Surface Loss Extraction (SLE)**
- **Sources of device-to-device variability**



So...how useful are resonators?

Pros:

- Easy/Easier to fabrication
- Easy/Easier to measure/automate
- Easy/Easier to simulate (2D, classical)
- Some analytic results exist
- High $Q \rightarrow$ high sensitivity

Optimist's outlook: Resonators are useful tool for characterizing the properties of the enabling technologies for superconducting quantum circuits.

Cons:

- Not many 'knobs'
- May not address specific questions
- Extra fab steps for qubit caps
- Variability/fluctuations
- Too reductionist/worth the effort?

Pessimist's outlook: Resonators are too blunt and unwieldy of a tool to meaningfully assess the properties of the enabling technologies for superconducting quantum circuits.



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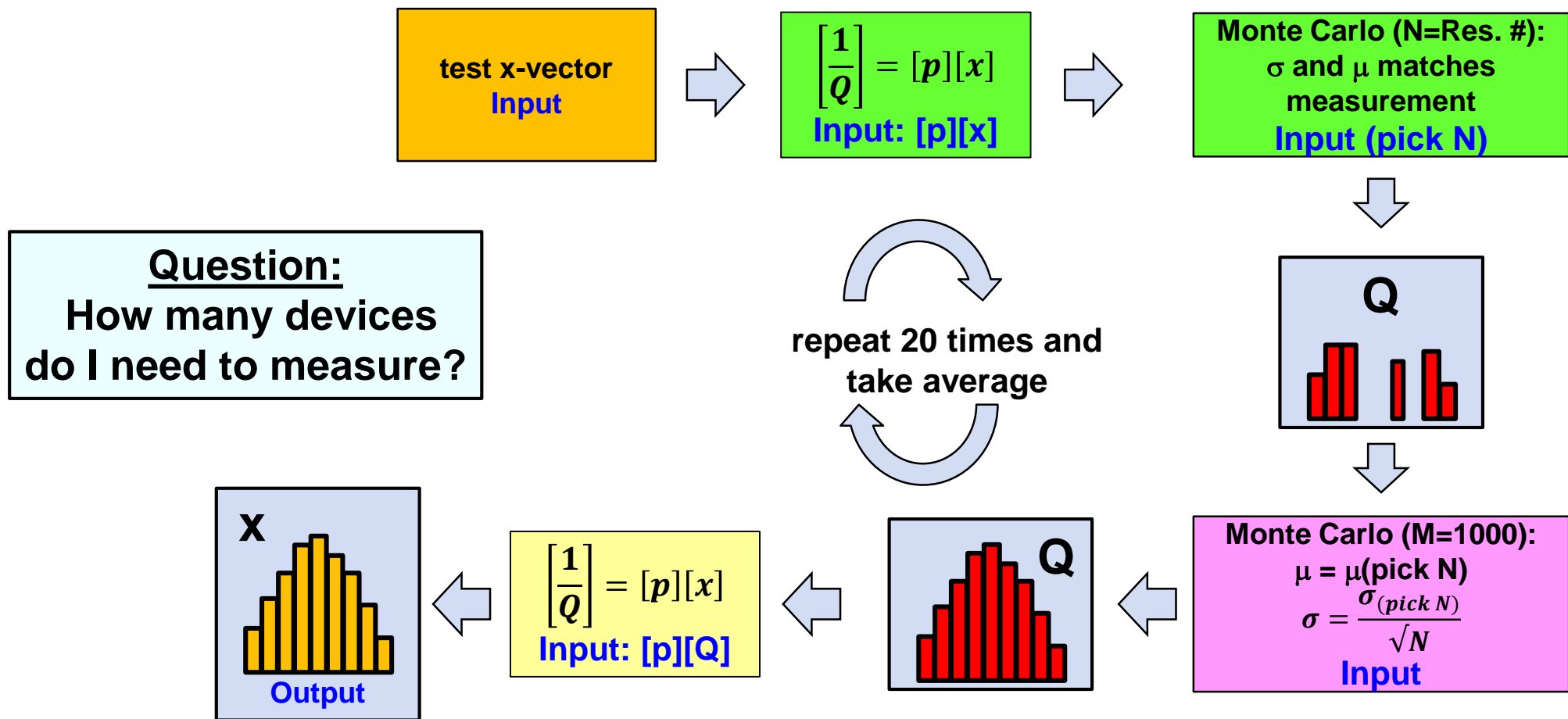




Backup



Estimating Measurement Accuracy



“Simulated Experiment”: estimation of extraction accuracy