具有 0.5V 超低输入电压的 TPS61022 8A 升压转换器

1 特性

- 输入电压范围：0.5V 至 5.5V
- 启动时的最小输入电压为 1.8V
- 输出电压设置范围：2.2V 至 5.5V
- 两个 12mΩ (LS)/18mΩ (HS) 金属氧化物半导体场效应晶体管 (MOSFET)
- 8A 谷值开关电流限制
- V_{IN} = 3.6V、V_{OUT} = 5V 且 I_{OUT} = 3A 时效率为 94.7%
- V_{IN} > 1.5V 时开关频率为 1MHz，V_{IN} < 1V 时开关频率为 0.6MHz
- 在 –40°C 至 +125°C 温度范围内，基准电压精度为 ±2.5%
- 轻负载运行时引脚可选自动 PFM 工作模式或强制 PWM 工作模式
- V_{IN} > V_{OUT} 时切换为直通模式
- 在关断期间真正断开输入域输出之间的连接
- 输出过压和热关断保护
- 输出短路保护
- 2mm × 2mm VQFN 7 引脚封装

2 应用

- USB 端口
- 备用超级电容器
- GPRS 电源

3 说明

TPS61022 可以为由多种电池和超级电容器供电的便携式设备和物联网设备提供电源解决方案。在整个温度范围内，TPS61022 的谷值开关电流限制最小值为 6.5A。在 0.5V 至 5.5V 的宽输入电压范围内，TPS61022 支持超级电容器备用电源 应用，这可能导致超级电容器深度放电。

当输入电压高于 1.5V 时，TPS61022的工作频率为 1MHz。当输入电压低于 1.5V 甚至降至 1V 时，开关频率逐渐降至 0.6MHz。在轻负载条件下，MODE 引脚将 TPS61022 工作模式设定为省电模式或强制 PWM 模式。在轻负载条件下，TPS61022 仅消耗 V_{OUT} 处的 26μA 静态电流。关断期间，负载与输入电源完全断开。TPS61022 还具有 5.7V 输出过压保护、输出短路保护和热关断保护。

TPS61022 采用 2mm × 2mm VQFN 封装，最大限度地减少了外部组件的数量，因而拥有非常小巧的解决方案尺寸。

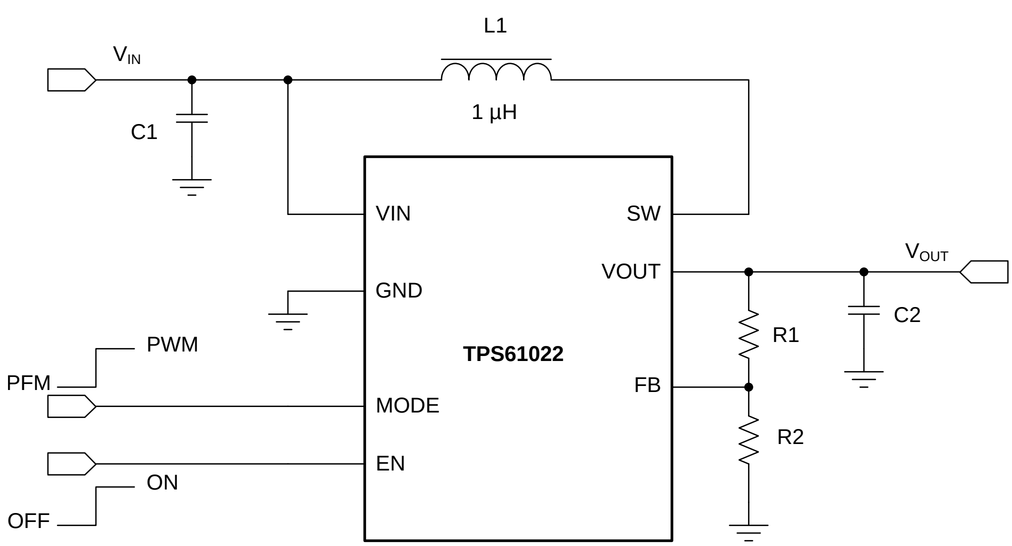
器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS61022	VQFN (7)	2.00mm × 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

ADVANCE INFORMATION

典型应用电路



目录

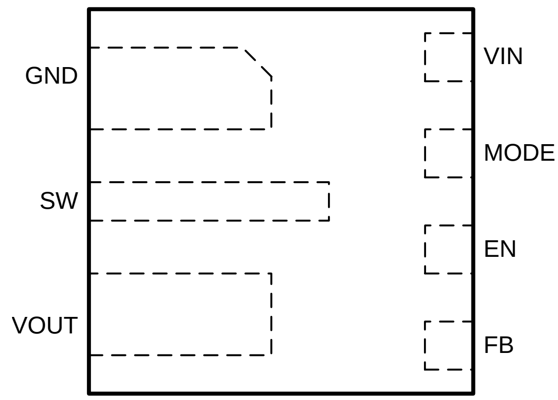
4 修订历史记录

日期	修订版本	说明
2019 年 1 月	*	初始发行版

ADVANCE INFORMATION

5 Pin Configuration and Functions

RWU Package
7-Pin VQFN with Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	GND	PWR	Ground pin of the IC
2	SW	PWR	The switch pin of the converter. It is connected to the drain of the internal low-side power MOSFET and the source of the internal high-side power MOSFET.
3	VOUT	PWR	Boost converter output
4	FB	I	Voltage feedback of adjustable output voltage.
5	EN	I	Enable logic input. Logic high voltage enables the device. Logic low voltage disables the device and turns it into shutdown mode.
6	MODE	I	Operation mode selection in the light load condition. When it is connected to logic high voltage, the device works in forced PWM mode. When it is connected to logic low voltage, the device works in auto PFM mode.
7	VIN	I	IC power supply input

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range at terminals(2)	VIN, EN, FB, MODE, SW, VOUT	–0.3	7	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	Output voltage pre biased < 0.7V before start-up	0.5		4.8	V
		Output voltage pre biased > 0.7V before start-up	0.5		5.5	V
V_{OUT}	Output voltage setting range		2.2		5.5	V
L	Effective inductance range		0.33	1.0	2.9	µH
C_{IN}	Effective input capacitance range		4.7	10		µF
C_{OUT}	Effective output capacitance range		10	22	1000	µF
T_J	Operating junction temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS61022 RWU (VQFN) - 7 PINS Standard	TPS61022 RWU (VQFN) - 7 PINS EVM(2)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.2	50.9	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	70.2	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.1	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.6	1.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	36.7	20.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Measured on TPS61022EVM-034, 4-layer, 2oz copper 58mm×46mm PCB.

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6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 3.6 V and V_{OUT} = 5.0 V. Typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		0.5		5.5	V
V_{IN_UVLO}	Under-voltage lockout threshold	V_{IN} rising		1.7	1.8	V
		V_{IN} falling		0.4	0.5	V
I_Q	Quiescent current into VIN pin	IC enabled, No load, No switching V_{IN} = 1.8 V to 5.5 V, V_{FB} = V_{REF} + 0.1 V, T_J up to 85°C			3.0	µA
	Quiescent current into VOUT pin	IC enabled, No load, No switching V_{OUT} = 2.2 V to 5.5 V, V_{FB} = V_{REF} + 0.1 V, T_J up to 85°C		27	32	µA
I_{SD}	Shutdown current into VIN and SW pin	IC disabled, V_{IN} = 1.8 V to 5.5 V, T_J = 25°C		0.25	0.6	µA
		IC disabled, V_{IN} = 1.8 V to 5.5 V, T_J up to 85°C		0.25	3.0	µA
OUTPUT						
V_{OUT}	Output voltage setting range		2.2		5.5	V
V_{REF}	Reference voltage at the FB pin	PWM mode	585	600	615	mV
		PFM mode	590	606		mV
V_{OVP}	Output over-voltage protection threshold	V_{OUT} rising	5.5	5.7	6.0	V
V_{OVP_HYS}	Over-voltage protection hysteresis			0.1		V
I_{FB_LKG}	Leakage current at FB pin				20	nA
I_{VOUT_LKG}	Leakage current into VOUT pin	IC disabled, V_{IN} = 0 V, V_{SW} = 0 V, V_{OUT} = 5.5 V,T_J up to 85°C		1	3	µA
t_{SS}	Soft startup time	From active EN to VOUT regulation. V_{IN} = 2.5 V, V_{OUT} = 5.0 V, C_{OUT_EFF} = 30µF, I_{OUT} = 0		700		µs
POWER SWITCH						
$R_{DS(on)}$	High-side MOSFET on resistance	V_{OUT} = 5.0 V		18		mΩ
	Low-side MOSFET on resistance	V_{OUT} = 5.0 V		12		mΩ
f_{SW}	Switching frequency	V_{IN} = 3.6 V, V_{OUT} = 5.0 V, PWM mode		1.0		MHz
		V_{IN} = 1.0 V, V_{OUT} = 5.0 V, PWM mode		0.6		MHz
t_{OFF_min}	Minimum off time			80	120	ns
I_{LIM_SW}	Valley current limit	V_{IN} = 3.6 V, V_{OUT} = 5.0 V	6.5	8	10	A
I_{LIM_CHG}	Pre-charge current	V_{IN} = 1.8 - 4.8 V, V_{OUT} < 0.4 V	400	700		mA
$I_{LIM\_CHG\_max}$	Maximum pre-charge current	V_{IN} = 2.4 V, V_{OUT} > 0.4 V	2	2.4		A
LOGIC INTERFACE						
V_{EN_H}	EN logic high threshold	V_{IN} > 1.8 V or V_{OUT} > 2.2 V			1.2	V
V_{EN_L}	EN logic low threshold	V_{IN} > 1.8 V or V_{OUT} > 2.2 V	0.35	0.42	0.45	
V_{MODE_H}	MODE logic high threshold	V_{IN} > 1.8 V or V_{OUT} > 2.2 V			1.2	V
V_{MODE_L}	MODE logic low threshold	V_{IN} > 1.8 V or V_{OUT} > 2.2 V	0.4			
PROTECTION						
T_{SD}	Thermal shutdown threshold	T_J rising		150		°C
T_{SD_HYS}	Thermal shutdown hysteresis	T_J falling below T_{SD}		20		°C

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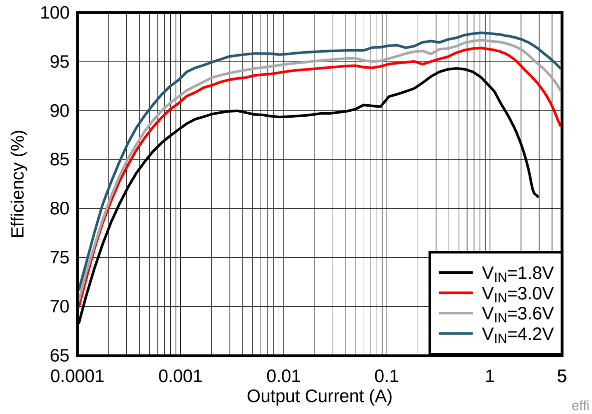
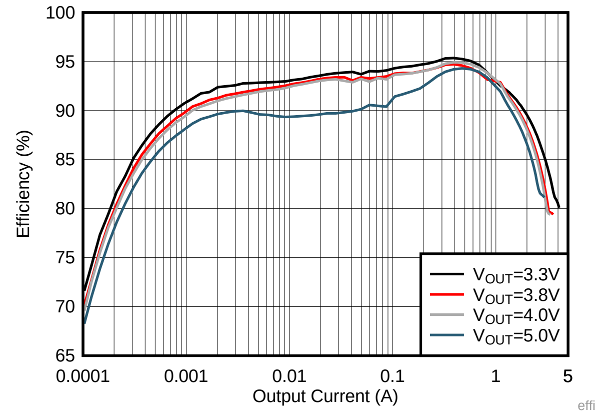
6.6 Typical Characteristics

V_{IN} = 3.6 V, V_{OUT} = 5 V, T_J = 25°C, unless otherwise noted



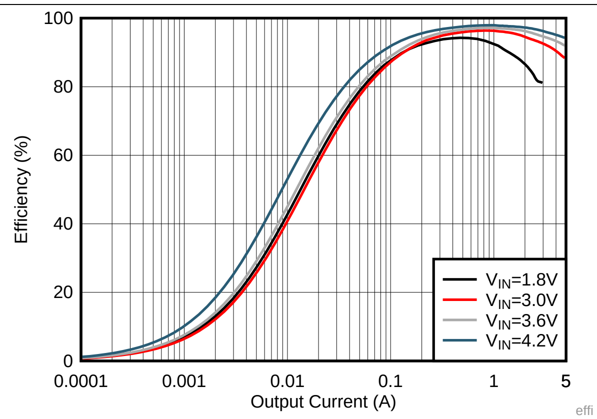
V_{IN} = 1.8 V, 3 V, 3.6 V, 4.2 V; V_{OUT} = 5 V

图 1. Load Efficiency With Different Input in Auto PFM



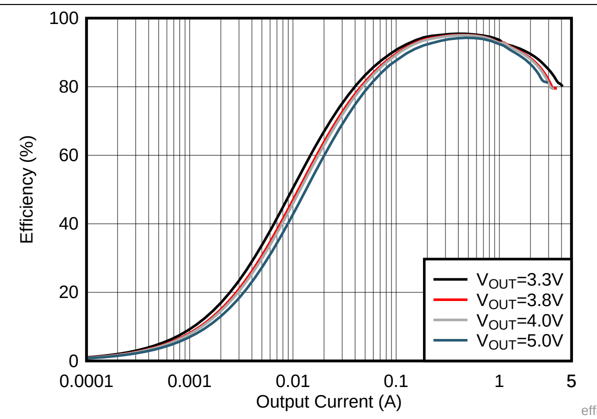
V_{IN} = 1.8 V; V_{OUT} = 3.3 V, 3.8 V, 4 V, 5 V

图 2. Load Efficiency With Different Output in Auto PFM



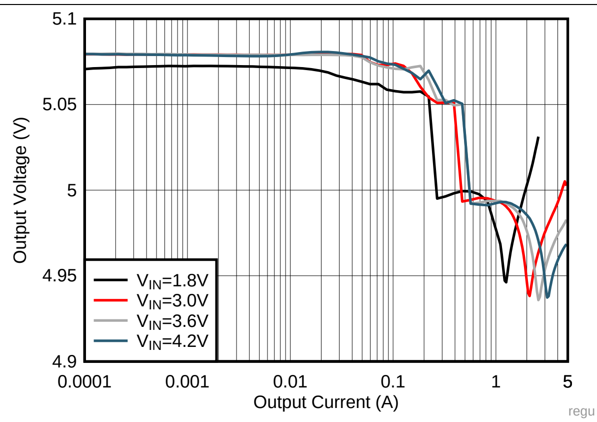
V_{IN} = 1.8 V, 3 V, 3.6 V, 4.2 V; V_{OUT} = 5 V

图 3. Load Efficiency With Different Input in Forced PWM



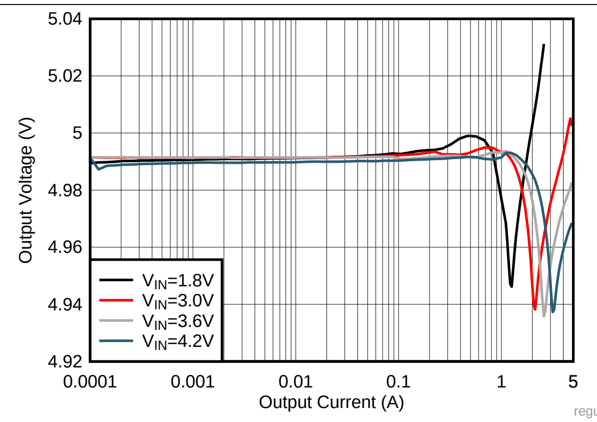
V_{IN} = 1.8 V; V_{OUT} = 3.3 V, 3.8 V, 4 V, 5 V

图 4. Load Efficiency With Different Output in Forced PWM



V_{IN} = 1.8 V, 3 V, 3.6 V, 4.2 V; V_{OUT} = 5 V

图 5. Load Regulation in Auto PFM

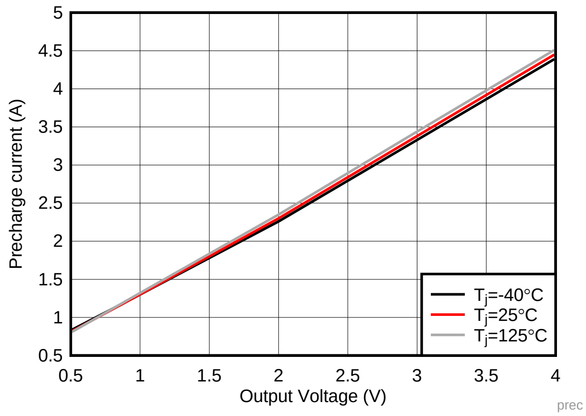


V_{IN} = 1.8 V, 3 V, 3.6 V, 4.2 V; V_{OUT} = 5 V

图 6. Load Regulation in Forced PWM

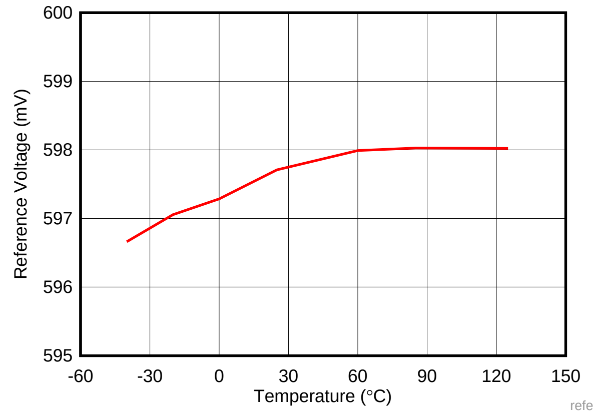
Typical Characteristics (接下页)

V_{IN} = 3.6 V, V_{OUT} = 5 V, T_J = 25°C, unless otherwise noted



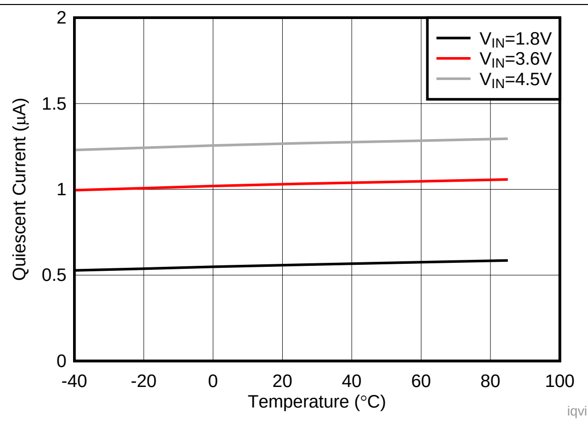
V_{IN} = 5 V; V_{OUT} = 0.5 V to 4 V

图 7. Pre-charge Current vs Output Voltage



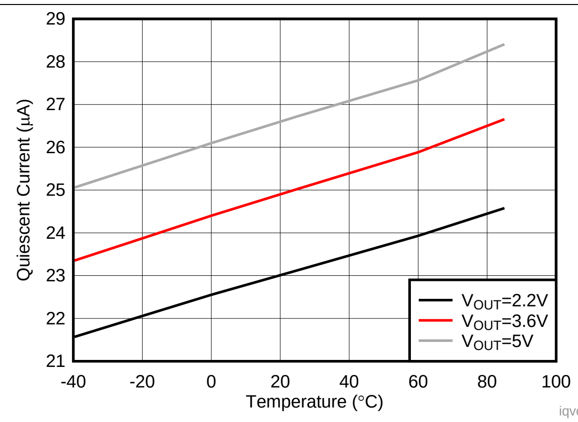
V_{IN} = 3.6 V; V_{OUT} = 5 V, T_J = –40°C to +125°C

图 8. Reference Voltage vs Temperature



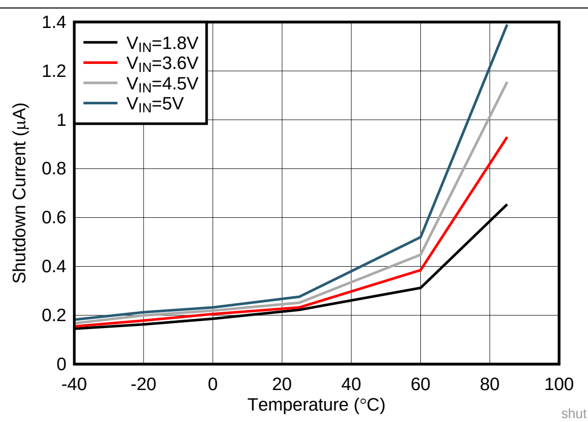
V_{IN} = 1.8 V, 3.6 V 4.5 V; V_{OUT} = 5 V, T_J = –40°C to +85°C, No switching

图 9. Quiescent Current into VIN vs Temperature



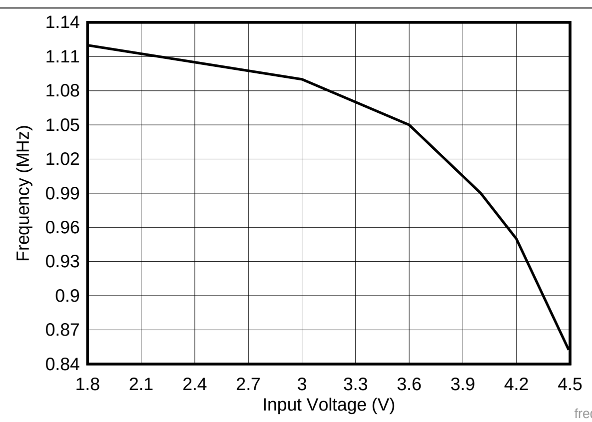
V_{IN} = 1.8 V; V_{OUT} = 2.2 V, 3.6 V, 5 V, T_J = –40°C to +85°C, No switching

图 10. Quiescent Current into VOUT vs Temperature



V_{IN} = V_{SW} = 1.8 V, 3.6 V, 4.5 V, 5 V; T_J = –40°C to +85°C

图 11. Shutdown Current vs Temperature



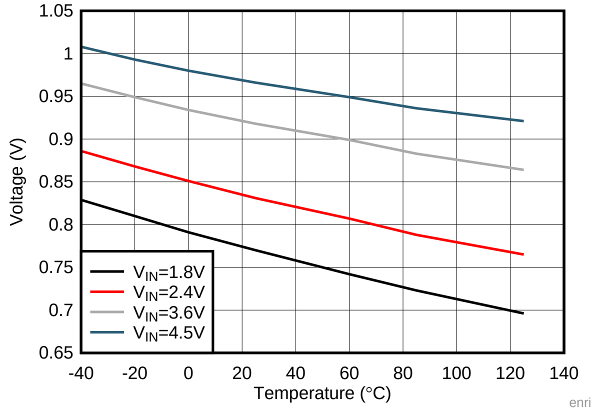
V_{IN} = 1.8 V to 4.5 V; V_{OUT} = 5 V

图 12. Switching Frequency vs Input Voltage

ADVANCE INFORMATION

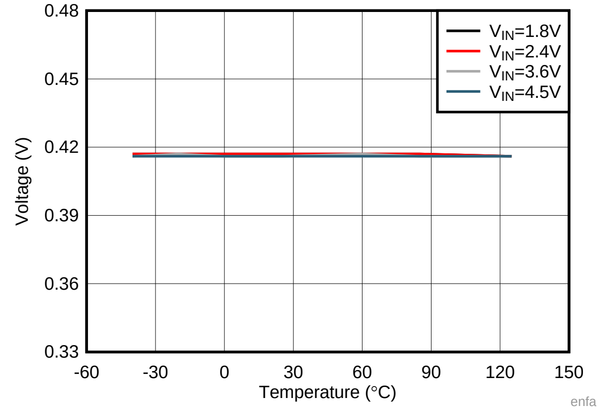
Typical Characteristics (接下页)

V_{IN} = 3.6 V, V_{OUT} = 5 V, T_J = 25°C, unless otherwise noted



V_{IN} = 1.8 V, 2.4 V, 3.6 V, 4.5 V; V_{OUT} = 5 V; T_J = –40°C to +125°C

图 13. EN Rising Threshold vs Temperature



V_{IN} = 1.8 V, 2.4 V, 3.6 V, 4.5 V; V_{OUT} = 5 V; T_J = –40°C to +125°C

图 14. EN Falling Threshold vs Temperature

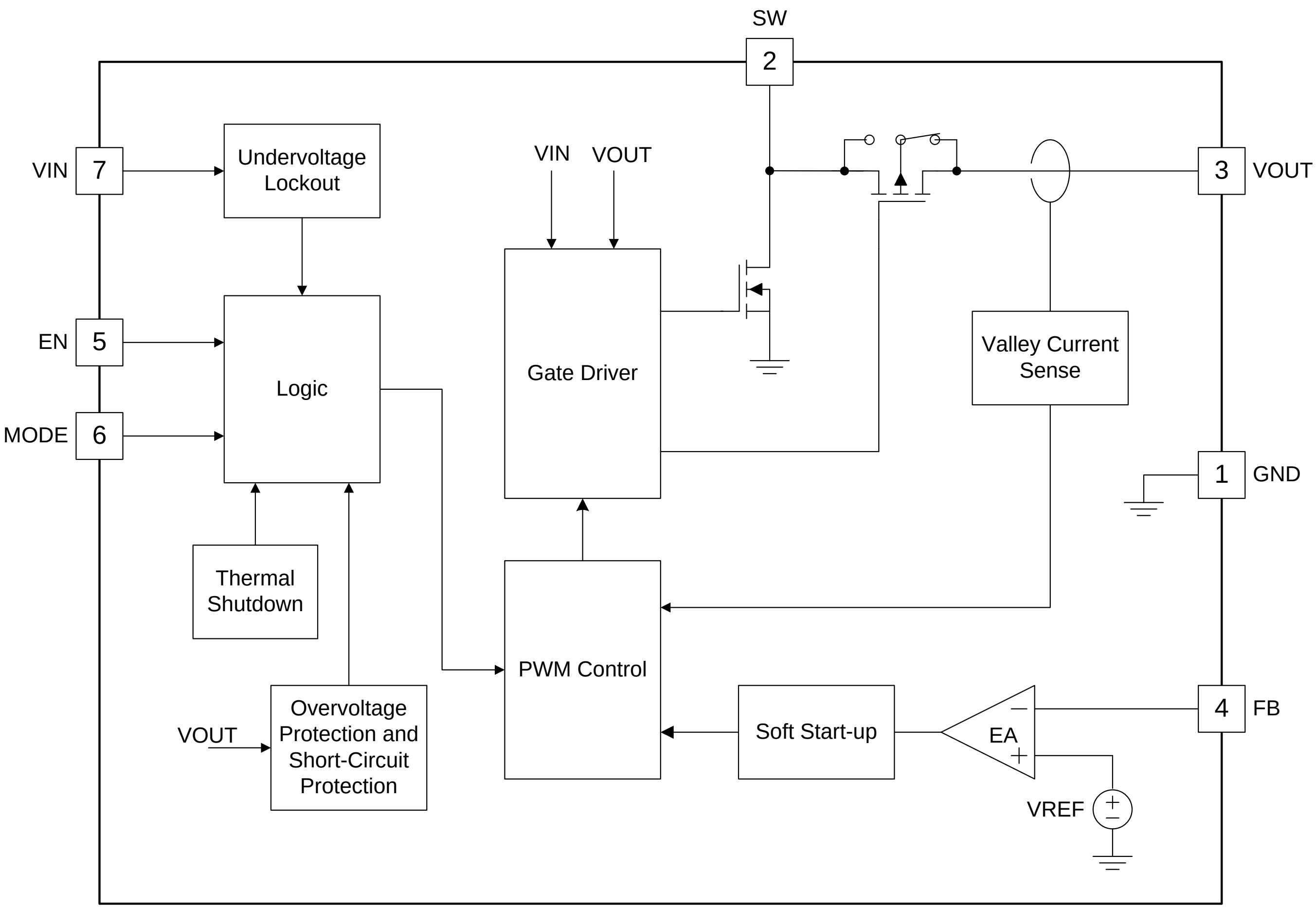
ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The TPS61022 synchronous step-up converter is designed to operate from an input voltage supply range between 0.5 V and 5.5 V with 6.5-A (minimum) valley switch current limit. The TPS61022 typically operates at a quasi-constant frequency pulse width modulation (PWM) at moderate to heavy load currents. The switching frequency is 1 MHz when the input voltage is above 1.5 V. The switching frequency reduces down to 0.6 MHz gradually when the input voltage goes down from 1.5 V to 1 V and keeps at 0.6 MHz when the input voltage is below 1 V. The MODE pin sets the TPS61022 converter operating in power-save mode with pulse frequency modulation (PFM) or forced PWM mode in light load conditions. During PWM operation, the converter uses adaptive constant on-time valley current mode control scheme to achieve excellent line regulation and load regulation and allows the use of a small inductor and ceramic capacitors. Internal loop compensation simplifies the design process while minimizing the number of external components.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Undervoltage Lockout

The TPS61022 has a built-in undervoltage lockout (UVLO) circuit to ensure the device working properly. When the input voltage is above the UVLO rising threshold of 1.8 V, the TPS61022 can be enabled to boost the output voltage. After the TPS61022 starts up and the output voltage is above 2.2 V, the TPS61022 works with input voltage as low as 0.5 V.

7.3.2 Enable and Soft Start

When the input voltage is above the UVLO rising threshold and the EN pin is pulled to a voltage above 1.2 V, the TPS61022 is enabled and starts up. At the beginning, the TPS61022 charges the output capacitors with a current of about 700 mA when the output voltage is below 0.4 V. When the output voltage is charged above 0.4 V, the output current is changed to having output current capability to drive 1-Ω resistance load. After the output voltage reaches the input voltage, the TPS61022 starts switching, and the output voltage ramps up further. The typical start-up time is 700 µs accounting from EN high to output reaching target voltage for the application with input voltage is 2.5 V, output voltage is 5 V, output effective capacitance is 30 µF and no load. When the voltage at the EN pin is below 0.4 V, the internal enable comparator turns the device into shutdown mode. In the shutdown mode, the device is entirely turned off. The output is disconnected from input power supply.

7.3.3 Switching Frequency

The TPS61022 switches at a quasi-constant 1-MHz frequency when the input voltage is above 1.5 V. When the input voltage is lower than 1.5 V, the switching frequency is reduced gradually to 0.6 MHz to improve the efficiency and get higher boost ratio. When the input voltage is below 1 V, the switching frequency is fixed at a quasi-constant 0.6 MHz.

7.3.4 Current Limit Operation

The TPS61022 uses a valley current limit sensing scheme. Current limit detection occurs during the off-time by sensing of the voltage drop across the synchronous rectifier.

When the load current is increased such that the inductor current is above the current limit within the whole switching cycle time, the off-time is increased to allow the inductor current to decrease to this threshold before the next on-time begins (so called frequency fold-back mechanism). When the current limit is reached, the output voltage decreases during further load increase.

The maximum continuous output current ($I_{OUT(LC)}$), before entering current limit (CL) operation, can be defined by 公式 1.

$$I_{OUT(CL)} = (1-D) \times \left(I_{LIM} + \frac{1}{2} \Delta I_{L(P-P)} \right)$$

where

- D is the duty cycle
- $\Delta I_{L(P-P)}$ is the inductor ripple current (1)

The duty cycle can be estimated by 公式 2.

$$D = 1 - \frac{V_{IN} \times \eta}{V_{OUT}}$$

where

- V_{OUT} is the output voltage of the boost converter
- V_{IN} is the input voltage of the boost converter
- η is the efficiency of the converter, use 90% for most applications (2)

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Feature Description (接下页)

The peak-to-peak inductor ripple current is calculated by 公式 3.

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times D}{L \times f_{SW}}$$

where

- L is the inductance value of the inductor
- f_{SW} is the switching frequency
- D is the duty cycle
- V_{IN} is the input voltage of the boost converter (3)

7.3.5 Pass-Through Operation

When the input voltage is higher than the setting output voltage, the output voltage is higher than the target regulation voltage. When the output voltage is 101% of the setting target voltage, the TPS61022 stops switching and fully turns on the high-side PMOS FET. The device works in pass-through mode. The output voltage is the input voltage minus the voltage drop across the DCR of the inductor and the $R_{DS(on)}$ of the PMOS FET. When the output voltage drops below the 97% of the setting target voltage as the input voltage declines or the load current increases, the TPS61022 resumes switching again to regulate the output voltage.

7.3.6 Overvoltage Protection

The TPS61022 has an output overvoltage protection (OVP) to protect the device if the external feedback resistor divider is wrongly populated. When the output voltage is above 5.7 V typically, the device stops switching. Once the output voltage falls 0.1 V below the OVP threshold, the device resumes operating again.

7.3.7 Output Short-to-Ground Protection

The TPS61022 starts to limit the output current when the output voltage is below 1.8 V. The lower the output voltage reaches, the smaller the output current is. When the VOUT pin is short to ground, and the output voltage becomes less than 0.4 V, the output current is limited to approximate 700 mA. Once the short circuit is released, the TPS61022 goes through the soft start-up again to the regulated output voltage.

7.3.8 Thermal Shutdown

The TPS61022 goes into thermal shutdown once the junction temperature exceeds 150°C. When the junction temperature drops below the thermal shutdown recovery temperature, typically 130°C, the device starts operating again.

7.4 Device Functional Modes

The TPS61022 operates at a quasi-constant frequency pulse width modulation (PWM) in moderate-to heavy load condition. Based on the input voltage to output voltage ratio, a circuit predicts the required on-time of the switching cycle. At the beginning of each switching cycle, the low-side NMOS FET switch, shown in *Functional Block Diagram*, is turned on. The input voltage is applied across the inductor and the inductor current ramps up. In this phase, the output capacitor is discharged by the load current. When the on-time expires, the main switch NMOS FET is turned off, and the rectifier PMOS FET is turned on. The inductor transfers its stored energy to replenish the output capacitor and supply the load. The inductor current declines because the output voltage is higher than the input voltage. When the inductor current hits a value that is the error amplifier's output, the next switching cycle starts again. The error amplifier compares the feedback voltage of the output voltage with an internal reference voltage; its output determines the inductor valley current in every switching cycle.

In light load condition, the TPS61022 implements two operation modes (power-save mode with PFM and forced PWM mode) to meet different application requirements. The operation modes are set by the status of the MODE pin. When the MODE pin is connected to logic low, the device works in the PFM mode. When the MODE pin is connected to logic high, the device works in the forced PWM mode.

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Device Functional Modes (接下页)

7.4.1 Forced PWM Mode

In the forced PWM mode, the TPS61022 keeps the switching frequency constant in light load condition. When the load current decreases, the output of the internal error amplifier decreases as well to keep the inductor current down and deliver less power from input to output. When the output current further reduces, the current through the inductor decreases to zero during the off-time. The high-side P-MOSFET is not turned off even if the current through the MOSFET is zero. Thus, the inductor current changes its direction after it runs to zero. The power flow is from output side to input side. The efficiency is low in this mode. But with the fixed switching frequency, there is no audible noise and other problems which might be caused by low switching frequency in light load condition.

7.4.2 Power-Save Mode

The TPS61022 integrates a power-save mode with PFM to improve efficiency at light load. When the load current decreases, the inductor valley current set by the output of the error amplifier no longer regulates the output voltage. When the inductor valley current hits the low limit of 150 mA, the output voltage exceeds the setting voltage as the load current decreases further. When the FB voltage hits the PFM reference voltage, the TPS61022 goes into the power-save mode. In the power-save mode, when the FB voltage rises and hits the PFM reference voltage, the device continues switching for several cycles because of the delay time of the internal comparator — then it stops switching. The load is supplied by the output capacitor, and the output voltage declines. When the FB voltage falls below the PFM reference voltage, after the delay time of the comparator, the device starts switching again to ramp up the output voltage.

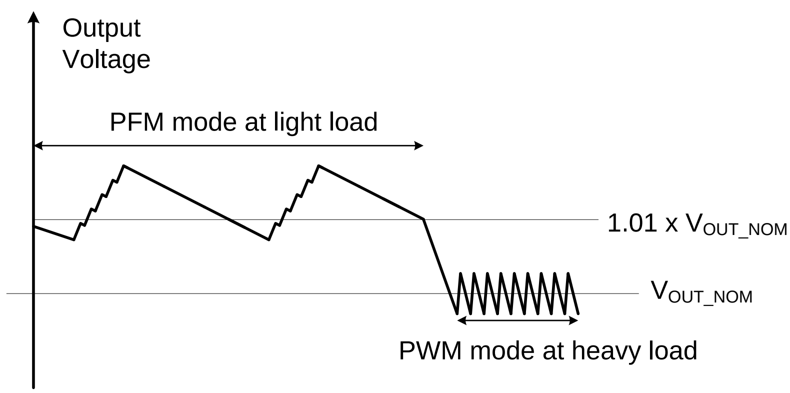

图 15. Output Voltage in PWM Mode and PFM Mode

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS61022 is a synchronous boost converter designed to operate from an input voltage supply range between 0.5 V and 5.5 V with a minimum 6.5-A valley switch current limit. The TPS61022 typically operates at a quasi-constant 1-MHz frequency PWM at moderate-to-heavy load currents when the input voltage is above 1.5 V. The switching frequency changes to 0.6 MHz gradually with the input voltage changing from 1.5 V to 1 V for better efficiency and high step-up ratio. When the input voltage is below 1 V, the switching frequency is fixed at a quasi-constant 0.6 MHz. At light load currents, when the MODE pin is set to low logic level, the TPS61022 converter operates in power-save mode with PFM to achieve high efficiency over the entire load current range. When the MODE pin is set to high logic level, the TPS61022 converter operates in forced PWM mode to keep the switching frequency constant.

8.2 Typical Application

The TPS61022 provides a power supply solution for portable devices powered by batteries or backup applications powered by super-capacitors. With minimum 6.5-A switch current capability, the TPS61022 can output 5 V and 3 A from a single-cell Li-ion battery.

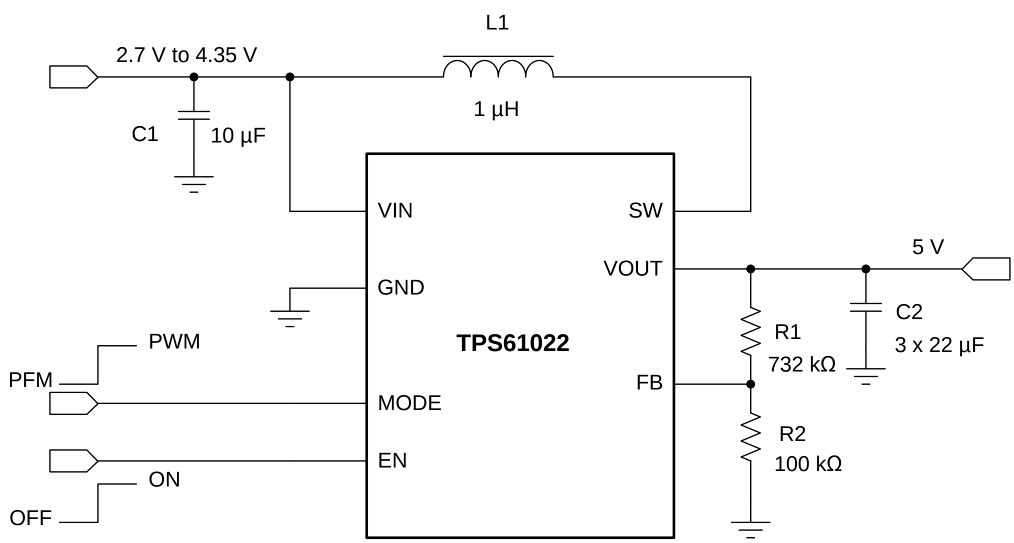

图 16. Li-ion Battery to 5-V Boost Converter

8.2.1 Design Requirements

The design parameters are listed in 表 1.

表 1. Design Parameters

PARAMETERS	VALUES
Input voltage	2.7 V to 4.35 V
Output voltage	5 V
Output current	3 A
Output voltage ripple	±50 mV

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8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Output Voltage

The output voltage is set by an external resistor divider (R1, R2 in 图 16). When the output voltage is regulated, the typical voltage at the FB pin is V_{REF}. Thus the resistor divider is determined by 公式 4.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R2$$

where
- V_{OUT} is the regulated output voltage
- V_{REF} is the internal reference voltage at the FB pin (4)

For best accuracy, keep R2 smaller than 300 kΩ to ensure the current flowing through R2 is at least 100 times larger than the FB pin leakage current. Changing R2 towards a lower value increases the immunity against noise injection. Changing the R2 towards a higher value reduces the quiescent current for achieving highest efficiency at low load currents.

8.2.2.2 Inductor Selection

Because the selection of the inductor affects steady-state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications, inductor value, saturation current, and dc resistance (DCR).

The TPS61022 is designed to work with inductor values between 0.33 µH and 2.9 µH. Follow 公式 5 to 公式 7 to calculate the inductor peak current for the application. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To have enough design margins, choose the inductor value with –30% tolerances, and low power-conversion efficiency for the calculation.

In a boost regulator, the inductor dc current can be calculated by 公式 5.

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta}$$

where
- V_{OUT} is the output voltage of the boost converter
- I_{OUT} is the output current of the boost converter
- V_{IN} is the input voltage of the boost converter
- η is the power conversion efficiency, use 90% for most applications (5)

The inductor ripple current is calculated by 公式 6.

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times D}{L \times f_{SW}}$$

where
- D is the duty cycle, which can be calculated by 公式 2
- L is the inductance value of the inductor
- f_{SW} is the switching frequency
- V_{IN} is the input voltage of the boost converter (6)

Therefore, the inductor peak current is calculated by 公式 7.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \quad (7)$$

Normally, it is advisable to work with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI. But in the same way, load transient response time is increased. The saturation current of the inductor must be higher than the calculated peak inductor current. 表 2 lists the recommended inductors for the TPS61022.

表 2. Recommended Inductors for the TPS61022

PART NUMBER	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	SIZE (LxWxH)	VENDOR
XAL7030-102MEC	1	5.00	28	8 × 8 × 3.1	Coilcraft
XAL6030-102MEC	1	6.18	23	6.36 × 6.56 × 3.1	Coilcraft
XEL5030-102MEC	1	8.40	16.9	5.3 × 5.5 × 3.1	Coilcraft
744316100	1	5.23	11.5	5.6 × 5.3 × 4.3	Wurth Elecktronik

8.2.2.3 Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability. The ripple voltage is related to capacitor capacitance and its equivalent series resistance (ESR). Assuming a ceramic capacitor with zero ESR, the minimum capacitance needed for a given ripple voltage can be calculated by 公式 8.

$$C_{OUT} = \frac{I_{OUT} \times D_{MAX}}{f_{SW} \times V_{RIPPLE}}$$

where

- D_{MAX} is the maximum switching duty cycle
- V_{RIPPLE} is the peak-to-peak output ripple voltage
- I_{OUT} is the maximum output current
- f_{SW} is the switching frequency (8)

The ESR impact on the output ripple must be considered if tantalum or aluminum electrolytic capacitors are used. The output peak-to-peak ripple voltage caused by the ESR of the output capacitors can be calculated by 公式 9.

$$V_{RIPPLE(ESR)} = I_{L(P)} \times R_{ESR} \quad (9)$$

Take care when evaluating the derating of a ceramic capacitor under dc bias voltage, aging, and ac signal. For example, the dc bias voltage can significantly reduce capacitance. A ceramic capacitor can lose more than 50% of its capacitance at its rated voltage. Therefore, always leave margin on the voltage rating to ensure adequate capacitance at the required output voltage. Increasing the output capacitor makes the output ripple voltage smaller in PWM mode.

TI recommends using the X5R or X7R ceramic output capacitor in the range of 10-µF to 50-µF effective capacitance. The output capacitor affects the small signal control loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable. Increasing the output capacitor makes the output ripple voltage smaller in PWM mode.

8.2.2.4 Loop Stability, Feedforward Capacitor Selection

When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable.

The load transient response is another approach to check the loop stability. During the load transient recovery time, V_{OUT} can be monitored for settling time, overshoot or ringing that helps judge the stability of the converters. Without any ringing, the loop has usually more than 45° of phase margin.

A feedforward capacitor (C3 in the 图 17) in parallel with R1 induces a pair of zero and pole in the loop transfer function. By setting the proper zero frequency, the feedforward capacitor can increase the phase margin to improve the loop stability. For large output capacitance more than 40 µF application, TI recommends a feedforward capacitor to set the zero frequency (f_{FFZ}) to 2 kHz. As for the input voltage lower than 2-V application, TI recommends setting the zero frequency (f_{FFZ}) to 20 kHz when the effective output capacitance is less than 40 µF. The value of the feedforward capacitor can be calculated by 公式 10.

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$$C3 = \frac{1}{2\pi \times f_{FFZ} \times R1}$$

where

- R1 is the resistor between the VOUT pin and FB pin
- f_{FFZ} is the zero frequency created by the feedforward capacitor (10)

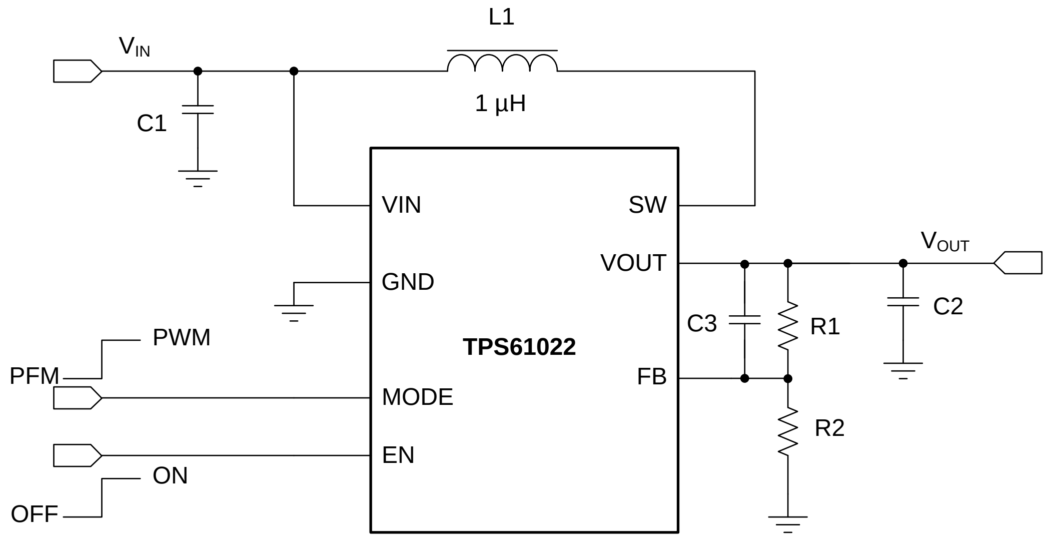
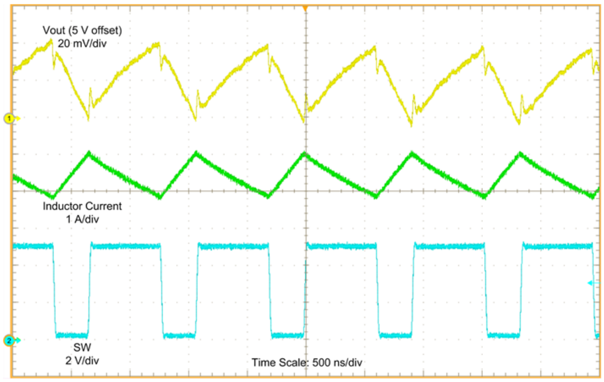


图 17. TPS61022 Circuit With Feedforward Capacitor

8.2.2.5 Input Capacitor Selection

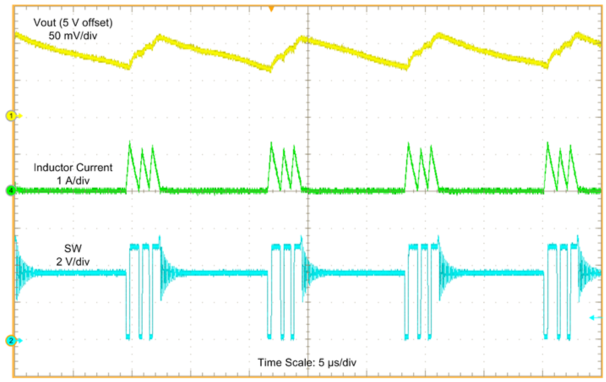
Multilayer X5R or X7R ceramic capacitors are excellent choices for input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors must be located as close as possible to the device. While a 10-µF input capacitor is sufficient for most applications, larger values may be used to reduce input current ripple without limitations. Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. In this circumstance, place additional bulk capacitance (tantalum or aluminum electrolytic capacitor) between ceramic input capacitor and the power source to reduce ringing that can occur between the inductance of the power source leads and ceramic input capacitor.

8.2.3 Application Curves



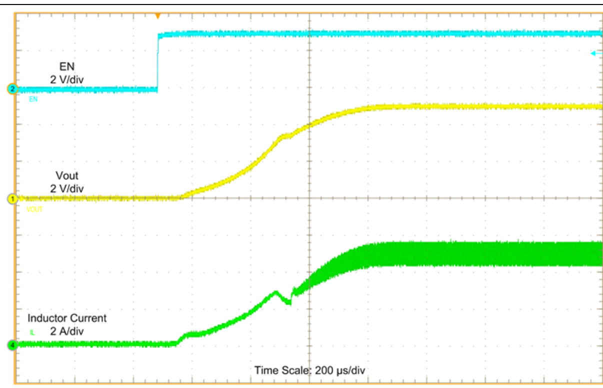
V_{IN} = 3.6 V, V_{OUT} = 5 V, I_{OUT} = 3 A

图 18. Switching Waveform at Heavy Load



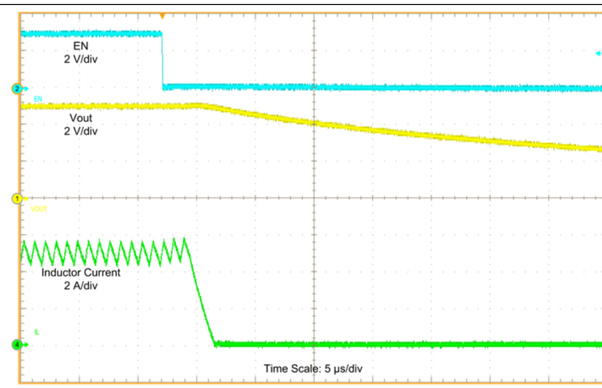
V_{IN} = 3.6 V, V_{OUT} = 5 V, I_{OUT} = 100 mA , MODE = low

图 19. Switching Waveform at Light Load



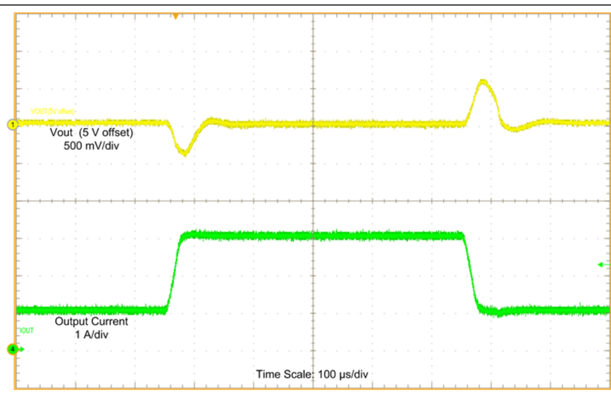
V_{IN} = 3.6 V, V_{OUT} = 5 V, 1.6-Ω resistance load

图 20. Start-up Waveform



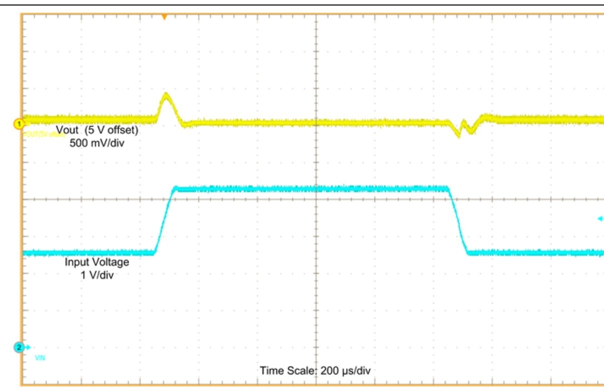
V_{IN} = 3.6 V, V_{OUT} = 5 V, 1.6-Ω resistance load

图 21. Shutdown Waveform



V_{IN} = 3.6 V, V_{OUT} = 5 V, I_{OUT} = 1 A to 3 A with 20-µs slew rate

图 22. Load Transient



V_{IN} = 2.7 V to 4.35 V with 50-µs slew rate, V_{OUT} = 5 V, I_{OUT} = 3 A

图 23. Line Transient

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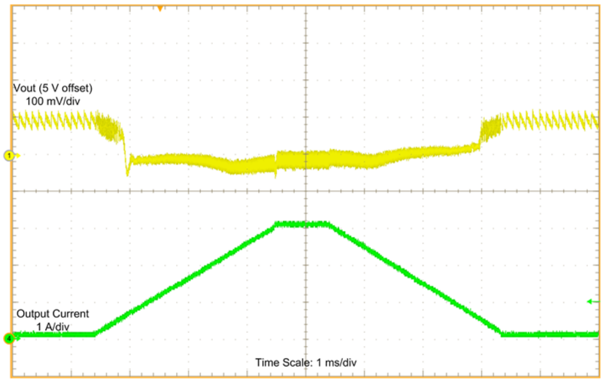
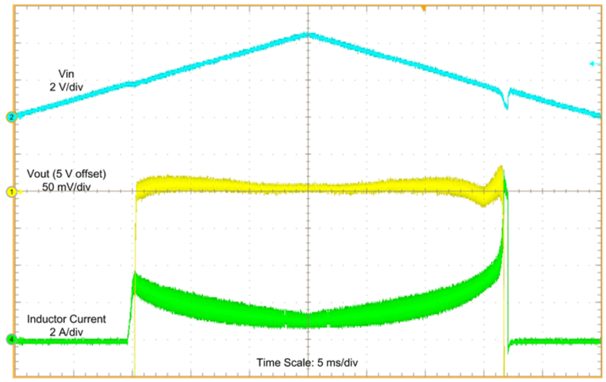


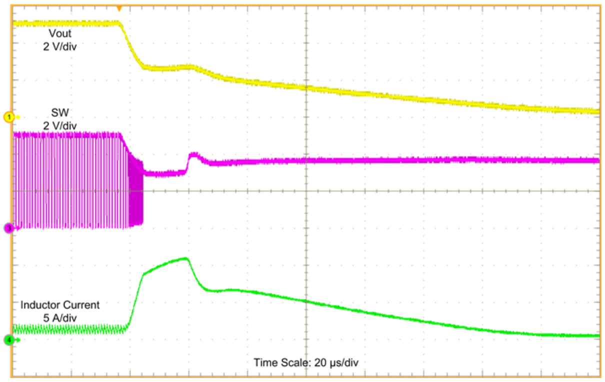
V_{IN} = 3.6 V, V_{OUT} = 5 V, I_{OUT} = 0 A to 3 A Sweep, MODE = low

图 24. Load Sweep



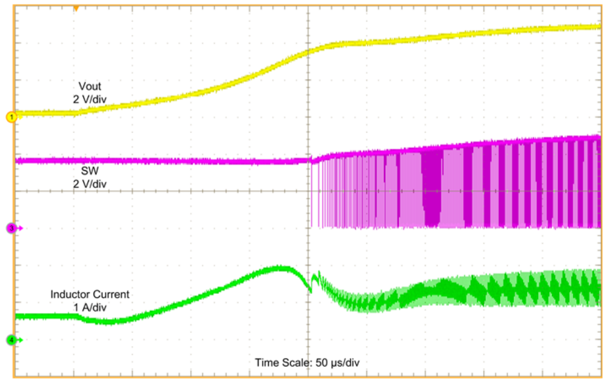
V_{IN} = 0 V to 4.35 V Sweep, V_{OUT} = 5 V, I_{OUT} = 1 A

图 25. Line Sweep



V_{IN} = 3.6 V, V_{OUT} = 5 V, I_{OUT} = 1 A

图 26. Output Short Protection (Entry)



V_{IN} = 3.6 V, V_{OUT} = 5 V, I_{OUT} = 1 A

图 27. Output Short Protection (Recover)

8.3 System Examples

For those applications with input voltage higher than 4.8 V, TI suggests adding a diode between the VIN pin and the VOUT pin to pre-bias the output before the TPS61022 is enabled. As an example shown in 图 28, the input voltage is from a USB port in the range of 4.5 V to 5.25 V. The target output voltage is 5 V to 5.25 V.

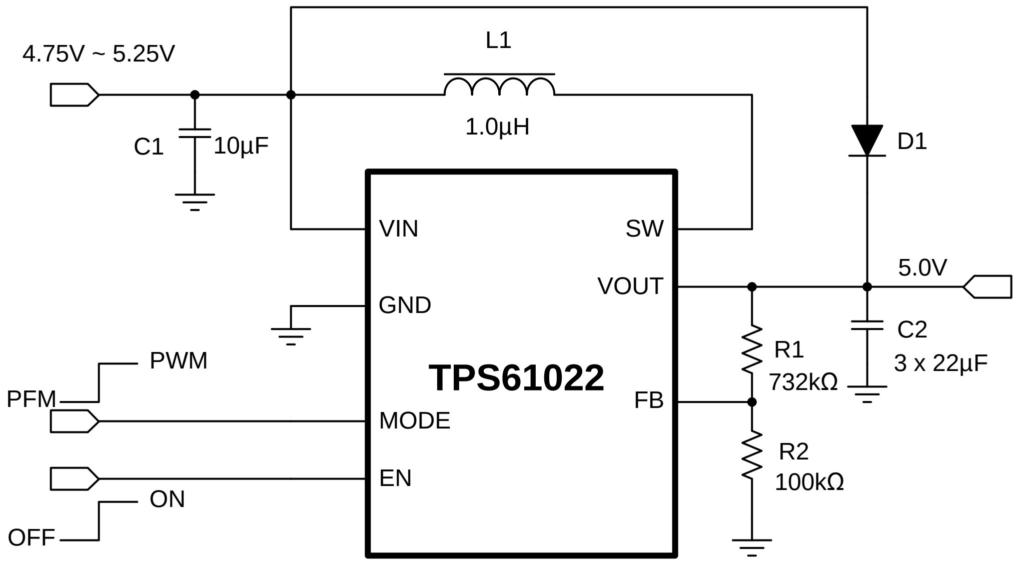


图 28. TPS61022 Circuit for V_{IN} > 4.8-V Application

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 0.5 V to 5.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A typical choice is a tantalum or aluminum electrolytic capacitor with a value of 100 µF. Output current of the input power supply must be rated according to the supply voltage, output voltage, and output current of the TPS61022.

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10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If the layout is not carefully done, the regulator could suffer from instability and noise problems. To maximize efficiency, switch rise and fall time are very fast. To prevent radiation of high frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling. The input capacitor needs not only to be close to the VIN pin, but also to the GND pin in order to reduce input supply ripple.

The most critical current path for all boost converters is from the switching FET, through the rectifier FET, then the output capacitors, and back to ground of the switching FET. This high current path contains nanosecond rise and fall time and must be kept as short as possible. Therefore, the output capacitor not only must be close to the VOUT pin, but also to the GND pin to reduce the overshoot at the SW pin and VOUT pin.

10.2 Layout Example

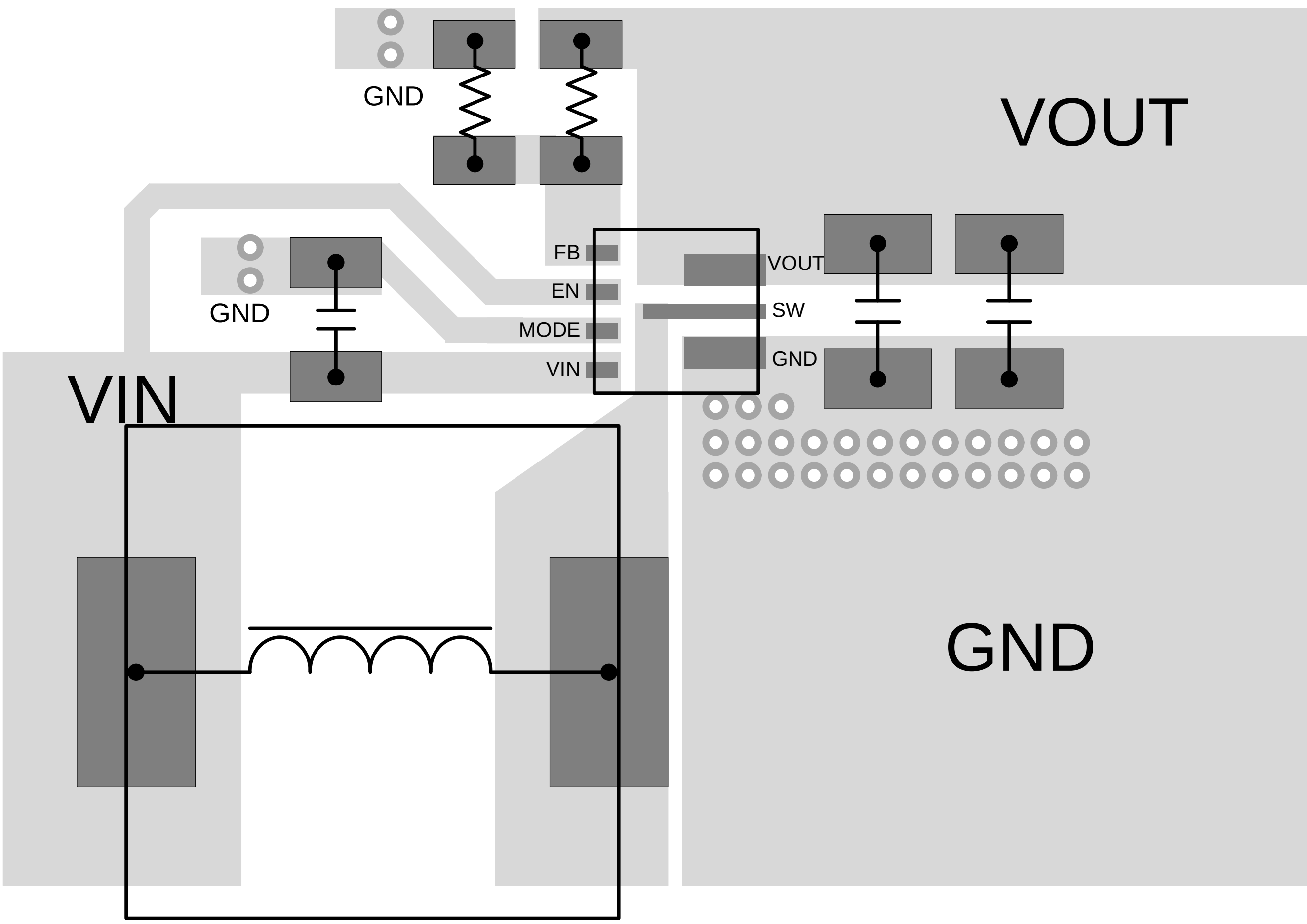

图 29. Layout Example

10.3 Thermal Considerations

Restrict the maximum IC junction temperature to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using 公式 11.

$$P_{D(max)} = \frac{125 - T_A}{R_{\theta JA}}$$

where

- T_A is the maximum ambient temperature for the application
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in *Thermal Information* (11)

The TPS61022 comes in a VQFN package. This package includes three power pads that improves the thermal capabilities of the package. The real junction-to-ambient thermal resistance of the package greatly depends on the PCB type, layout, and thermal pad connection. Using larger and thicker PCB copper for the power pads (GND, SW, and VOUT) to enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

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11 器件和文档支持

11.1 器件支持

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11.6 术语表

SLYZ022 — *TI 术语表*。
这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61022RWUR	ACTIVE	VQFN-HR	RWU	7	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1UNF	Samples
TPS61022RWUT	ACTIVE	VQFN-HR	RWU	7	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1UNF	Samples
XTPS61022RWUT	ACTIVE	VQFN-HR	RWU	7	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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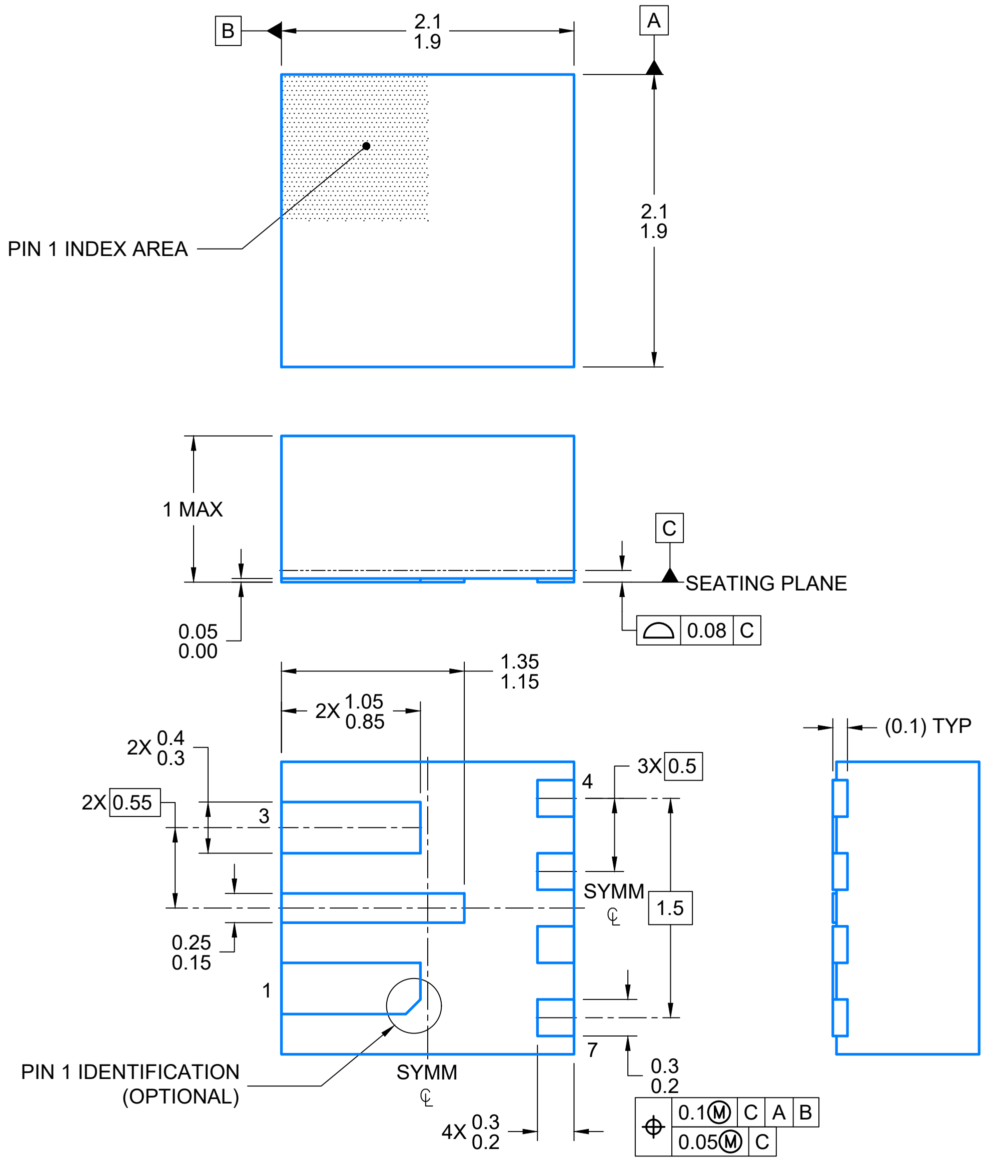

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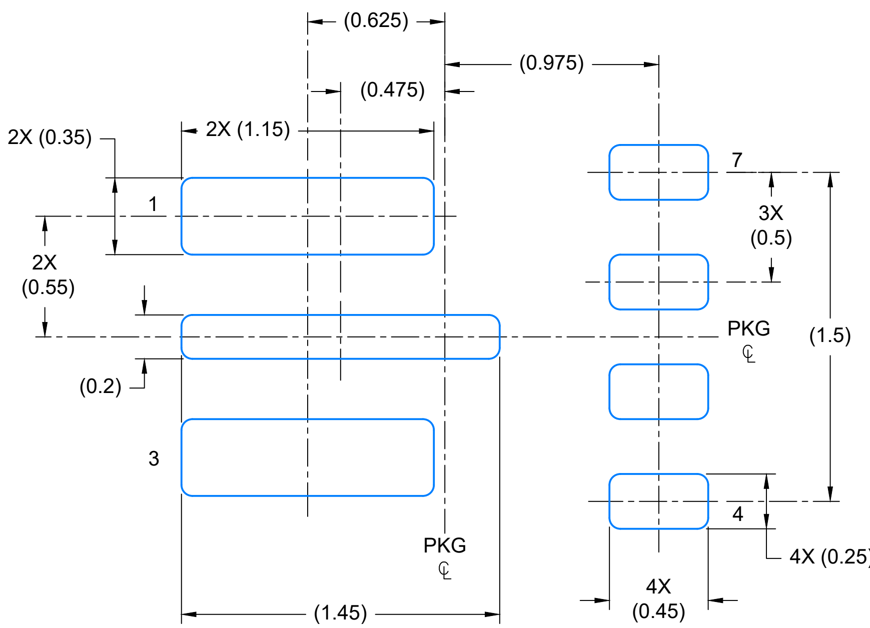
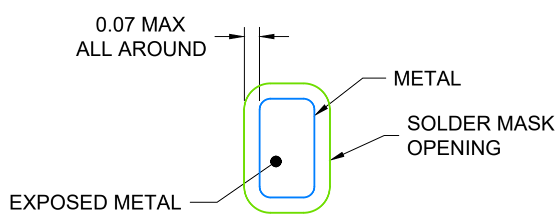
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



NON- SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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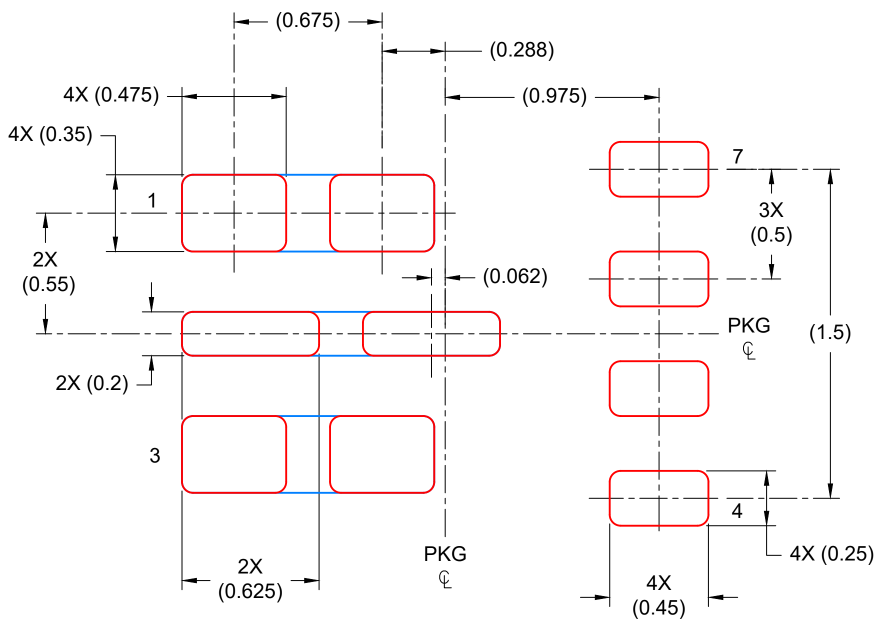
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1-3: 83%
SCALE: 30X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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