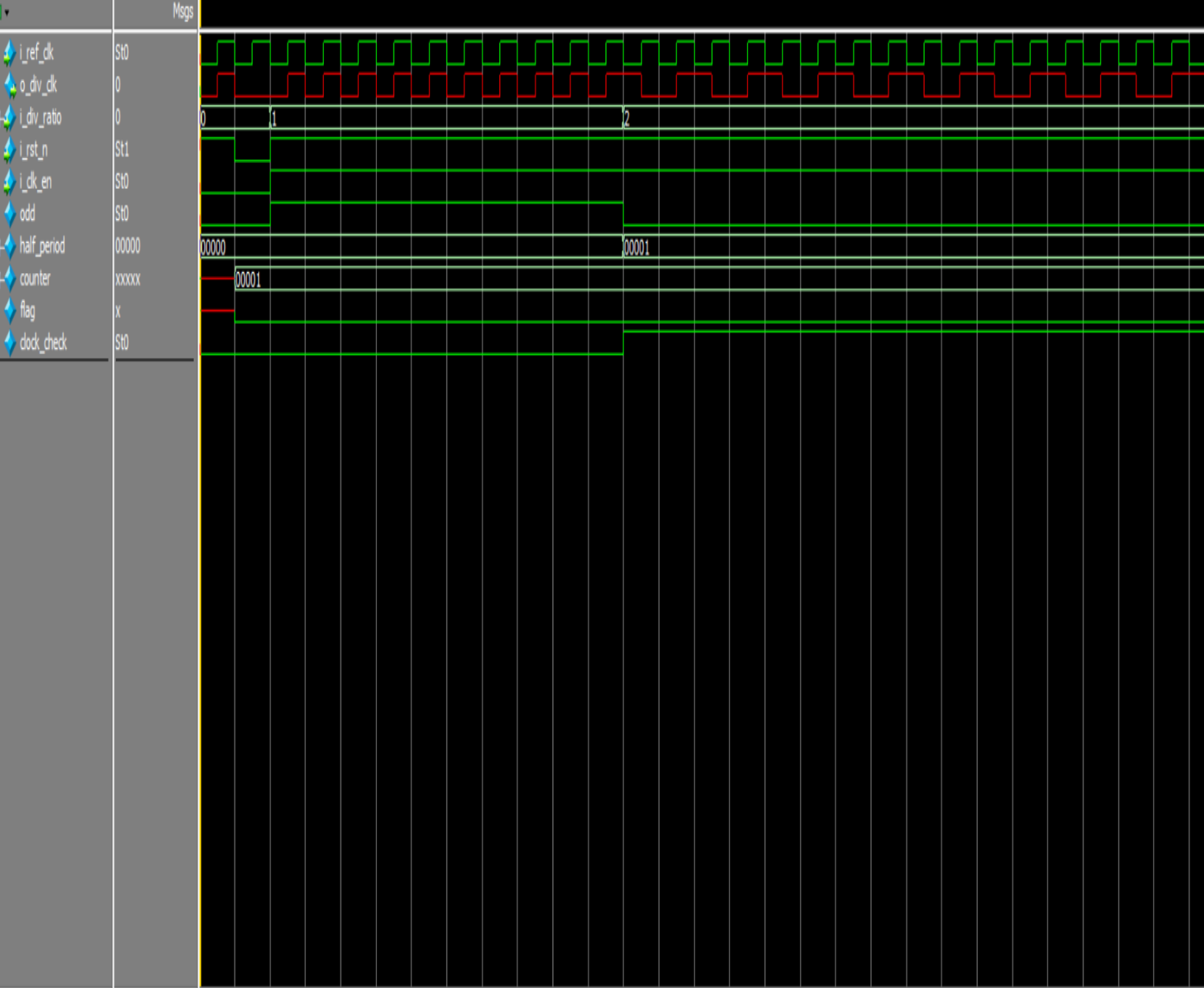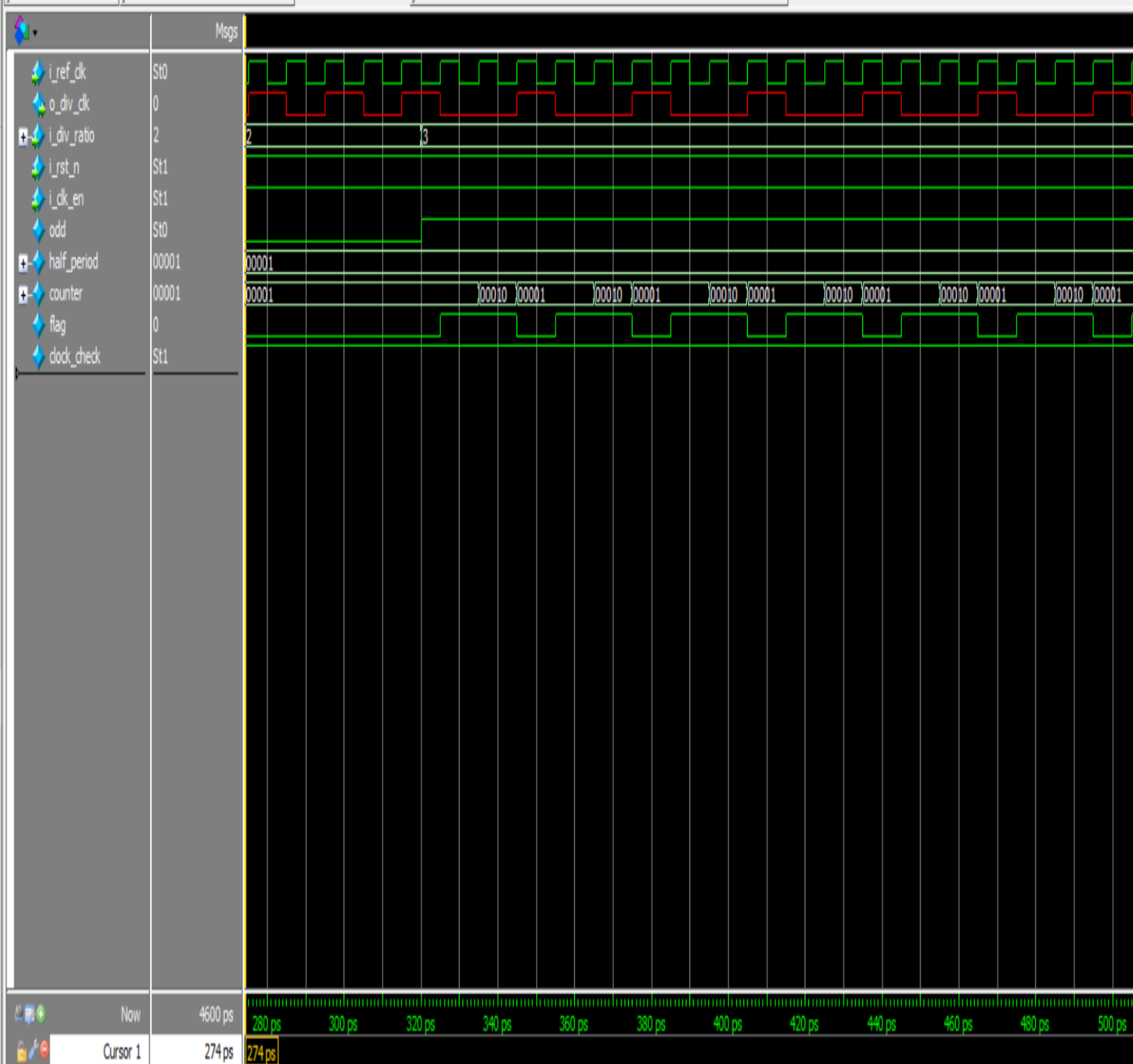# Name: Boutros George Sabri

# Digital IC design
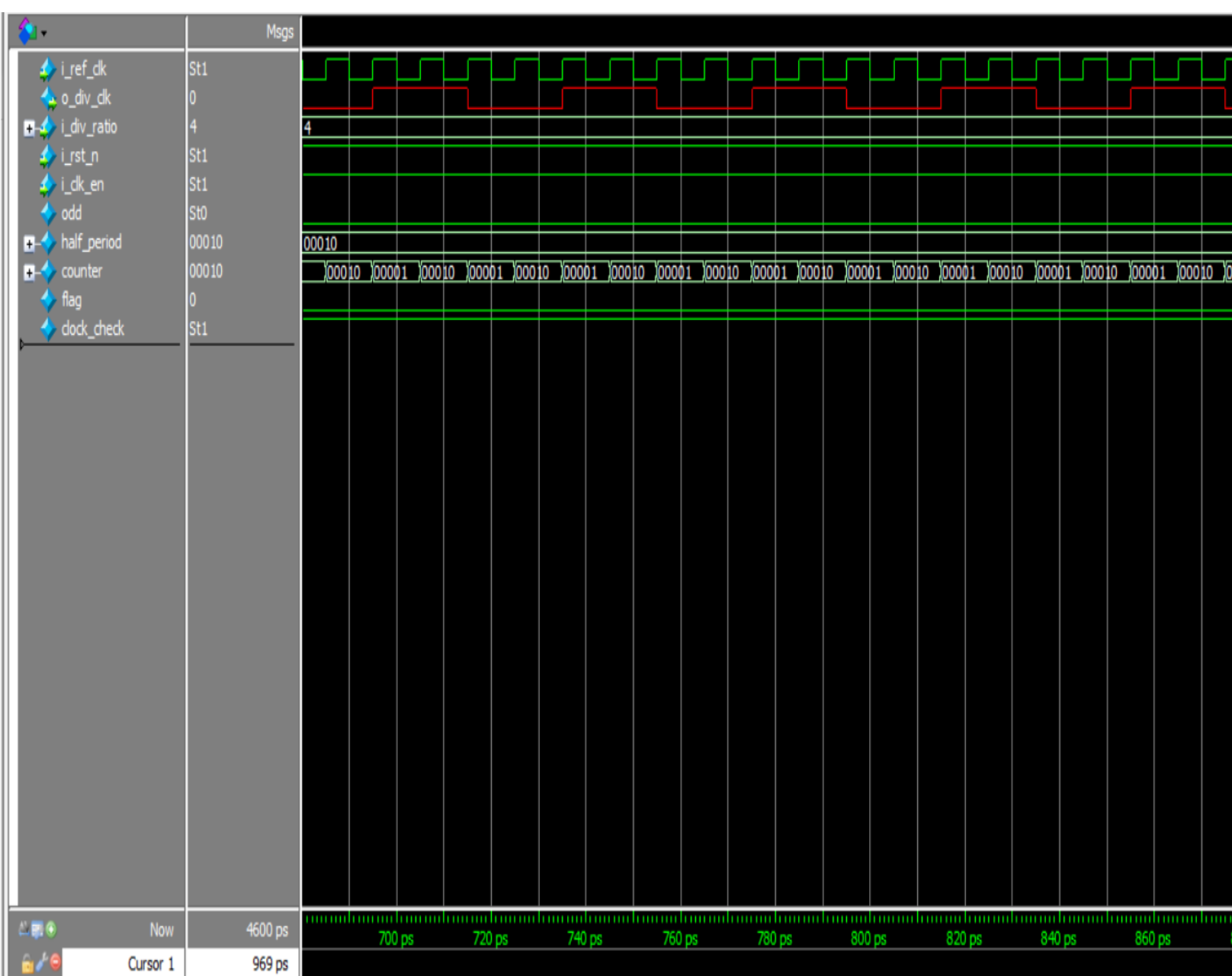
# Clock divider
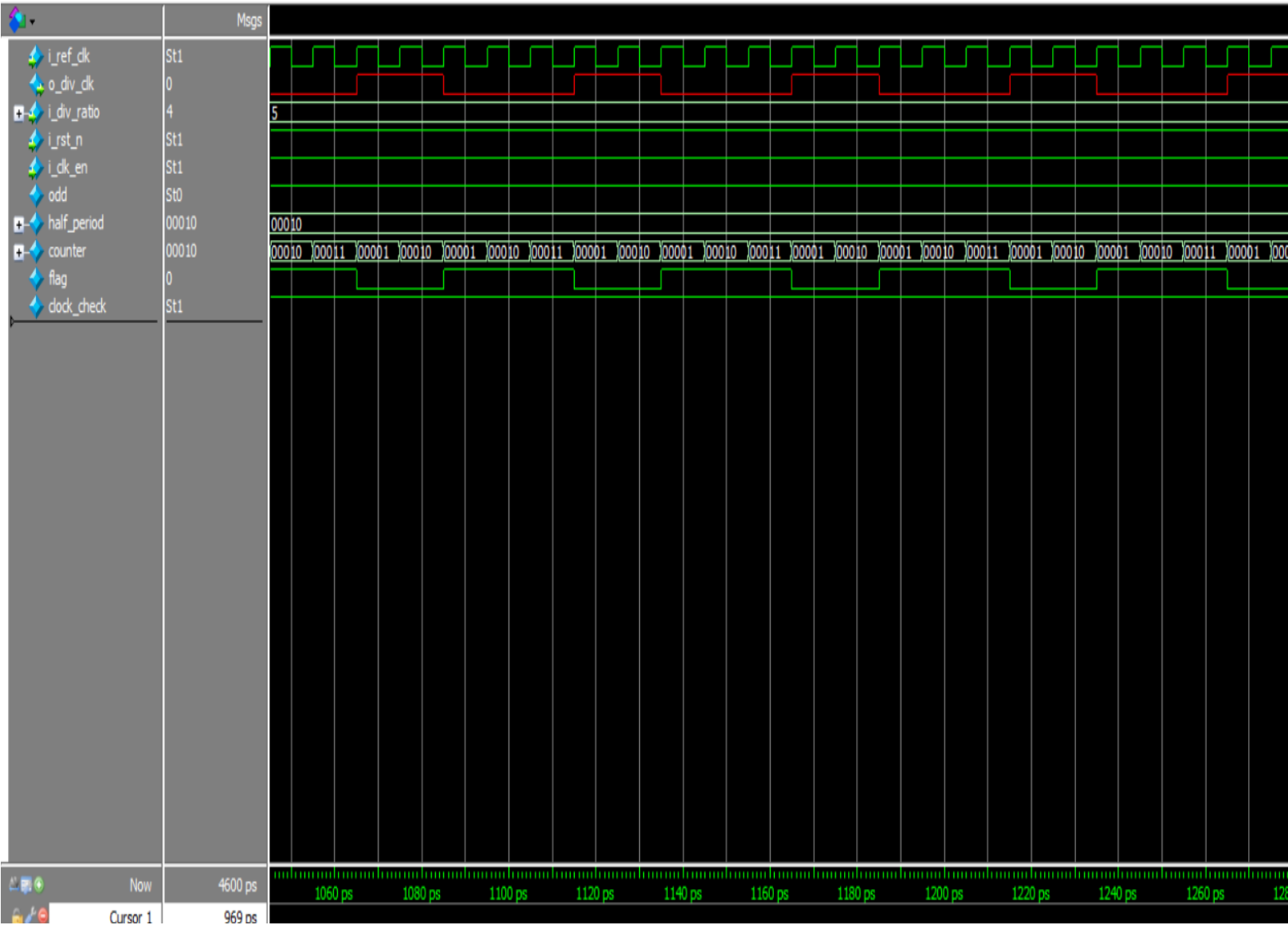
O_div_clk equals i_ref_clk when i_div_ratio equals 0 or 1 and then o_div_clk when i_div_ratio=2

i_ref_clk St0
o_div_clk 0
i_div_ratio 2
i_rst_n St1
i_clk_en St1
odd St0
half_period 00001
counter 00001
flag 0
clock_check St1

Now 4600 ps
Cursor 1 274 ps

**O_div_clk when i_div_ratio=3**

| | Msgs | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| i_ref_clk | St1 | | | | | | | | | | | | | | | | | | | | | |
| o_div_clk | 0 | | | | | | | | | | | | | | | | | | | | | |
| i_div_ratio | 4 | 4 | | | | | | | | | | | | | | | | | | | | |
| i_rst_n | St1 | | | | | | | | | | | | | | | | | | | | | |
| i_clk_en | St1 | | | | | | | | | | | | | | | | | | | | | |
| odd | St0 | | | | | | | | | | | | | | | | | | | | | |
| half_period | 00010 | 00010 | | | | | | | | | | | | | | | | | | | | |
| counter | 00010 | 00010 | 00001 | 00010 | 00001 | 00010 | 00001 | 00010 | 00001 | 00010 | 00001 | 00010 | 00001 | 00010 | 00001 | 00010 | 00001 | 00010 | 00001 | 00010 | | |
| flag | 0 | | | | | | | | | | | | | | | | | | | | | |
| clock_check | St1 | | | | | | | | | | | | | | | | | | | | | |

| | | |
|---|---|---|
| Now | 4600 ps | |
| Cursor 1 | 969 ps | |

700 ps  720 ps  740 ps  760 ps  780 ps  800 ps  820 ps  840 ps  860 ps

**O_div_clk when i_div_ratio=4**

i_ref_clk St1
o_div_clk 0
i_div_ratio 4
i_rst_n St1
i_clk_en St1
odd St0
half_period 00010
counter 00010
flag 0
clock_check St1

Now 4600 ps
Cursor 1 969 ps

**O_div_clk when i_div_ratio=5**

| | Msgs | |
|---|---|---|
| i_ref_clk | St1 | |
| o_div_clk | 0 | |
| i_div_ratio | 4 | 6 |
| i_rst_n | St1 | |
| i_clk_en | St1 | |
| odd | St0 | |
| half_period | 00010 | 00011 |
| counter | 00010 | 00001 00010 00011 00001 00010 00011 00001 00010 00011 00001 00010 00011 00001 00010 00011 00001 00010 00011 00001 00010 00011 00001 00010 00011 |
| flag | 0 | |
| clock_check | St1 | |

O_div_clk when i_div_ratio=6

| | | Msgs | |
|---|---|---|---|
| i_ref_clk | St1 | | |
| o_div_clk | 0 | | |
| i_div_ratio | 4 | 7 | |
| i_rst_n | St1 | | |
| i_clk_en | St1 | | |
| odd | St0 | | |
| half_period | 00010 | 00011 | |
| counter | 00010 | 00011 00100 00001 00010 00011 00001 00010 00011 00100 00001 00010 00011 00001 00010 00011 00100 00001 00010 00011 00001 00010 00011 00100 | |
| flag | 0 | | |
| clock_check | St1 | | |

| Now | 4600 ps | 2180 ps 2200 ps 2220 ps 2240 ps 2260 ps 2280 ps 2300 ps 2320 ps 2340 ps 2360 ps 2380 ps |
|---|---|---|
| Cursor 1 | 969 ns | |

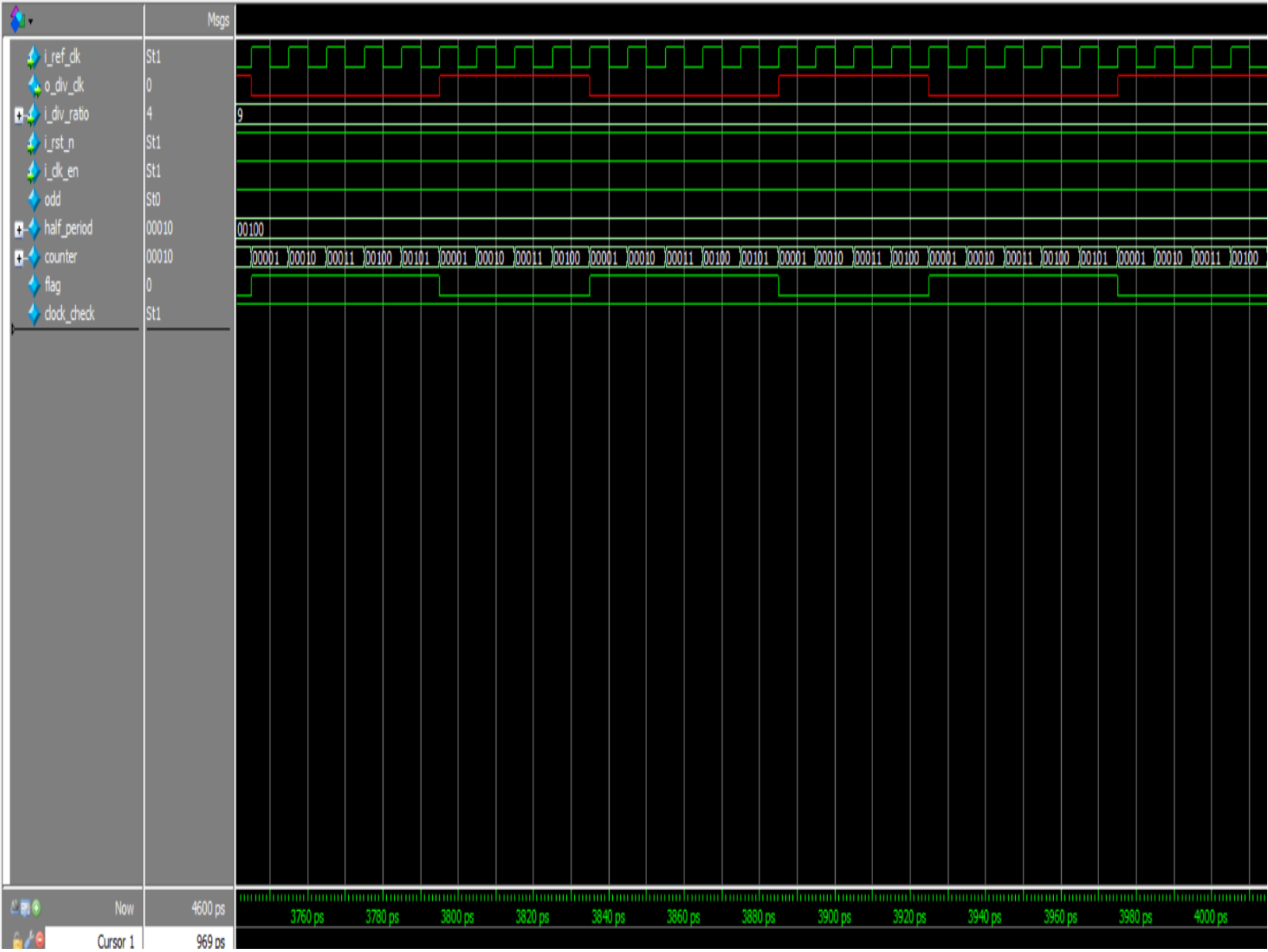**O_div_clk when i_div_ratio=7**

O_div_clk when i_div_ratio=8

O_div_clk when i_div_ratio=9