HARRIS RTX 2000 vs. AMD Am29000 architecture comparison

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Vilnius
2024

General info

The **AMD Am29000**, announced in March 1987 and released in May 1988, commonly shortened to 29k, is a family of 32-bit RISC microprocessors and microcontrollers developed and fabricated by Advanced Micro Devices (AMD). Based on the seminal Berkeley RISC, the 29k added a number of significant improvements. They were, for a time, the most popular RISC chips on the market. It ran at a 25 MHz nominal operating frequency and supported 17 million instructions per second sustained and 1.5 clock cycles per instruction average.

The **HARRIS RTX 2000** (**RTX2010**), launched in 1988, manufactured by Intersil, is a radiation hardened stack machine microprocessor which has been used in numerous spacecraft. With a max. CPU clock rate 8 MHz It is a two-stack machine, each stack 256 words deep, that supports direct execution of Forth programming language. Subroutine calls and returns only take one processor cycle and it also has a very low and consistent interrupt latency of only four processor cycles, which lends it well to realtime applications. Step Arithmetic instructions which are performed through the ALU are divide and square root. Execution of each step of the arithmetic operation takes one cycle, a 32/16-bit Step Divide takes 21 cycles, and a 32/16-bit Step Square Root takes 25 cycles.

Physical characteristics

The AMD Am29000, contained 428,000 transistors on a 1-micron process with a 0.8-micron effective channel length, making it a VLSI machine. The Am29000 was 1.1" x 1.1" or 2.8cm x 2.8cm in size and it‘s Maximum power dissipation was 2.31 Watts (specifically the Am29000-20KC, the size and wattage varied).

The RTX2010, is a microprocessor making it VLSI. Die dimensions: 364 mils x 371 mils x 21 mils ±1mil. Maximum Package Power Dissipation : 2 Watts.

The weight of both machines is negligible, most likely a few grams at most.

Architecture

The AMD Am29000 was a 32-bit architecture, with a machine word size of 32 bits. The 29k evolved from the same Berkeley RISC design. It‘s a three-adress instruction architecture. The registers were how 29000 differed from earlier designs, using a variable window size. It also added more registers, including the same 128 registers for the procedure stack, but adding another 64 for global access. The 29000 also extended the register window stack with an in-memory (and in theory, in-cache) stack. When the window filled the calls would be pushed off the end of the register stack into memory, restored as required when the routine returned. Generally, the 29000's register usage was considerably more advanced than competing designs based on the Berkeley concepts. The Am29000 contains 23 special-purpose registers. These registers provide controls and data for certain processor functions. Special-purpose registers are accessed by data movement only. Any special-purpose register can be written with the contents of any general-purpose register, and any general-purpose register can be written with the contents of any special-purpose register. Operations cannot be directly performed on the contents of special-purpose registers. Some special-purpose registers are protected, and can be accessed only in the Supervisor mode. This restriction applies to both read and write accesses. An attempt by a User-mode program to access a protected register causes a trap to occur. It did not implement flags.
Normal program flow may be preempted by an interrupt or trap for which the processor is enabled. The effect on the processor is identical for interrupts and traps; the distinction is in the different mechanisms by which interrupts and traps are enabled. It is intended that interrupts be used for suspending current program execution and causing another program to execute, while traps are used to report errors and exceptional conditions.

HARRIS RTX 2000 is a two-stack machine, each stack 256 words deep, with 16 bit wide words. Each 256-word stack may be subdivided into up to eight 32 word substacks, four 64 word substacks, or two 128 word substacks. Being a stack machine, it was therefore, zero-address. This processor contains eight 16-bit internal registers, which may be accessed implicitly or explicitly, depending upon the register accessed and the function being performed. There are:

- RTX Internal Registers
- Timer/Counter Registers
- Multiplier-Accumulator (MAC) Registers
- On-Chip Peripheral Registers
- Interrupt Controller Registers
- Stack Controller Registers
- Memory Page Controller Registers

Events in an interrupt sequence are as follows:
e1. The Interrupt Controller samples the interrupt request inputs on the rising edge of PCLK. If NMI rises between e1 and the rising edge of PCLK prior to e5, the interrupt vector will be for NMI.
e2. If any interrupt requests were sampled, the Interrupt Controller issues an interrupt request to the core on the falling edge of PCLK.
e3. The core samples the state of the interrupt requests from the Interrupt Controller on the falling edge of PCLK. If INTSUP is high, maskable
interrupts will not be detected at this time.
e4. When the core samples an interrupt request on the falling edge of PCLK, an Interrupt Acknowledge cycle will begin on the next rising edge
of PCLK.
e5. Following the detection of an interrupt request by the core, an Interrupt Acknowledge cycle begins. The interrupt vector will be based on the highest priority interrupt request active at this time.
Interrupt requests should be held active until the Interrupt Acknowledge cycle for that interrupt occurs

RTX 2000 implemanted flags:
FATAL STACK ERROR FLAG
PARAMETER STACK UNDERFLOW FLAG
PARAMETER STACK OVERFLOW FLAG
RETURN STACK UNDERFLOW FLAG
RETURN STACK OVERFLOW FLAG

Memory

The AMD Am29000 has 4 giga-byte virtual address space. External instructions and data are contained in one of four, 32-bit address-spaces:
1) InstructionlData Memory.
2) Input/Output.
3) Coprocessor.
4) Instruction Read-Only Memory (Instruction ROM).

An address in the InstructiOn/Data Memory address-space may be treated as virtual or physical, as determined by the Current Processor Status Register. Address translation for data accesses is enabled separately from address translation for instruction accesses. A

program in the Supervisor mode may temporarily disable address translation for individual loads and stores; this permits load-real and store-real operations.
It is possible to partition physical instruction and data addresses into two, separate physical address-spaces. However, virtual instruction and data addresses appear in the same virtual address-space (i.e instruction/data memory).

Am29k supported register-addressing and idirect register addressing.

A Branch Target Cache (512 bytes on the 29000 and 1024 bytes on the 29050) stored sets of 4 or 2 sequential instructions found at the branch target address, reducing the instruction fetch latency during taken branches

HARRIS RTX 2000: Each 256-word stack may be subdivided into up to eight 32 word substacks, four 64 word substacks, or two 128 word substacks. Each stack has a Stack Start Flag (PSF and RSF) which may be used for implementing virtual stacks. Manipulating the Stack Start Flag provides a mechanism for creating a virtual stack in memory which is maintained by interrupt driven handlers.

Bit 12 of the Memory Access Opcode, is used to determine whether byte or word operations are to be performed (where bit 12 = 0 signifies a word operation, and bit 12 = 1 signifies a byte operation). In addition, the determination of whether a byte swap is to occur depends on whether Addressing Mode 0 or Mode 1 is in effect (as determined by bit 2 of the cr and on whether an even or odd address is being accessed

Instruction set

The Am29000 instruction set contains 115 instructions. These instructions are divided into 9 classes:
1) Integer Arithmetic-perform integer add, subtract, multiply, and divide operations.
2) Compare-perform arithmetic and logical comparisons. Some instructions in this class allow the generation of a trap if the comparison condition is not met.
3) Logical-perform a set of bit-wise Boolean operations.
4) Shift-perform arithmetic and logical shifts, and allow the extraction of 32-bit words from 64-bit double-words.
5) Data Movement-perform mqvement of data fields between registers, and the movement of data to and from external devices and memories.
6) Constant-allow the generation of large constant values in registers.
7) Floating-Point-included for floating-point arithmetic, comparisons, and format conversions. These instructions are not currently implemented directly in processor hardware.
8) Branch-perform program jumps and subroutine calls.
9) Miscellaneous-perform miscellaneous control functions and operations not provided by other classes.

Some instruction examples:

JMPT Jump True

JMPTI	Jump True Indirect
LOAD	Load
LOADL	Load and Lock
LOADM	Load Multiple
LOADSET	Load and Set
MFSR	Move from Special Register
MFTLB	Move from Translation Look-Aside Buffer Register
MTSR	Move to Special Register
MTSRIM	Move to Special Register Immediate
MTTLB	Move to Translation Look-Aside Buffer Register
MUL	Multiply Step
MULL	Multiply Last Step
MULTIPLY	Integer Multiply
MULU	Multiply Step, Unsigned
NAND	NAND Logical

The instruction set for the HS-RTX2010RH TForth compiler combines multiple high level instructions into single machine instructions without having to rely on either pipelines or caches. This optimization yields an effective throughput which is faster than the processor's clock speed, while avoiding the unpredictable execution behavior exhibited by most RISC processors caused by pipeline flushes and cache misses.

Some instruction examples:
inv shift
lit inv
lit SWAP inv
lit SWAP op
nn inv (short literal)
nn OVER op
nn SWAP op
op shift
DUP @ SWAP
DUP nn G! inv
DUP U! inv
DUP U@ op
nn G! Inv
nn G@ inv
nn G@ DROP inv
nn G@ OVER op

Data types

AM 2900: A word is defined as 32 bits of data. A half-word consists of 16 bits, and a double-word consists of 64 bits. Bytes are 8 bits in length. The Am29000 has direct support for word.-integer(signed and unsigned), word-logical, word-Boolean, half-word integer (signed and unsigned), and character (byte) data. Other data types, such as character strings, are supported with sequences of basic instructions and/or external hardware. Single- and double-precision floating-point types are defined for the Am29000, but are not directly supported by hardware. The format for Boolean data used by the processor is such that the Boolean values TRUE and FALSE are represented by 1 and 0, respectively, in the most-significant bit of a word.

Most Am29000 instructions deal directly with word-length integer data; integers may be either signed or unsigned, depending on the instruction. Some instructions (e.g. AND) treat word-length operands as strings of bits. In addition, there is support for character, half-word, and Boolean data types. Single-precision and double-precision floating- point data types are defined, but not directly supported by processor hardware.

The 29050 was notable for being early to feature a floating point unit capable of executing one multiply–add operation per cycle.

HARRIS RTX 2000:
Single Cycle 16-Bit Multiply
Single Cycle 16-Bit Multiply Accumulate
Single Cycle 32-Bit Barrel Shift
Hardware Floating Point Support

Application areas

Positioned as a product for "medium- to high-performance embedded applications" with potential for use in Unix workstations, the 29000 was used in a variety of products such as X terminals, laser printer controller cards, graphics accelerator cards, optical character recognition solutions, and network bridges. The memory architecture of the 29000 was a particular attraction for product designers, allowing them to forego external cache memory and to employ dynamic RAM directly while maintaining acceptable performance, permitting a degree of flexibility in the choice of memory technologies used to retain program instructions and data.

One notable product utilising the 29k was Apple's Macintosh Display Card 8·24 GC for its Macintosh IIfx, featuring a 30 MHz Am29000 processor, 64 KB static RAM cache, and 2 MB of video RAM, with the option of an additional 2 MB of dynamic RAM for use by the QuickDraw graphical toolkit. The inclusion of the 29k differentiated this particular version of the card from other versions sold by Apple, significantly improving performance when handling 24-bits-per-pixel images.

Example spacecraft that use the RTX2010:

- Advanced Composition Explorer (ACE)
- NEAR/Shoemaker
- TIMED
- Rosetta's lander – Philae

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