中山大学软件学院 2009 级软件工程专业(2010 学年春季学期)

《SE-215 计算机组成原理与接口技术》

期末考试试卷(A)

(考试形式： 闭卷 考试时间：2 小时)

警示

《中山大学授予学士学位工作细则》第六条

考试作弊不授予学士学位

方向：_____ 姓名：_____ 学号：_____成绩：_____

注意：答案一定要写在答题纸上，写在本试卷中不给分。本试卷要和答卷一起交回。

Part I Fill in blanks（20 points）

1. (3 points) In every computer there are three types of buses:_____、_____ 、_____.

2. (3 points) A CPU consists of three basic parts: _____ , _____, and _____ .

3. (2 points)In Intel literature concerning 8086/8088, there are two types of addresses: _____ is the 20-bit address, logical address can be consists of _____, and offset address .

4. (5 points) Cache memory is placed between _____and _____ , there are three types of cache organization: _____ , _____ , and _____ .

5. (1 point) IF SP=2000H，six PUSHs and two POPs have been executed, then the current SP=_____.

6. (2 points) If 8259 is used with an 8088 CPU, the ICW2 is 08H，the interrupt of IR6 is _____H, the interrupt vector table location for IR6 is _____H.

7. (2 points) To ensure the integrity of the contents of ROM and RAM, the _____ is used for ROM, the _____ is used for RAM.

8. (2 points) State the status of A0 and BHE when accessing an even-addressed byte. A0= _____, BHE=_____.

Part II Answer the following questions. (15 points)

1. (8 points) Suppose three values x, y, and z are stored in a machine's memory. Describe the sequence of events (loading registers from memory, saving values in memory, and so on) that leads to the computation of x + y - z. How about (2x) + y?

2. (7 points) What is the function of the interrupt vector table? How many bytes are used by the interrupt vector table, and why?

Part III Choose the best answer from the choices. (20分)

1. (2 point) The purpose of decoder in CPU is ( )

A: Choose the special data to ALU

B: Instruction decoder

C: Address decoder

D: Data decoder

2. (2 points) Which one of the following is used to express the address in computer? ( )

A: signedmagnitude representation B: 1's complement

C: unsigned number D: 2's complement

3. (2 points) Main memory block can be placed into the cache of any location in the address mapping

A.associative B. set associative C.segment D.direct

4、(2 points) Which instruction is wrong? ( )

A: IN AL, DX B: OUT DX, AX

C: IN DX, AL D: OUT DX, AL

5. (2 points) The CPU finishes the present ( ) before it responds with HOLDA.

A: procedure B: instruction

C: clock period D: bus cycle

6. (2 points) According to the little endian convention, the hexadecimal number 12345678H will be stored from the lower address to higher address as, ( )

A. 12345678 B. 78563412 C. 56781234 D. 34127856

7. (2 points) DA1 DB 4 DUP (0, 2 DUP (1, 0, 0)), the size of DA1 is ( ).

A:28 B: 24 C: 20 D: 16

8. (2 points) Microinstructions are placed in ( )

A: memory controller B: main memory

C: control memory D: Cache

9. (2 points) In the IBM PC, the 74LS373 is used for ( )

A: Address latch B: isolating the address bus

C: address bus boosting D: All of the above

10. (2 points) For a special RAM chip, the organization is 512 x 8, the total number of address pins and data pins is ( ).

A: 21 B:17 C: 19 D:20

Part IV In a 5-level interrupt system, the default interrupt priority is 1→2→3→4→5. The interrupt mask bits are set to change the interrupt priority to 1→2→4→3→5. During the CPU execution of a program, IR2 and IR3 interrupt request arrive, when IR3 is being processed, IR4 and IR5 request arrive at the same time. At the end of IR4, IR1 interrupt request arrived.

1) Show the interrupt mask characters;

2) Draw the diagrams for CPU processing these interrupts (10 points)

Part V Write a program to convert all lowercase letters to uppercase. “MY name is Joe”. (8 points)

Part VI Show the design of an 8255 connection to the PC bus using simple logic gates. Assume port address 304H as the base port address for the 8255. (7 points)

Part VII Suppose that CPU has 16-bit address pins and 8-bit data pins, access the memory when $\overline{MREQ}$ is active low, $\overline{WR}$ is control signal (low for writing/ high for reading). Using this CPU and RAM (1K x 4), ROM (2K x 8), 74LS138, and several logic gates to build the system satisfy the following requests:

1) The assigned address space for ROM is 8000H ~ 87FFH
2) The assigned address space for RAM is 8800H ~ 8BFFH

How many chips are needed to build the system? Show the diagram. (10 points)

Part VIII (a) Find the control word if PA=out, PB=in, PC0-PC3=in, and PC4-PC7=out.
(b) Program the 8255 to get data from port A and send it to port B. In addition, data from PC0-PC3 is sent to the PC4-PC7.

Use port addresses of 300H-303H for the 8255 chip. (10 points)

Appendix

8255Control word

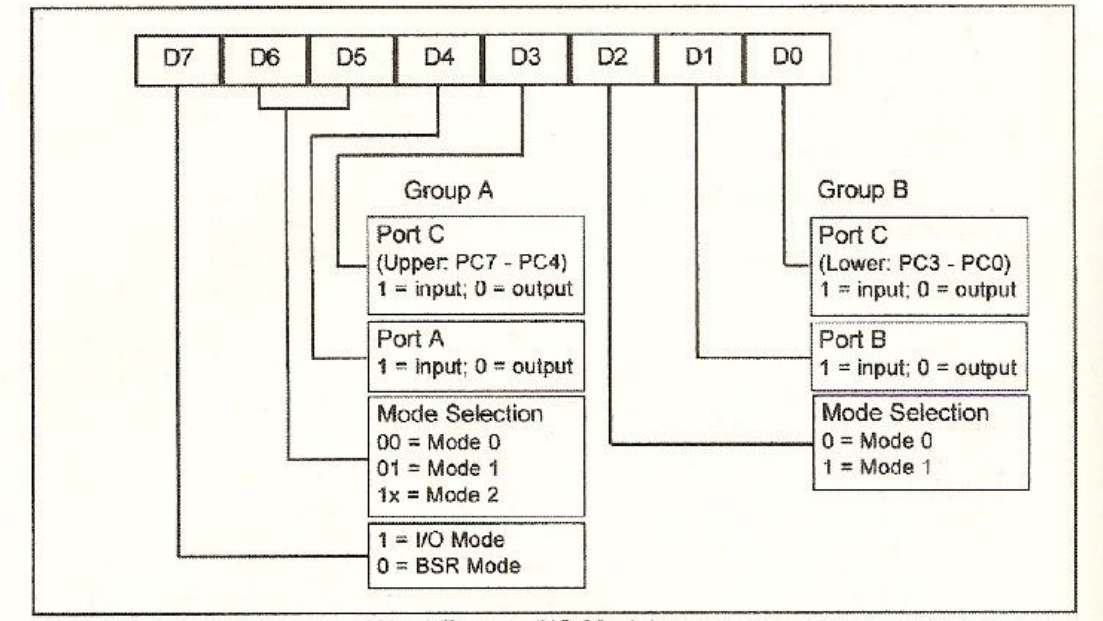

Figure 11-12. 8255 Control Word Format (I/O Mode)

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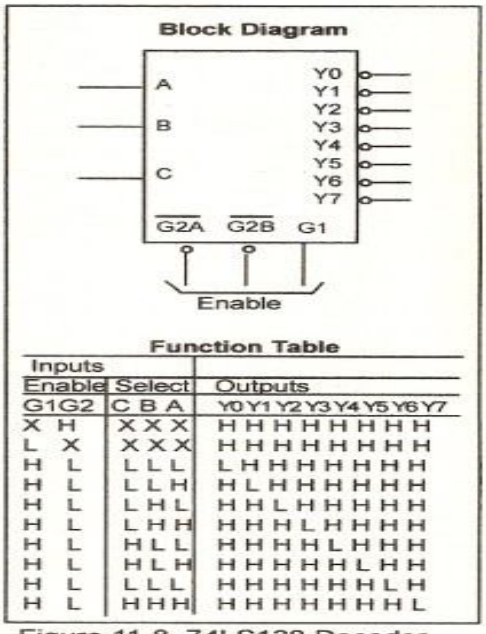
74LS138



Function Table

Inputs				Outputs							
Enable		Select									
G1	G2	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	L	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Figure 11-8. 74LS138 Decoder

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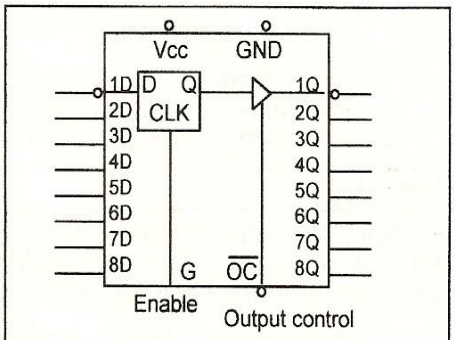

Function Table

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q0
H	X	X	Z

Figure 11-1. 74LS373 D Latch

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