中山大学软件学院 2010 级软件工程专业(2011 春季学期)

《计算机组成原理与接口技术》期末考试答案(A)

(考试形式： 闭卷 考试时间：2 小时)

警示

《中山大学授予学士学位工作细则》第六条

考试作弊不授予学士学位

方向：_____ 姓名：_____ 学号：_____成绩：_____

出卷：_____邓革、李国桢_____ 审核：_____

注意：答案一定要写在答题纸上，写在本试卷中不给分。本试卷要和答卷一起交回。

Part I Choose the best answer from the choices. (2 points for each question, 20 points total)

1. In register indirect addressing, the operand value is located in ( )

A. Register B. Instruction C. Memory D. Program Counter

C

2. Which condition can not result in the pipeline conflict.

A. bypass data B. resource conflict

C. data dependency D. conditional branch statements

A

3. Which register is visible to assemble language programmer?

A. Memory address register B. Program counter

C. Memory data register D. Instruction register

B

4. Computer organization is a computer architecture ( ) implementation。

A. physics B. logical C. circuit D. simulate

B

5. Which statement about RISC/CISC is not correct?

A. Most RISC instructions are executed with one clock cycle.

B. CISC architecture has many instructions and many addressing modes.

C. A CPU of RISC architecture has a large number of registers.

D. In CISC, they are implemented using the hardwire method.

D

6. Which one is the purpose of cache?

A. Speed up the memory access B. Expand the size of memory

C. Add the number of registers in CPU D. Easy to store data or instructions

A

7. Which instruction is wrong? ( )

A. MOV AL, [DI] B. OUT DX, AL

C. MOV [DI], [BX] D. MOV DI, BX

C

8. A byte is being transferred on the D0-D7 data bus from an even-address location, the status of A0 and BHE are ( )

A. A0=0, BHE=0 B. A0=0, BHE=1 C. A0=1, BHE=0 D. A0=1, BHE=1

B

9. DATA1 DB 5 DUP (0, FFH, 2 DUP (1, 0, 0)), the size of DATA1 is ( ).

A.40 B. 20 C. 13 D. 35

A

10. For a special RAM chip, the organization is 1024 x 16, the total number of address pins and data pins is ( ).

A. 14 B.26 C. 25 D. 16

B

Part II True or Fault (1 points for each question, 10 points total)

1. Control memory to hold all the data and procedures. (F)

2. An arithmetic right shift to maintain the highest unchanged, but the logical right shift the highest complement of 0. (T)

3. Port and interfaces have the same concepts, both can be implemented in the same way. (F)

4. In instruction-level pipelining, all hardware units have common control logic.

(F)

5. The main parts of CPU are ALU, Register and Control unit. (T)

6. To ensure the integrity of the contents of ROM, the parity bit is used . (F)

7. No bus can serve two masters at the same time. (T)

8. In 8086, physical address is the 20-bit address, logical address can be consists of 16-bit segment value, and 16-bit offset address . (T)

9. CISC is complete instruction set computer. (F)

10. Accessing cache memory by CPU is faster than accessing main memory or register. (F)

Part III Answer the following questions. (22 points)

1. (5 points) Find the INT type number assigned to IR0 and IR7 if IR3 is assigned INT 1BH.

IR0 will have the INT 18H, and IR7 will have the INT 1FH.

2. (5 points) Give variables that affect the bus bandwidth.

The data bus width and bus cycle time.

3. (5points) Which control signal is activated during the memory read cycle? Which control signal is activated during the I/O write cycle?

MEMR is activated during the memory read cycle. IOW is activated during the I/O write cycle.

4. (7 points) Express the following number in IEEE 754 32-bit floating-point format.

1664.75

$1664.75=11010000000.11=1.101000000011 \times 2^{10}$

The sign bit is 0

Exponent bits 10+127=137=1000 1001B

Mantissa bits 10100000 00110000 0000000

IEEE 754 32-bit Express is

0 10001001 10100000 00110000 0000000

Part IV Write a program to find the numbers of one in a 16-bit word stored in DS:0200H and DS:0201H. (10 points)

```
STSEG SEGMENT
  DB 32 DUP(?)
STSEG ENDS
DTSEG SEGMENT
  NUM   DW 0000H
  COUNT DW ?
DESEG ENDS
CODE SEGMENT
     ASSUME CS:CODE, DS:DTSEG, SS :STSEG
  START   PROC FAR
          MOV AX, DTSEG
          MOV DS, AX
          MOV CX, 16
          CLC
          SUB  BX, BX
          MOV DI, 0200H
          MOV AX, WORD PTR [DI]
     BACK: SHR AX, 1
          JNC END_LOOP
          INC BX
    END_LOOP: LOOP BACK
          MOV COUNT, BX
          MOV AH, 4CH
          INT 21H
START    ENDP
CODE ENDS
      END START
```

Part V The following program contains some errors. Fix the errors and make the program run correctly. (8 points)

```
  TITLE  Transfers of 6 bytes of data
   .MODEL SMALL
   .STACK 32
   .DATA
      ORG 10H
      DATA_IN   DB  25H, 4FH, 85H, FAH, 2BH, C4H
      ORG 28H
      COPY    DB  6 DUP(?)
   .CODE
MAIN:  PROC FAR
    MOV  AX, DATA
    MOV DS, AX
    CALL START
     MOV AH, 4CH
     INT 21H
     ENDP
START  PROC
    MOV SI, offset DATA_IN
    MOV DI, offset COPY
    MOV CX, 06H
LOOP1  MOV [DI], [SI]
       INC SI
       INC DI
       DEC CX
       JNZ LOOP1
START ENDP
     END START
```

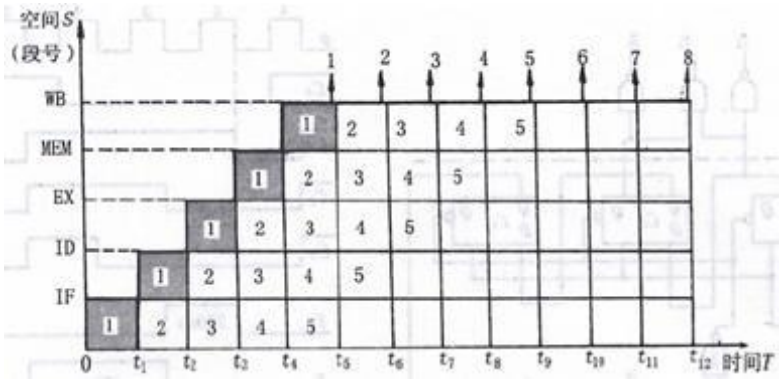
TITLE Transfers of 6 bytes of data

```
    .MODEL SMALL
    .STACK 32
    .DATA
       ORG 10H
       DATA_IN   DB  25H, 4FH, 85H, 0FAH, 2BH, 0C4H
       ORG 28H
       COPY    DB  6DUP(?)
    .CODE
MAIN  PROC FAR
     MOV  AX, @DATA
     MOV DS, AX
     CALL START
      MOV AH, 4CH
      INT 21H
MAIN ENDP
START  PROC
     MOV SI, offset DATA_IN
     MOV DI, offset COPY
     MOV CX, 06H
LOOP1:  MOV AL, [SI]
        MOV [DI], AL
        INC SI
        INC DI
        DEC CX
        JNZ LOOP1
     RET
START ENDP
      END MAIN
```

Part VI Suppose the fetch-decode-execute cycle can be broken into the five "mini-steps", fetch (IF) and decoding (ID), execute (EX), memory (MEM) Writebacks (WB), a total of 12 instructions entered the pipeline.

1. Show the space-time diagram assuming the clock time is 100ns.
2. Calculate the throughput rate and speedup ratio. (10 points)

Solution:



The throughput rate is 12/[(12+5-1)100ns]=7500000

The speedup ratio is 12×5/(5+11)=60/16=3.75

Part VII Suppose that CPU has 16-bit address pins and 8-bit data pins, access the memory when $\overline{MREQ}$ is active low, $\overline{WR}$ is control signal (low for writing/ high for reading). Using this CPU and RAM (1K x 4, 2K x 8, 4K x 8), ROM (2K x 8, 4K x 4, 8K x 8), 74LS138, and several logic gates to build the system satisfy the following requests:

The first 4K is set aside for system program;

4096~16383 is set aside for user program.

Which chip and how many chips will be used to build the system? Show the diagram. (10 points)

Solution:

Two chips of ROM (4K x 4)

Three chips of RAM (4K x 8)

ROM 0000H~0FFFH

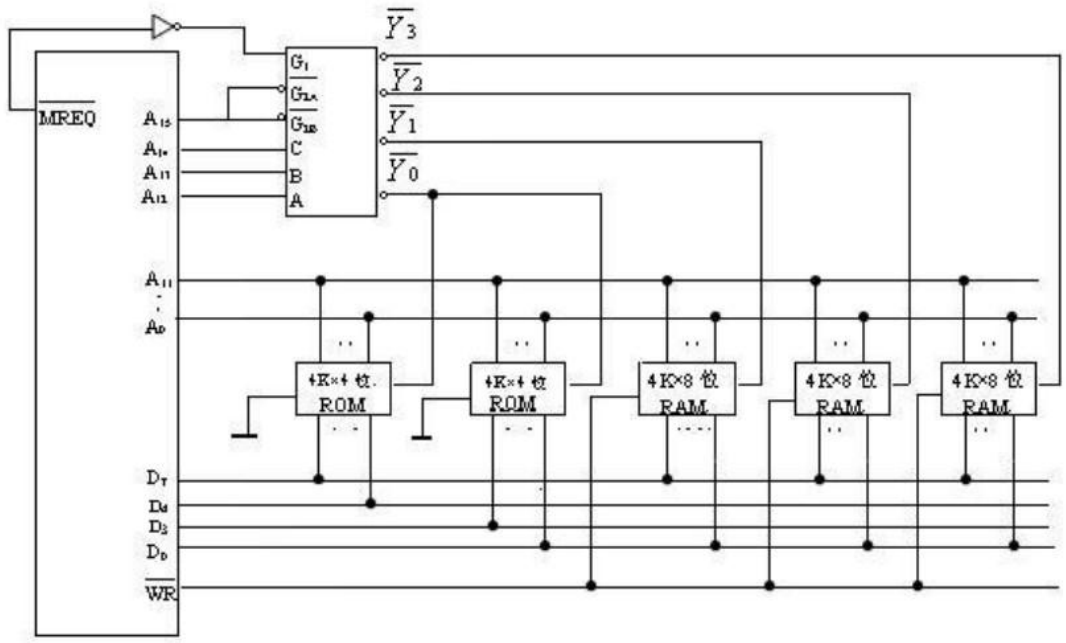
0000 0000 0000 0000 ~0000 1111 1111 1111

RAM 1000H~3FFFH

0001 0000 0000 0000 ~ 0001 1111 1111 1111

0010 0000 0000 0000 ~ 0010 1111 1111 1111

0011 0000 0000 0000 ~ 0011 1111 1111 1111



Part VIII Write a program in Assembly language to get a byte of data from PA of 8255, convert it to ASCII bytes, and store in registers CL, AH, and AL. The port address of PA is 310H. For example, an input of FFH will show as 255. (Note: FF in binary becomes 32 35 35 in ASCII).

(10 point)

Solution:

```
MOV  AL, 90H     ;  PA=IN
MOV  DX, 313H
OUT DX, AL
MOV DX, 310H
```

```
IN AL, DX

MOV BL,10

SUB AH,AH

DIV BL

MOV CL, AH

SUB AH,AH

DIV BL

OR AX, 3030H

OR CL, 30H
```

Appendix

8255Control word

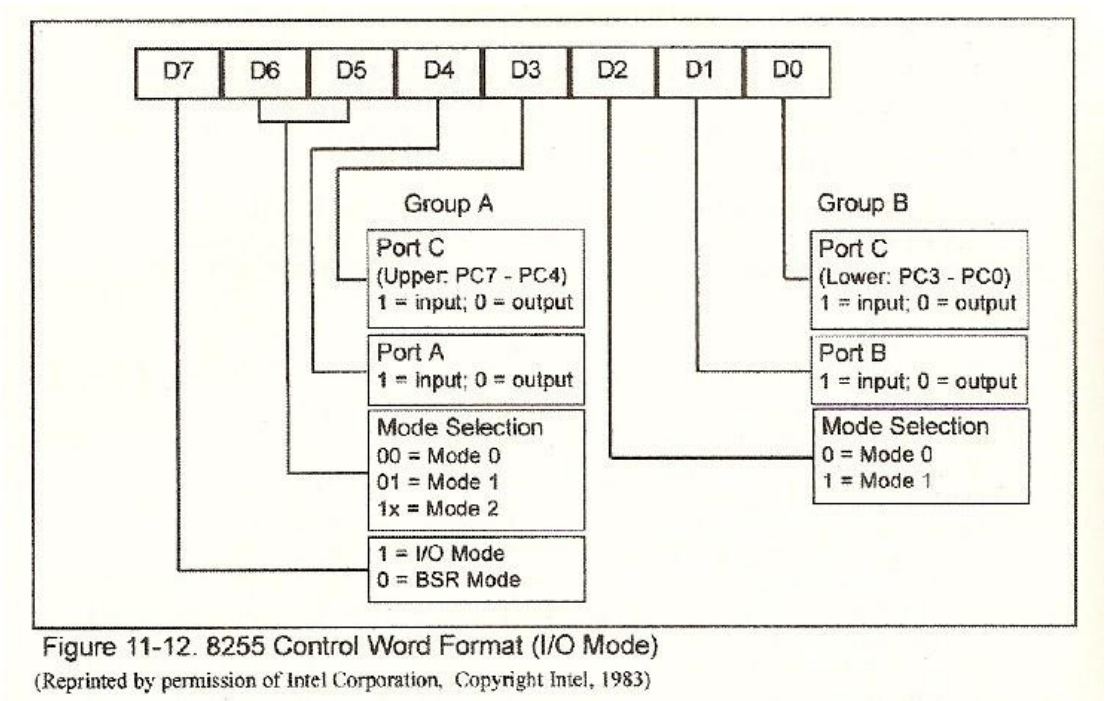


Figure 11-12. 8255 Control Word Format (I/O Mode)

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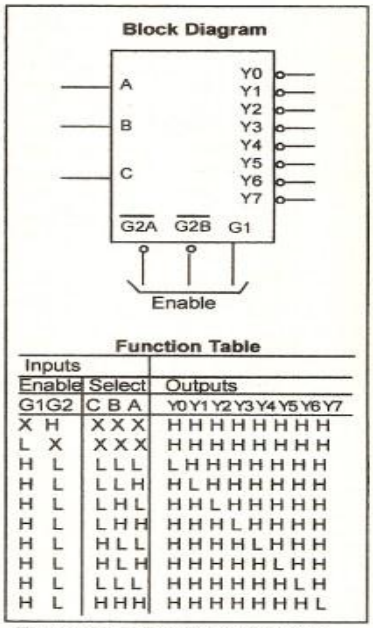
74LS138



Function Table

Inputs				Outputs							
Enable		Select									
G1	G2	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	L	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Figure 11-8. 74LS138 Decoder
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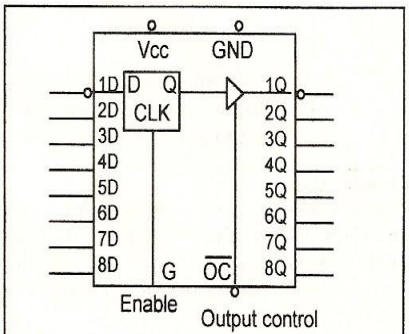

Function Table

Output Control	Enable G	Enable D	Output
L	H	H	H
L	H	L	L
L	L	X	Q0
H	X	X	Z

Figure 11-1. 74LS373 D Latch
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