中山大学软件学院 2008 级软件工程专业(2009-2)

《计算机原理与接口技术》期末试题试卷(A)

(考试形式： 闭卷 考试时间：2 小时)

警示 **《中山大学授予学士学位工作细则》第六条**

考试作弊不授予学士学位

方向：_____ 姓名：_____ 学号：_____成绩：_____

注意：答案一定要写在答题纸上，写在本试卷中不给分。本试卷要和答卷一起交回。

Part I Fill in blanks（20 points）

1、(4 points) The 8086 is a microprocessor with a ___ bit data internally and ___ bit externally. 8088 has an ___ bit data internally and a ___ bit data externally.

16、16、16、8

2、(5 point) Assume BX=7830H and CF=1，after the execution of "ADC BX，87CFH", then BX=_____, CF=_____,ZF=_____,OF=_____,SF=_____.

0000H、1、1、0、0

3、(1 point) Assume SP=2000H，find the stack pointer after the execution of "PUSH AX". SP=_____.

1FFEH

4、(2 points) If 8259 is used with an 8088 CPU, the ICW2 is 70H，the interrupt of IR6 is _____H, the interrupt vector table location for IR6 is _____H.

76H、0000：01D8H

5、(2 points) The last instruction in the ISR is _____, whereas the last instruction in a subroutine is _____.

IRET, RET

6、(2 points) There are three kinds of methods on which CPU accesses I/O,they are querry, _____ and_____.

Interpret, DMA

7、(3 points) In the execution of "OUT DX，AL" instruction，$M/\overline{IO}$ is _____，

$\overline{RD}$ is _____，$\overline{WR}$ is _____.

Low, high, low

8、(1 points) INTR is an active-high level-triggered input signal, receive the _____.

The interrupt request from the 8259 interrupt controller chip.

Part II Answer the following questions.（15 points）

1、**(7 points)What, if anything, is wrong with "MOV AL, [BX] [SI]" and "MOV [BX], [DI]" instruction?**

MOV [BX],[DI] is wrong, Memory to memory data transfers are not allowed.

MOV AL, [BX] [SI] is correct, it just uses an alternative addressing style.

2、**(8 points)Reset the carry flag in three or more modes, state the purpose of the carry flag.**

```
CLC
XOR AX, AX
SUB AX, AX
```

This flag is set wherever there is a carry out, either from D7 after an 8-bit data operation, or from D15 after a 16-bit data operation.

Part III Choose the best answer from the choices.（20 分）

1、**(2 point)The purpose of SP is ( )**

A. Saving the location of the next instruction.

B. Saving the memory address which CPU will access.

C. points at the current memory location used for the top of the stack.

D. points at the current memory location used for the bottom of the stack.

C

2、**(2 points) If the physical address is 25680H，the incorrect logic address is ( ).**

A. 5680H:2000H B. 2568H：0000H

C. 2560H:0080H　　D. 2500H: 0680H

A

3、 (2 points) When $\overline{BHE}$ = 1， and A0=0 in 8086, then ( ) .

A. transfer 8 bits information in even address.

B. transfer 16 bits information in even address.

C. transfer 8 bits information in odd address.

D. transfer 16 bits information in odd address.

A

4、(2 points) Which one is wrong?

A. IN AL， DX　　B. IN DX， AX

C. IN AX， DX　　D. OUT DX， AL

B

5、(2 points)In instruction "MOV CX, 1245H" , where is the location for source operand?

A. DS：1245H　　B. In the instruction

C. In register　　D. None of the above

B

6、(2 points)The "OUT" instruction means ( ) .

A. I/O write operation　　B. I/O read operation

C. Memory write operation　　D. Memory read operation

A

7、(2 points) The CPU finishes the present ( ) before it responds with HLDA.

A. procedure　　B. instruction

C. clock period　　D. bus cycle

D

8、(2 points) NMI can not be invoked by ( )

A. 8087 interrupt request　　B. I/O channel check

C. RAM parity check　　D. real-time clock

D

9、(2 points) DA1 DB 4 DUP (0, 3 DUP((1,0)) , the size of DA1 is ( ) .

A. 4 B. 8 C. 16 D. 28

D

10、(2 points) Which one is incorrect?

A. 8237 can be in control status, can provide MEMR/MEMW, IOW/IOR signals.

B. 8237 needs 16 port addresses provided by A0~A3

C. 8237can be used in cascaded mode

D. Data transferring between I/O and 8088 register can be realized in 8237 control status.

D

Part IV Write a program to reset the TF, D8 is TF in 16 bits flag register.（7 points）

```
PUSHF
POP AX
AND AX, FEFFH
PUSH AX
POPF
```

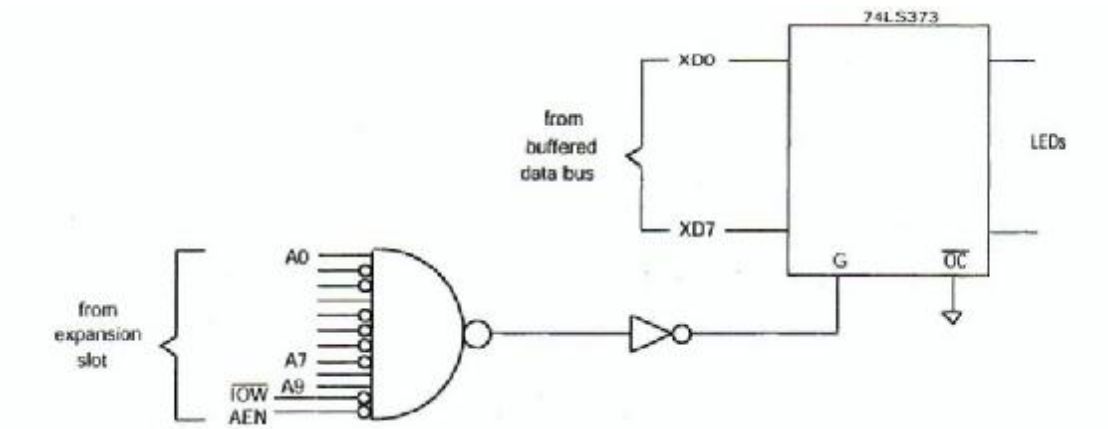
Part V Write a program that finds the number of ones in a 16-bit word.（8 points）

```
STSEG SEGMENT
  DB 32 DUP(?)
STSEG ENDS
DTSEG SEGMENT
  NUM   DW 0000H
  COUNT DW ?
DESEG ENDS
CODE SEGMENT
    ASSUME CS:CODE, DS:DTSEG, SS :STSEG
  START   PROC FAR
```

```
        MOV AX, DTSEG
        MOV DS, AX
        MOV CX, 16
        CLC
        SUB  BX, BX
        MOV AX, NUM
    BACK: SHR AX, 1
        JNC END_LOOP
        INC BX
  END_LOOP: LOOP BACK
        MOV COUNT, BX
        MOV AH, 4CH
        INT 21H
START    ENDP
CODE ENDS
      END START
```

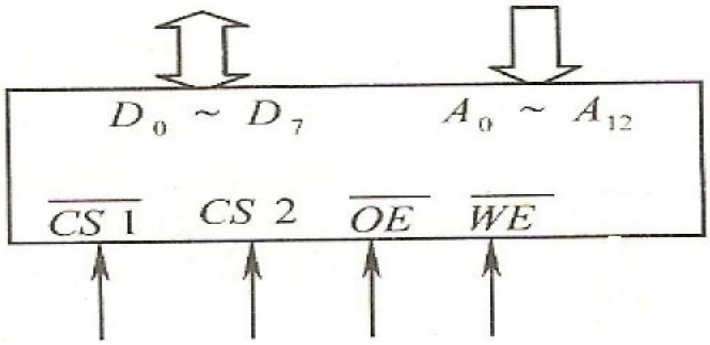
Part VI　Show the circuit connection to the PC bus for the "MOV DX, 309H" and "OUT DX, AL" instructions. Use simple logic gates 74LS373. (10points)

The address decoder is



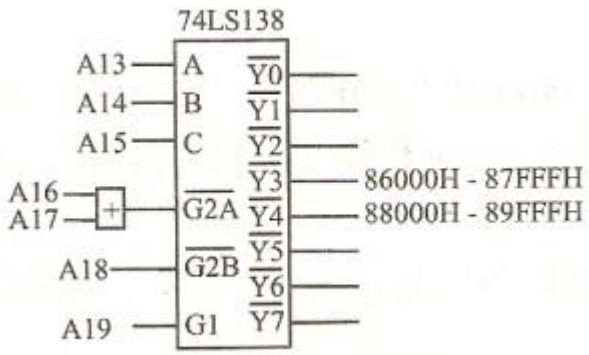
Part VII　Draw a block diagram for the 8088 minimum mode connection to the 74LS373,

74LS245, 74LS138 and memories shown in the figure. The starting address of the memory is 86000H, the size of memory is 16KB. （10 分）

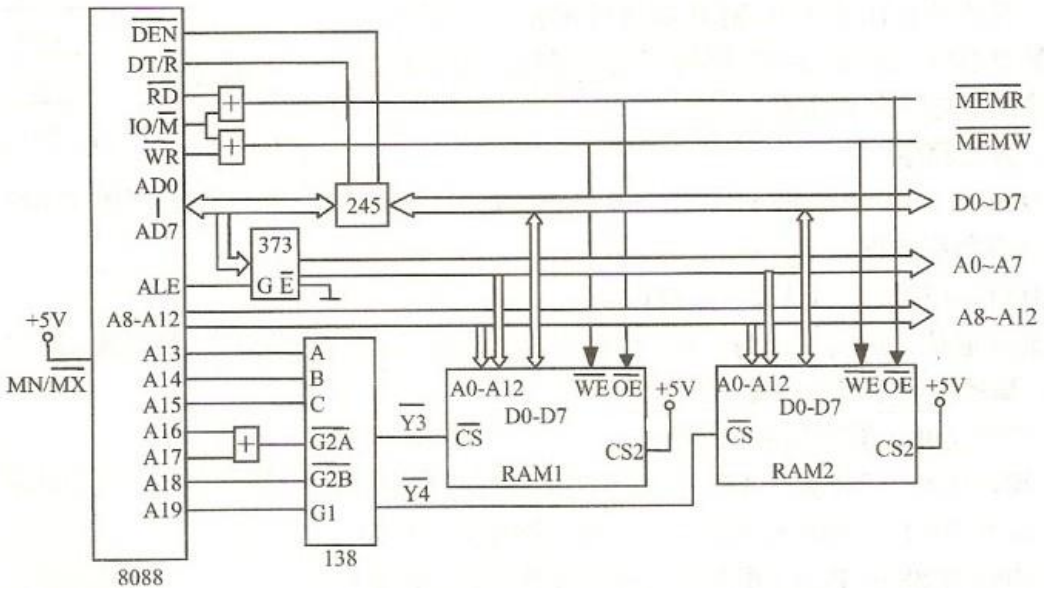


2^{13}=8KB, two memory chips will be needed. The address of one chip is 86000H - 87FFFH, the other is 88000H`- 89FFFH.

The address decoder is



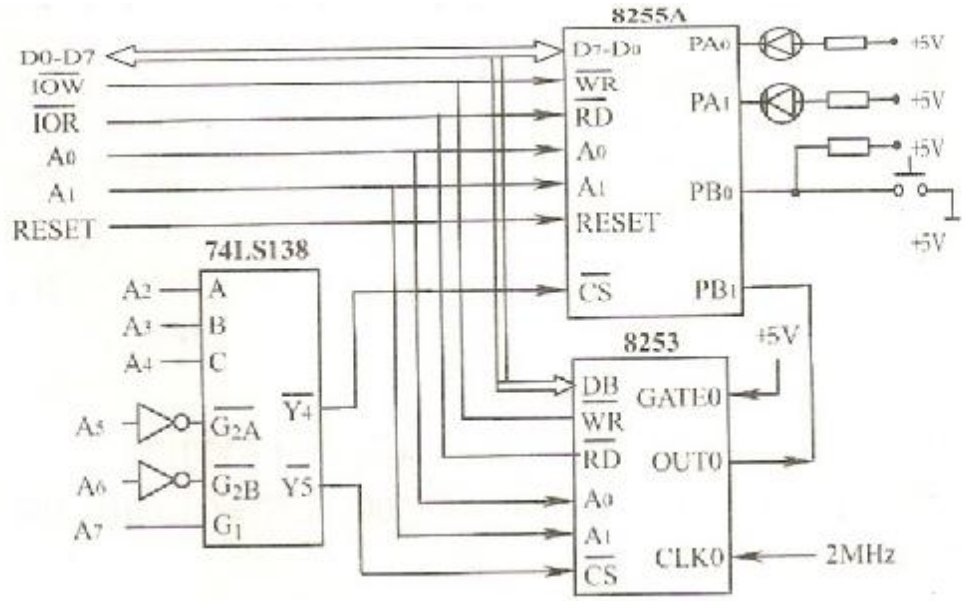
The block diagram is



Part VIII The following figure shows an interfacing circuit, PA is configured as output to lighten the two LEDs in turn, each LED will be turned on 5ms. PB is configured as input to receive the control signal and clock from 8253. When the switch is on, the procedure will exit. The 8253 chip controls the display time.

Find the port address of 8255 and 8237 chips.

Write a program to complete the function. (10points)



The port addresses of 8255 are F0~F3H

The port addresses of 8253 are F4~F7H

The clk0 of 8253 is divided by 20000, 2MHz/20000=100Hz, t=1/100Hz=10ms.

```
CODE SEGMENT
        ASSUME      CS:CODE
START : MOV AL, 36H             ; count 0, mode 3, Binary
            OUT     0F7H, AL
            MOV AX, 20000
            OUT 0F4H, AL        ; send the low byte
            MOV AL, AH
            OUT 0F4H, AL        ; send the high byte
            MOV AL, 82H          ; PA=output, PB=input
            OUT     0F3H, AL
LP1:        IN     AL, 0F1H
            AND AL, 02H
            JNZ LP1
            MOV AL, 0FEH
            OUT 0F0H, AL
LP2:        IN     AL, 0F1H
            AND AL, 02H
            JZ LP2
            MOV AL, 0FDH
            OUT     0F0H, AL
            IN     AL, 0F1H
            AND AL, 01H
            JNZ LP1
            MOV AH, 4CH
            INT 21H
CODE ENDS
          END START
```

Appendix

8255 control word

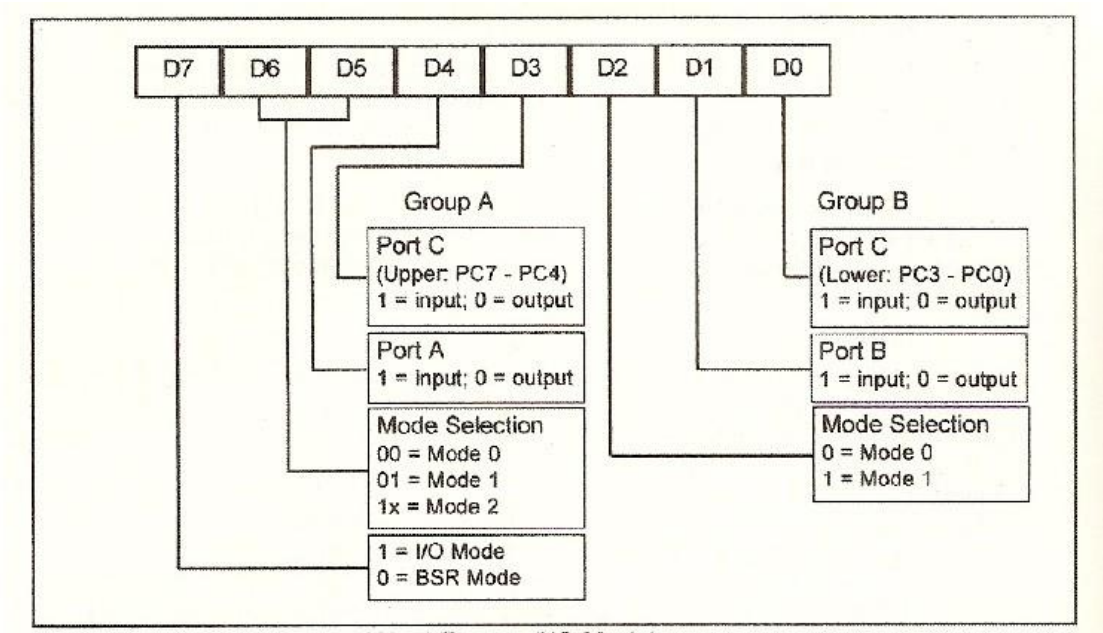


Figure 11-12. 8255 Control Word Format (I/O Mode)

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825 3control word

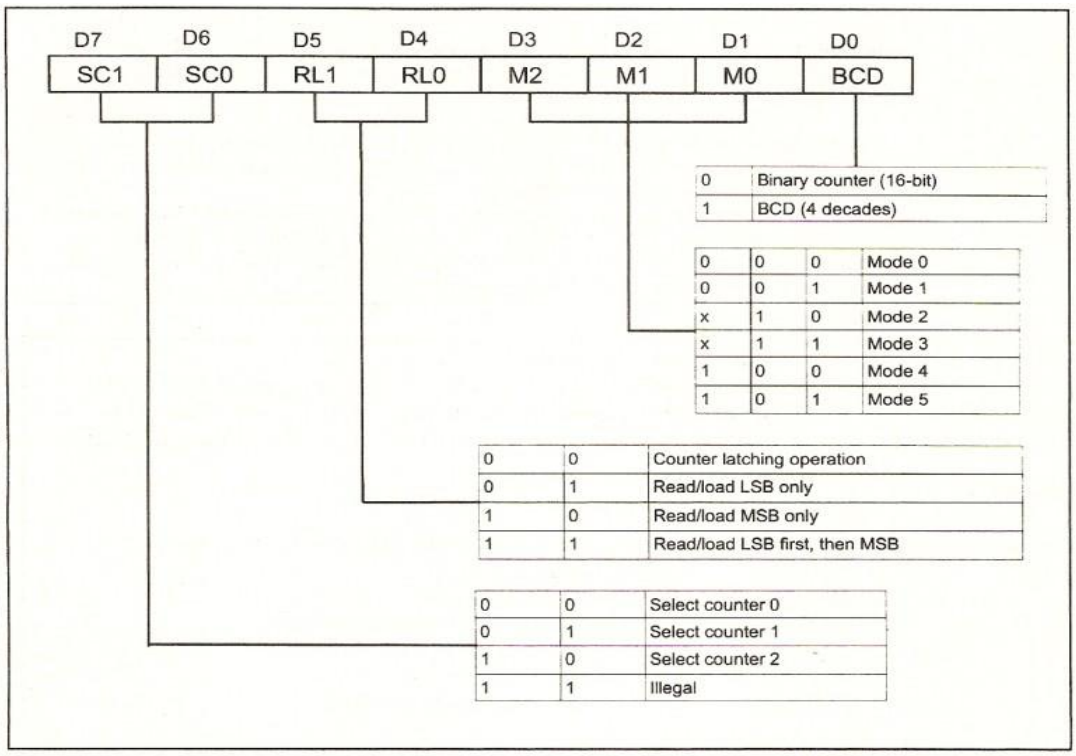

Figure 13-2. 8253/54 Control Word Format

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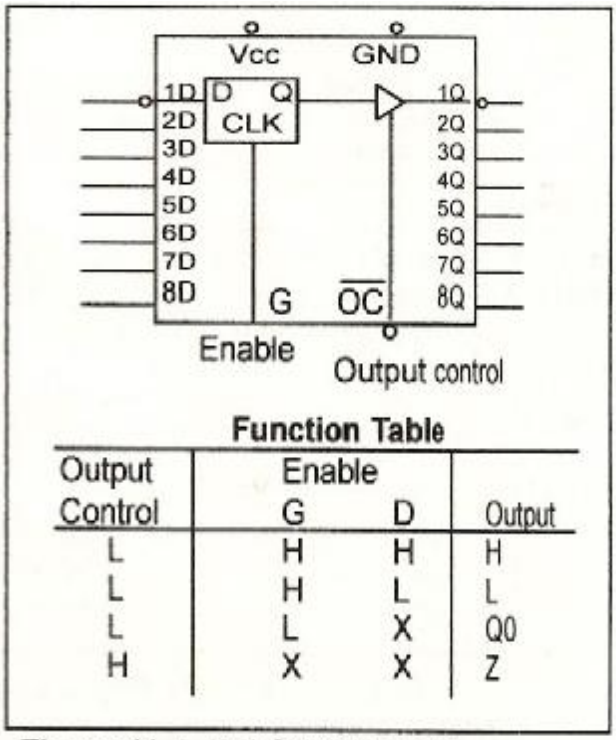
74LS373



Function Table

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q0
H	X	X	Z

Figure 11-1. 74LS373 D Latch
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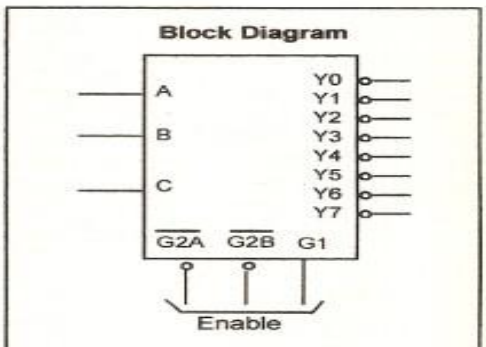
74LS138



Function Table

Inputs Enable G1 G2	Select C B A	Outputs Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
X H	X X X	H H H H H H H H
L X	X X X	H H H H H H H H
H L	L L L	L H H H H H H H
H L	L L H	H L H H H H H H
H L	L H L	H H L H H H H H
H L	L H H	H H H L H H H H
H L	H L L	H H H H L H H H
H L	H L H	H H H H H L H H
H L	L L L	H H H H H H L H
H L	H H H	H H H H H H H L

Figure 11-8. 74LS138 Decoder
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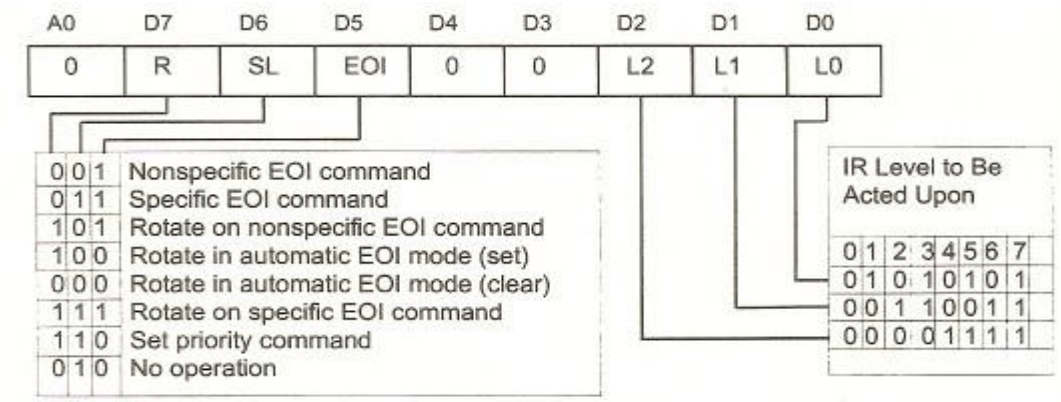
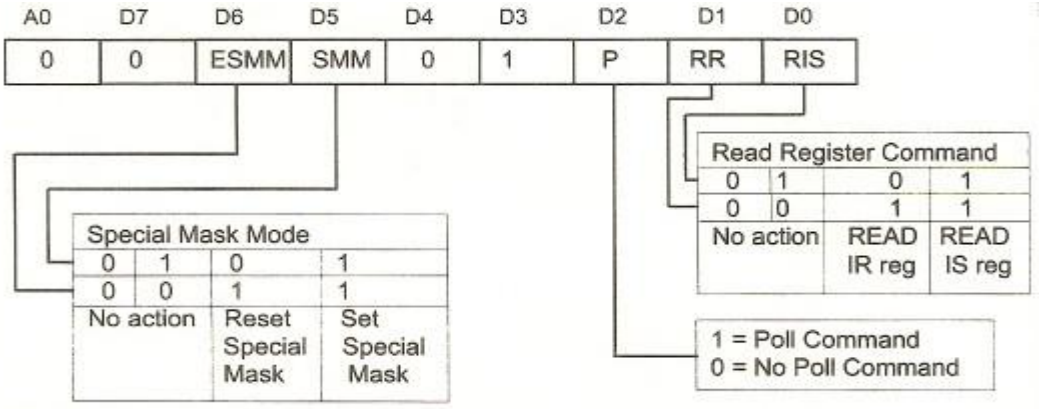
8259 control word

OCW2



OCW3



ICW1

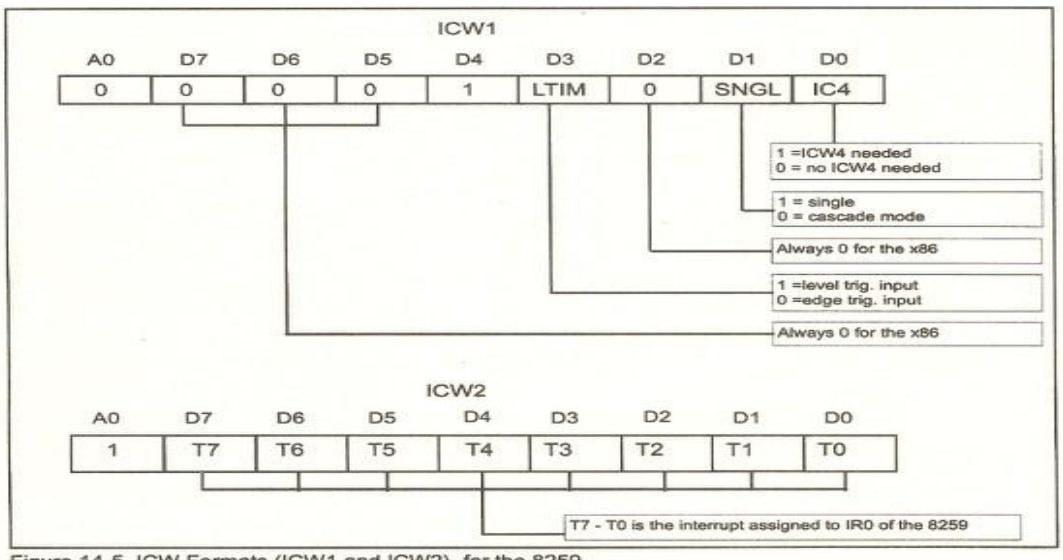


Figure 14-5. ICW Formats (ICW1 and ICW2) for the 8259