中山大学软件学院 2010 级软件工程专业(2011 学年春季学期)

《计算机组成原理与接口技术》期末考试试卷

答案(B)

(考试形式： 闭卷 考试时间：2 小时)

警示

《中山大学授予学士学位工作细则》第六条

考试作弊不授予学士学位

方向：_____ 姓名：_____ 学号：_____成绩：_____

出卷：_____邓革、李国桢_____ 审核：_____

注意：答案一定要写在答题纸上，写在本试卷中不给分。本试卷要和答卷一起交回。

Part I Choose the best answer from the choices. (2 points for each question, 20 points total)

1. Given x=-0.1010, the representation of 1.0110 is ( ).

   A. Sign-Magnitude Representation B. One's Complement Representation

   C. Two's Complement Representation D. Floating-Point Representation

   C

2. Which one is independent of the hit ratio of cache?

   A. Access time of memory B. The size of block

   C. Cache organization D. The size of cache

   A

3. Which of the following operations do not exist for ADD instruction in RISC?

   A. memory to register B. register to register

   C. immediate to register D. either B or C

   A

4. In the instruction "OUT DX, AL", the port address is:

   A. 8 bits B. 16 bits C. either A or B D. none of the above

   C

5. The main components in CPU are ( ).

A. Control Unit, ALU, Memory B. Control Unit, Register, Memory

C. Control Unit, ALU, Cache D. Instruction Pointer, I/O module

C

6. Microinstructions are placed in ( )

A. memory controller B. main memory

C. control memory D. Cache

C

7. A byte is being transferred on the D8-D15 data bus from an odd-address location, the status of A0 and BHE are ( )

A. A0=0, BHE=0 B. A0=0, BHE=1 C. A0=1, BHE=0 D. A0=1, BHE=1

C

8. For a special RAM chip, the organization is 256 x 4, the total number of address pins and data pins is ( ).

A. 10 B.12 C. 16 D. 8

B

9. Computer organization is a computer architecture ( ) implementation。

A. physics B. . logical C. circuit D. simulate

B

10. DATA1 DB 5 DUP (0, 2 DUP (1, 0, 0)), the size of DATA1 is ( ).

A.35 B. 30 C. 20 D. 16

A

Part II True or Fault (1 points for each question, 10 points total)

1. The last instruction in the ISR is IRET, whereas the last instruction in a FAR subroutine is RET. (T)

2. While CISC instructions are variable sizes, RISC instructions are all the same size. (T)

3. To ensure the integrity of the contents of RAM, the check sum is used . (F)

4. The more address pins, the more memory locations are inside the chip. The more

data pins, the more each location inside the chip will hold. (T)

5. IP(instruction pointer) register is available in low-byte and high-byte formats. (F)

6. Port and interfaces have the same concepts, both can be implemented in the same way. (F)

7. In 8086, physical address is the 20-bit address, logical address can be consists of 16-bit segment value, and 16-bit offset address . (T)

8. The NMI has a higher priority than INTR. (T)

9. While memory contains both code and data, ports contain data only. (T)

10. Memory-mapped I/O uses controls MEMR and MEMW. (T)

Part III Answer the following questions. (22 points)

1. (5 points) How many bytes are used by the interrupt vector table, and why?

1024 bytes, since there are 256 interrupts and each interrupt takes 4 bytes.

2. (5 points) What is the purpose of pseudo-instructions ?

Pseudo-instructions direct the assembler as to how to assemble the program.

3. (5points) Which control signal is activated during the memory write cycle? Which control signal is activated during the I/O read cycle?

MEMW is activated during the memory read cycle. IOR is activated during the I/O write cycle.

4. (7 points) Express the following number in IEEE 754 32-bit floating-point format.

-138.125

$-138.125=-10001010.001=-1.0001010001 \times 2^{7}$

The sign bit is 1

Exponent bits 7+127=134=1000 0110B

Mantissa bits 00010100 01000000 0000000

IEEE 754 32-bit Express is

1 10000110 00010100 01000000 0000000

Part IV Write a program to find the numbers of zero in a 16-bit word stored in DS:0300

and DS:0301. (10 points)

```
STSEG SEGMENT
  DB 32 DUP(?)
STSEG ENDS
DTSEG SEGMENT
  COUNT DW ?
DESEG ENDS
CODE SEGMENT
     ASSUME CS:CODE, DS:DTSEG, SS :STSEG
  START   PROC FAR
          MOV AX, DTSEG
          MOV DS, AX
          MOV CX, 16
          CLC
          SUB  BX, BX
          MOV DI, 0300H
          MOV AX, WORD PTR [DI]
     BACK: SHR AX, 1
          JC END_LOOP
          INC BX
    END_LOOP: LOOP BACK
          MOV COUNT, BX
          MOV AH, 4CH
          INT 21H
START    ENDP
CODE ENDS
      END START
```

Part V The following program contains some errors. Fix the errors and make the program run correctly. (8 points)

```
    .MODEL SMALL
    .STACK 32
    .DATA
       DATA    DW  234DH, DE6H, 3BC7H, 566AH
       SUM     DW  ?
    .CODE
START: PROC FAR
     MOV  AX, DATA
     MOV DS, AX
     MOV  CX, 04
     MOV BX, 0
     MOV DI, offset DATA
LOOP1:  ADD BX, [DI]
      INC DI
      JNZ LOOP1
      MOV SI, offset RESULT
      MOV [SI], BX
      MOV AH, 4CH
      INT 21H
START ENDP
      END STRT


    .MODEL SMALL
    .STACK 32
    .DATA
       DATA1    DW  234DH, 0DE6H, 3BC7H, 566AH
       RESULT     DW  ?
    .CODE
START PROC FAR
     MOV  AX, @DATA
```

```
    MOV DS, AX
    MOV  CX, 04
    MOV BX, 0
    MOV DI, offset DATA
LOOP1  ADD BX, [DI]
     INC DI
     DEC CX
     JNZ LOOP1
     MOV SI, offset RESULT
     MOV [SI], BX
     MOV AH, 4CH
     INT 21H
START ENDP
     END START
```

Part VI A computer has 32-bit instructions and 12-bit addresses. Suppose there are 250 2-address instructions. How many 1-address instructions can be formulated? Explain your answer. (10 points)

Solution:

6×2^{12}

1111 1010 0000 0000 0000 xxxx xxxx xxxx

1111 1010 1111 1111 1111 xxxx xxxx xxxx

1111 1011 0000 0000 0000 xxxx xxxx xxxx

1111 1011 1111 1111 1111 xxxx xxxx xxxx

1111 1100 0000 0000 0000 xxxx xxxx xxxx

1111 1100 1111 1111 1111 xxxx xxxx xxxx

1111 1101 0000 0000 0000 xxxx xxxx xxxx

1111 1101 1111 1111 1111 xxxx xxxx xxxx

1111 1110 0000 0000 0000 xxxx xxxx xxxx

1111 1110 1111 1111 1111 xxxx xxxx xxxx

1111 1111 0000 0000 0000 xxxx xxxx xxxx

1111 1111 1111 1111 1111 xxxx xxxx xxxx

Part VII Suppose that CPU has 16-bit address pins and 8-bit data pins, access the memory when $\overline{MREQ}$ is active low, $\overline{WR}$ is control signal (low for writing/ high for reading). Using this CPU and RAM (1K x 4, 2K x 8, 8K x 8, 16k x 1, 4k x 4), ROM (2K x 8, 8K x 8, 32K x 8), 74LS138, and several logic gates to build the system satisfy the following requests:

0~2047 is set aside for system program;

2048~8191 is set aside for user program.

Which chip and how many chips will be used to build the system? Show the diagram. (10 points)

Solution:

One chip of ROM (2K x 8)

Three chips of RAM (2K x 8)

ROM 0000H~0FFFH

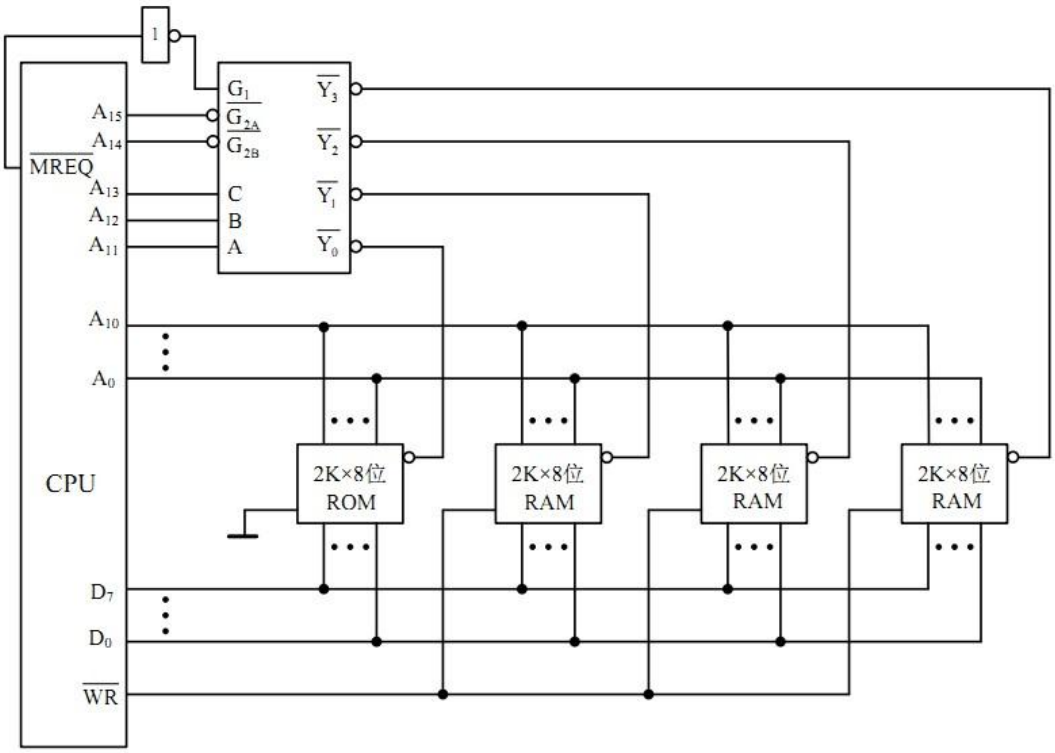
0000 0000 0000 0000 ~0000 0111 1111 1111

RAM 1000H~3FFFH

0000 1000 0000 0000 ~ 0000 1111 1111 1111

0001 0000 0000 0000 ~ 0001 0111 1111 1111

0001 1000 0000 0000 ~ 0001 1111 1111 1111



Part VIII Write a program in Assembly language to get a byte of data from PA of 8255. If D0 of the received byte is 1, then send the data stored in DS:0001H to PB; if D0 of the received byte is 0, then send data stored in DS:0002H to PB. The port address of PA is 310H. (10 point)

Solution:

```
MOV  AL, 90H      ;  PA=IN
MOV  DX, 313H
OUT DX, AL
MOV DX, 310H
IN AL, DX
SHR AL,1
JC LOOP1
MOV AL, [0002H]
MOV DX, 311H
OUT DX, AL
JMP LOOP2
```

```
LOOP1: MOV AL, [0001H]
       MOV DX, 311H
       OUT DX, AL
LOOP2:
```

Appendix

8255Control word

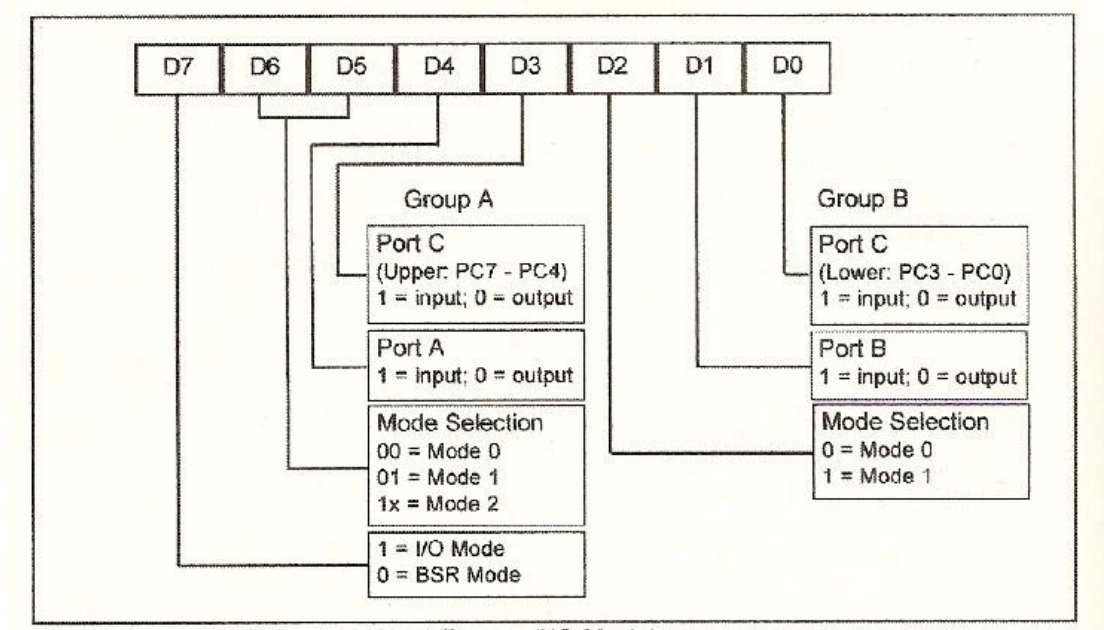


Figure 11-12. 8255 Control Word Format (I/O Mode)

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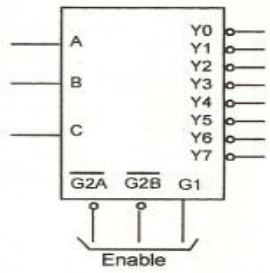
74LS138

Block Diagram



Function Table

Inputs				Outputs							
Enable		Select									
G1	G2	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	L	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Figure 11-8. 74LS138 Decoder