VLSI HW

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1. Functional Verification Using Selected Input Vectors

Table 1： Five representative input combinations of (X, Y, Ci) were applied to verify the functionality of the 3-bit ripple carry adder.

X(X2, X1, X0)	(1,1,1)	(0,0,0)	(0,0,1)	(0,1,0)	(0,1,1)
Y(Y2, Y1, Y0)	(1,1,1)	(0,0,0)	(0,1,0)	(0,1,1)	(1,0,0)
Ci	0	1	0	0	0
Cout(Cout, Ci2, Ci1)	(1,1,1)	(0,0,0)	(0,0,0)	(0,1,0)	(0,0,0)
Sum	(1,1,0)	(0,0,1)	(0,1,1)	(1,0,1)	(1,1,1)

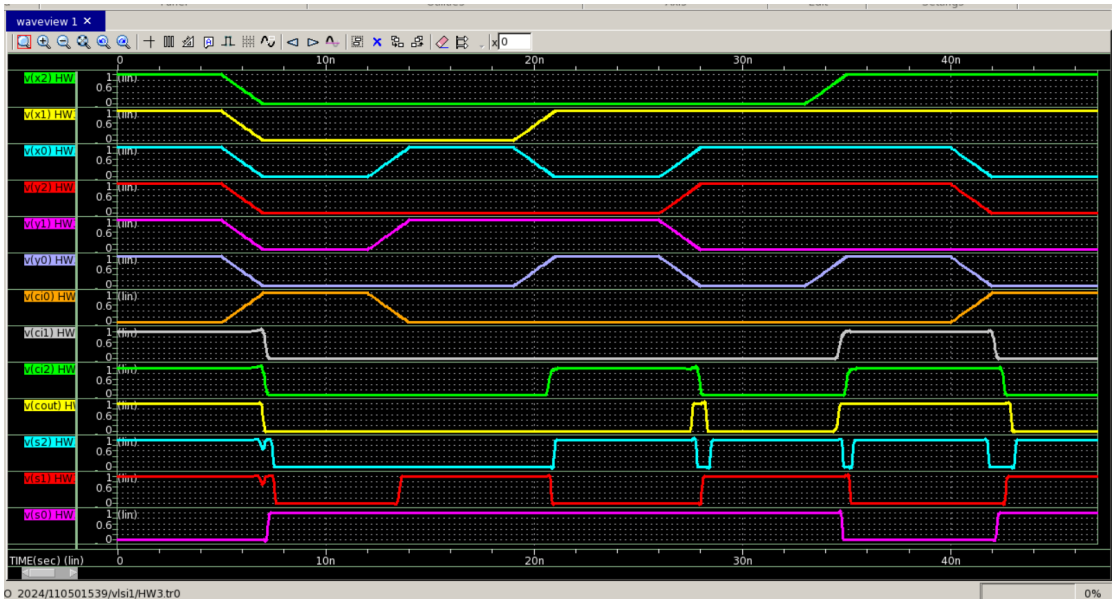

Figure 1：the waveform results for the five selected test cases. From top to bottom, the signals correspond to X2, X1, X0, Y2, Y1, Y0, Ci0, Ci1, Ci2, Cout, S2, S1, S0.

Each test vector was applied for 5 ns, followed by a 2 ns transition period, resulting in a total duration of 7 ns per test case. The final test case required only 5 ns, leading to a total functional simulation time of 33 ns. An additional interval from 33 ns to 47 ns was reserved for worst-case propagation delay verification.

2. Worst-Case Propagation Delay Analysis of the Ripple Carry Adder

To determine the worst-case propagation delay, a single full adder was first analyzed. The inputs (X, Y, Ci) correspond to (ain, bin, cin) in the waveform shown in Figure 2.

The input sequence follows the order listed in Table 2, where each test interval consists of 5 ns of stable input and 2 ns for input transition.

To accurately measure propagation delay, the output of each test case was forced to toggle by inverting the previous output state. In Table 2, only the entries highlighted in red represent valid measurement conditions, while the remaining entries were used to create output transitions.

Table 2：Summarizes all eight possible input combinations tested for a single full adder.

time(ns)	0-5	7-12	14-19	21-26	28-33	35-40	42-47	49-54	56-61	63-68	70-75	77-82	84-89	91-96	98-103	105-110	112-117
ain	0	1	0	1	0	1	1	1	0	1	1	1	1	0	1	1	0
bin	0	1	0	1	1	1	0	0	1	0	0	0	1	0	1	1	0
cin	0	0	1	0	0	0	0	0	1	0	1	0	0	0	1	1	0
cou	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	1	0
sum	0	0	1	0	1	0	1	1	0	1	0	1	0	0	1	1	0

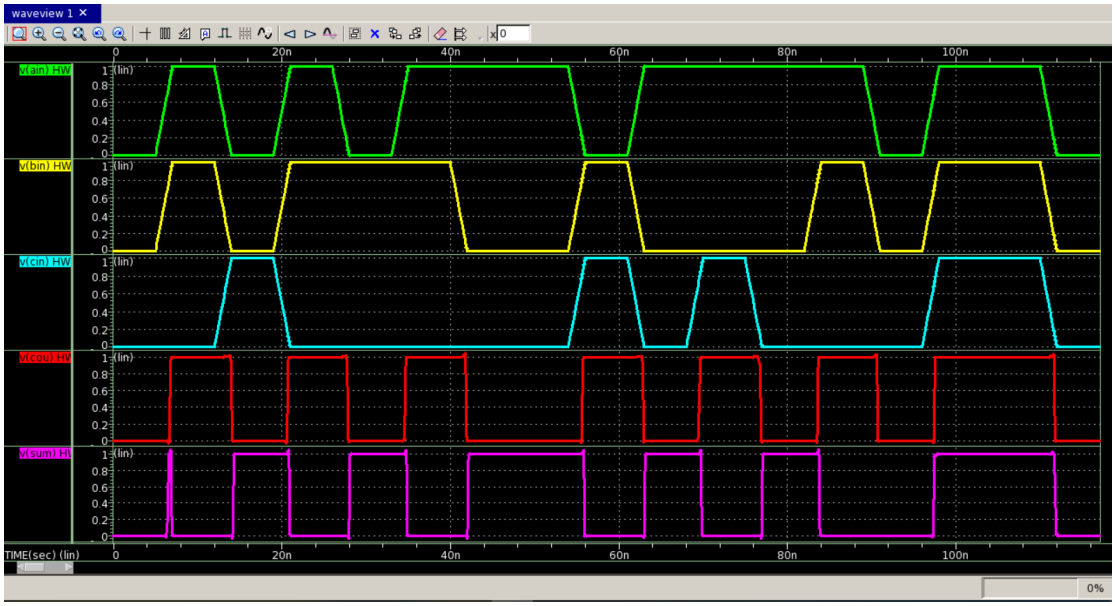

Figure 2：Waveforms used for propagation delay measurement. From top to bottom, the signals correspond toain, bin, cin, cou, sum.

```
y
 tdelay=   1.2220n  targ=  14.2220n   trig=  13.0000n
 tdelay1=   1.0173n  targ=  28.0173n   trig=  27.0000n
 tdelay2=   1.0733n  targ=  42.0733n   trig=  41.0000n
 tdelay3= 885.4790p  targ=  55.8855n   trig=  55.0000n
 tdelay4= 802.6349p  targ=  69.8026n   trig=  69.0000n
 tdelay5= 806.1730p  targ=  83.8062n   trig=  83.0000n
 tdelay6= 379.6536p  targ=  97.3797n   trig=  97.0000n
 tdelay7= 806.8425p  targ= 111.8068n   trig= 111.0000n
 tdelay8=   1.0267n  targ=  14.0267n   trig=  13.0000n
 tdelay9= 816.5509p  targ=  27.8166n   trig=  27.0000n
 tdelay10= 868.8957p  targ=  41.8689n   trig=  41.0000n
 tdelay11= 645.4256p  targ=  55.6454n   trig=  55.0000n
 tdelay12= 580.6965p  targ=  69.5807n   trig=  69.0000n
 tdelay13= 604.9642p  targ=  83.6050n   trig=  83.0000n
 tdelay14= 468.5418p  targ=  97.4685n   trig=  97.0000n
 tdelay15= 724.0501p  targ= 111.7241n   trig= 111.0000n
```

Figure 3：the delay data extracted from the simulation results. The measured delays(tdelay-tdelay7 correspond to the sum output under the eight input combinations, while tdelay8-tdelay15 correspond to the carry-out output.

The maximum propagation delay for both sum and carry-out occurs in the first input condition, (X, Y, Ci)=(0,0,1) , where the output transitions from (cou, sum)=(1,0) to (0,1).

To construct the worst-case condition for the 3-bit ripple carry adder, this input combination was applied to the least significant bit, while the next two stages used the second-largest delay condition, (X, Y, Ci)=(1,0,0). Under this configuration, the worst-case propagation delay occurs when (X, Y, Ci0) transitions from (7,5,0) to (6,0,1). As shown in Figure 4, the measured worst-case propagation delay is 2.1028 ns.

3. The measured average power consumption

```
y
 pwr=  18.4296u  from=   0.            to=  47.0000n
 tdelay=   2.1028n  targ=  43.1028n   trig=  41.0000n

          ***** job concluded
 ******
 **3bit ripple carry adder
```

Figure 4：3bit adder average power consumption.

The average power consumption of the 3-bit ripple carry adder was measured using the power analysis features provided by HSPICE. Figure 4 shows the simulated power waveform, from which the average power consumption was extracted. The measured average power consumption of the adder is 18.4296 μW.

4.Layout Results

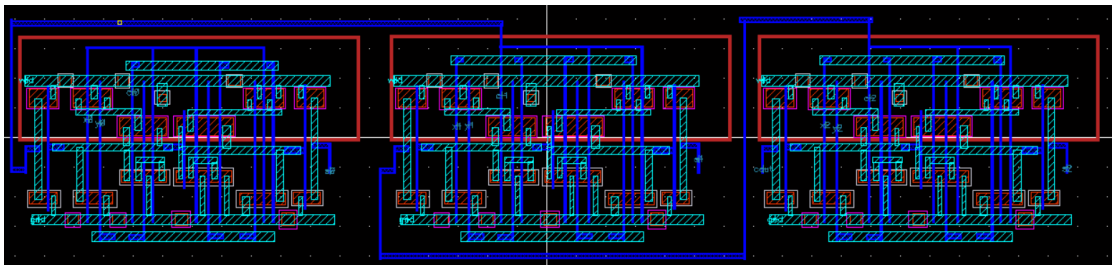

Figure 5：Layout Screenshot.

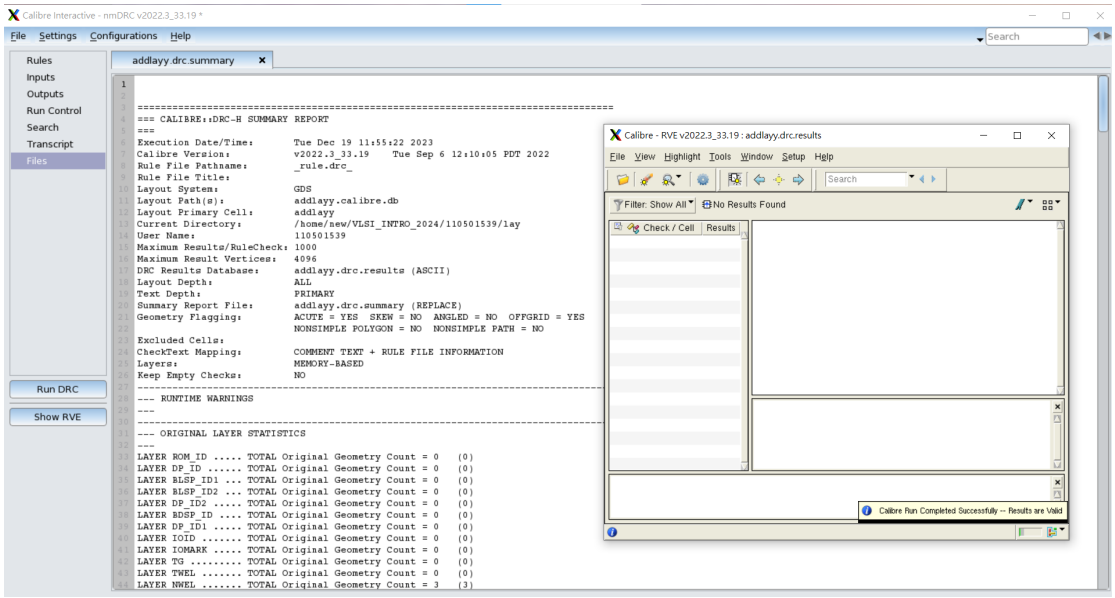

Figure 6：DRC Screenshot.

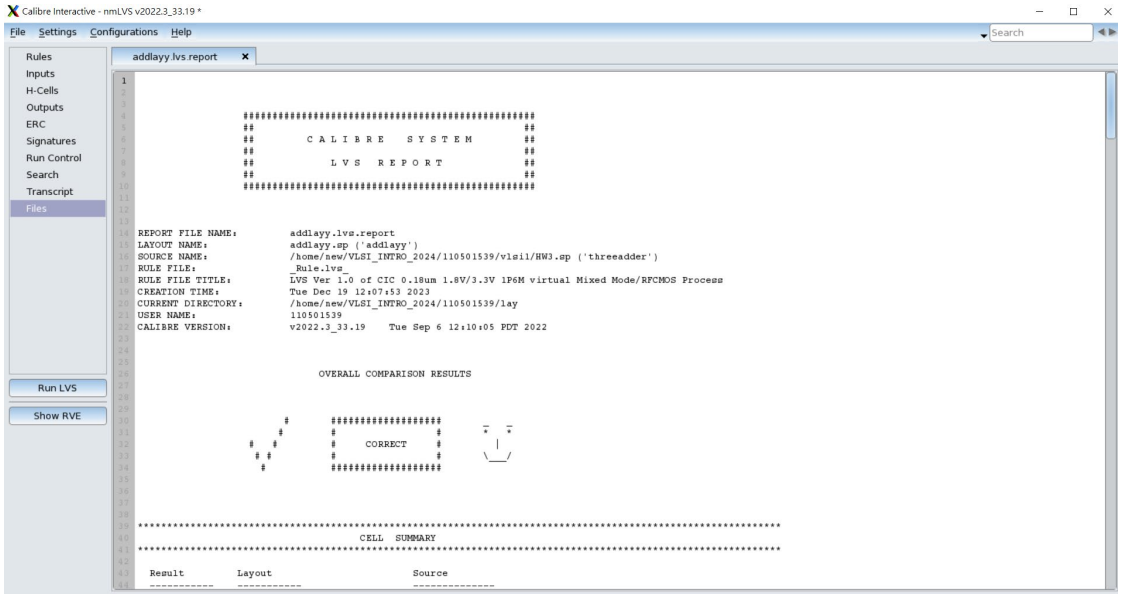

Figure 7：LVS Screenshot 1.

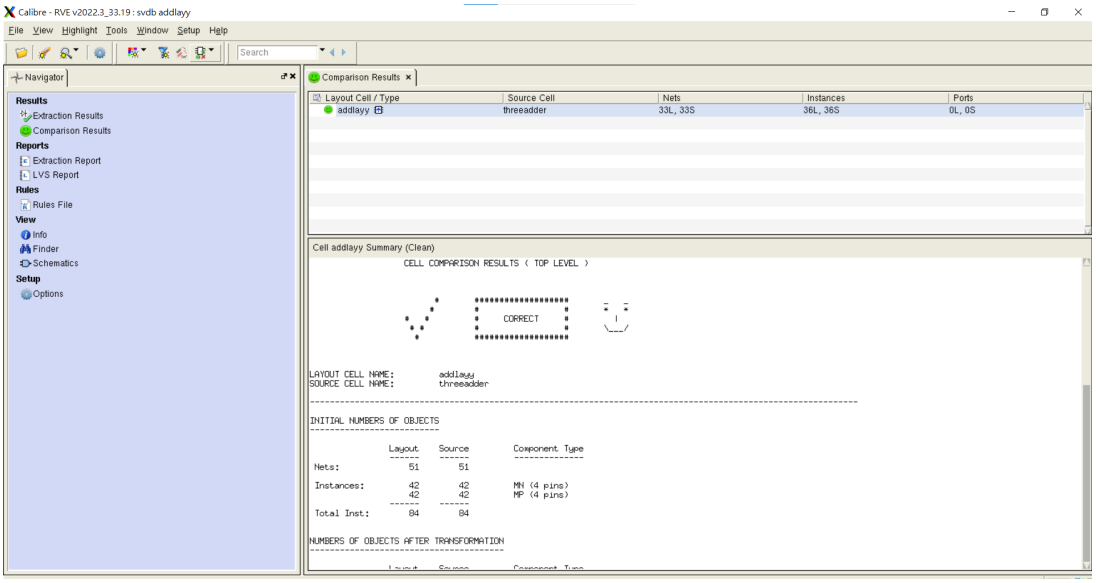

Figure 8：LVS Screenshot 2.

2.Post-sim Waveform analysis

Table 3：Input–output combinations for seven (X, Y, Ci) test cases.

X(X2, X1, X0)	(1,1,1)	(0,0,0)	(0,0,1)	(0,1,0)	(0,1,1)	(1,1,1)	(1,1,0)
Y(Y2, Y1, Y0)	(1,1,1)	(0,0,0)	(0,1,0)	(0,1,1)	(1,0,0)	(1,0,1)	(0,0,0)
Ci	0	1	0	0	0	0	1
Cout(Cout, Ci2, Ci1)	(1,1,1)	(0,0,0)	(0,0,0)	(0,1,0)	(0,0,0)	(1,1,1)	(0,0,0)
Sum	(1,1,0)	(0,0,1)	(0,1,1)	(1,0,1)	(1,1,1)	(1,0,0)	(1,1,1)

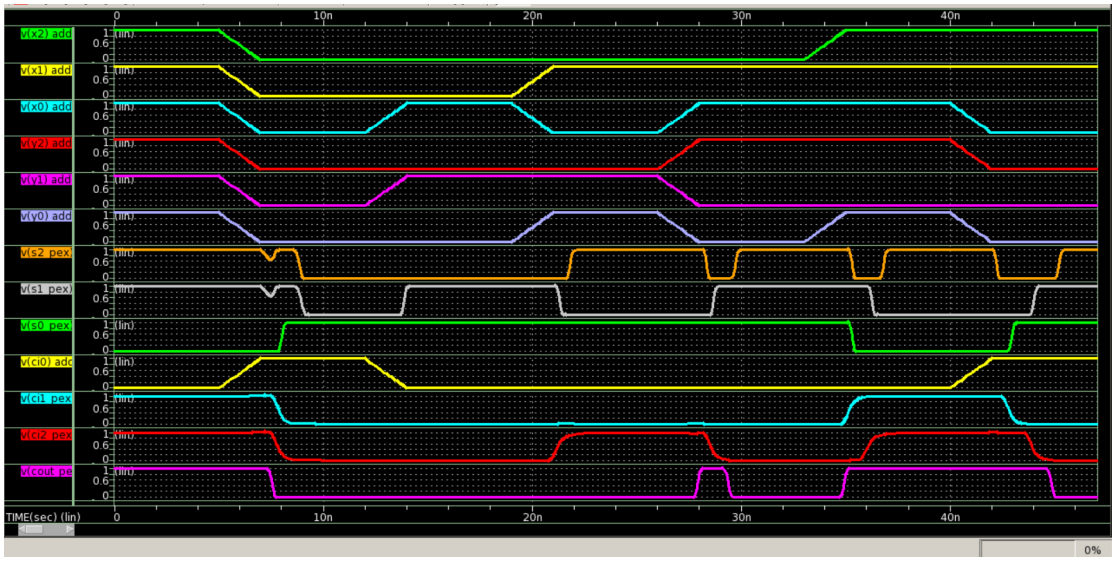

Figure 9：Post-sim Waveform. From top to bottom, the signals are X2, X1, X0, Y2, Y1, Y0, S2_pex, S1_pex, S0_pex, Ci0, Ci1, Ci2, Cout.

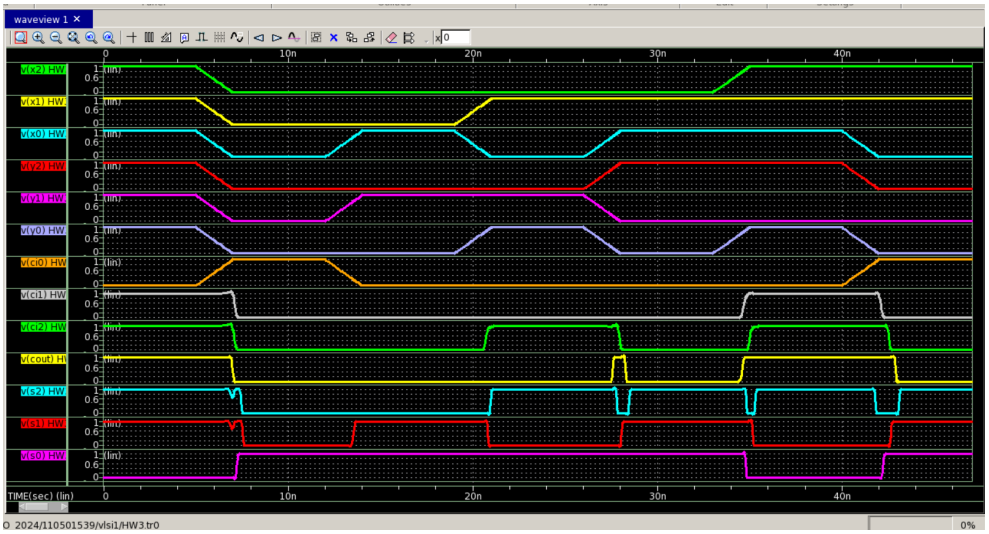

Figure 10：Pre-layout (schematic-level) simulation waveforms used for comparison. From top to bottom, the signals are X2, X1, X0, Y2, Y1, Y0, Ci0, Ci1, Ci2, Cout, S2, S1, S0.

3. Post-Layout worst-case propagation delay & average power consumption

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
pwr=  54.4991u  from=   0.              to=  47.0000n
tdelay=   2.8548n  targ=   8.8548n   trig=   6.0000n
tdelay1= 850.0493p  targ=  13.8500n   trig=  13.0000n
tdelay2=   1.8199n  targ=  21.8199n   trig=  20.0000n
tdelay3=   2.7465n  targ=  29.7465n   trig=  27.0000n
tdelay4=   2.8259n  targ=  36.8259n   trig=  34.0000n
tdelay5=   4.2272n  targ=  45.2272n   trig=  41.0000n
```

Figure 11：Post-Layout worst-case propagation delay & average power consumption. Tdelay to Tdelay5 correspond to the six propagation delays measured between successive signal transitions in Figure 11. The worst-case propagation delay is determined not only by the longest individual delay, but also by the accumulated delay effects from preceding transitions.

```
y
 pwr=  18.1910u  from=   0.              to=  47.0000n
 tdelay=   2.0816n  targ=  43.0816n   trig=  41.0000n
```

Figure 12：Pre-layout worst-case propagation delay and average power consumption with parasitic capacitances removed.

Table 4：Comparison of worst-case propagation delay and average power consumption before and after layout.

	Post-Layout	Pre-Layout
worst-case propagation delay	4.2272ns	2.0816ns
average power consumption	54.4991μW	18.1910μW