LAB 4 Milestone 2 Report

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Explanation：

The combinational FSM has six states: IDLE, RUN, DO, FINE, WR, and DONE.

IDLE is the initialization state; it transitions to the next state once done_trans becomes 1.

RUN is the state where coo_in is stored into the local signals coo_row and coo_col, and fm_wm_row_out is written into the 6×3 matrix.

DO is the first computation state, where the coo_in[0] row of fm_wm_row_out is added to the coo_in[1] row of the final ADJ_FM_WM matrix.

FINE is the second computation state, where the coo_in[1] row of fm_wm_row_out is added to the coo_in[0] row of the final ADJ_FM_WM matrix.

WR is the state that writes the ADJ_FM_WM results into memory.

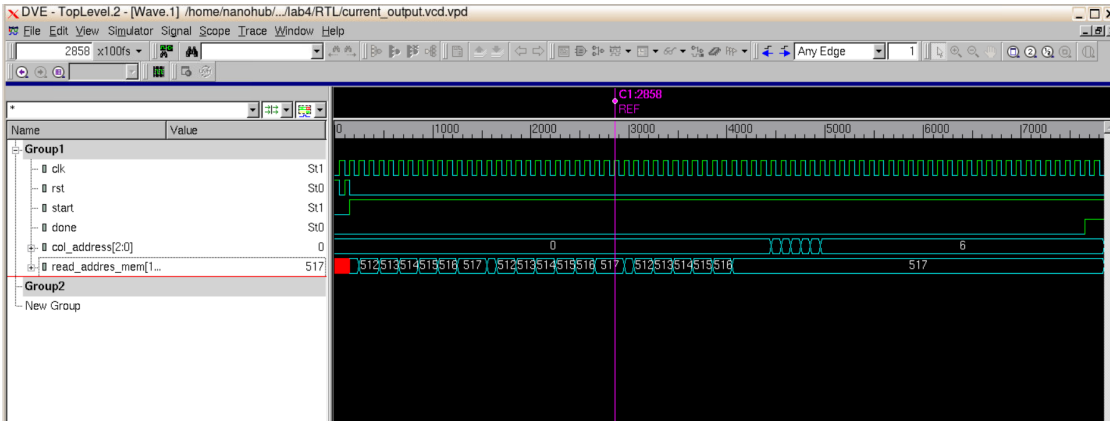
The Argmax FSM has three states: IDLE, RUN, and DONE.

IDLE is the initialization state; it transitions to the next state once done_comb becomes 1.

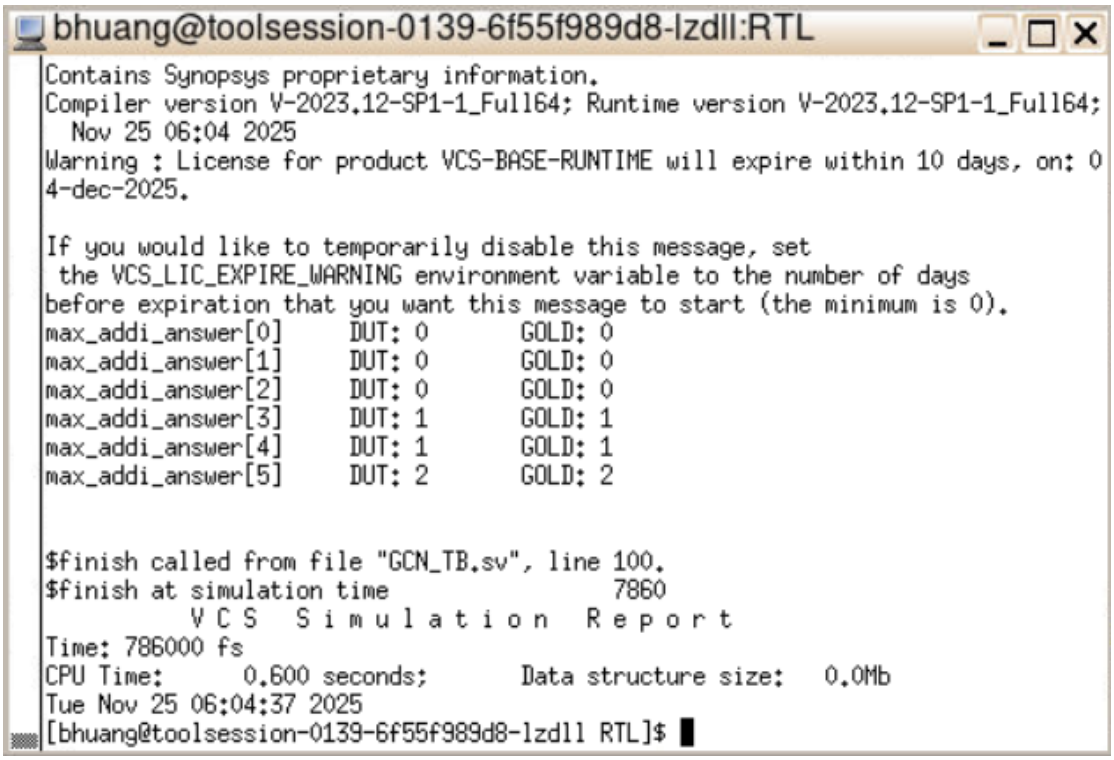
RUN is the state where each row is compared to determine which column contains the largest value and to record its index.

DONE indicates that the GCN computation is complete.

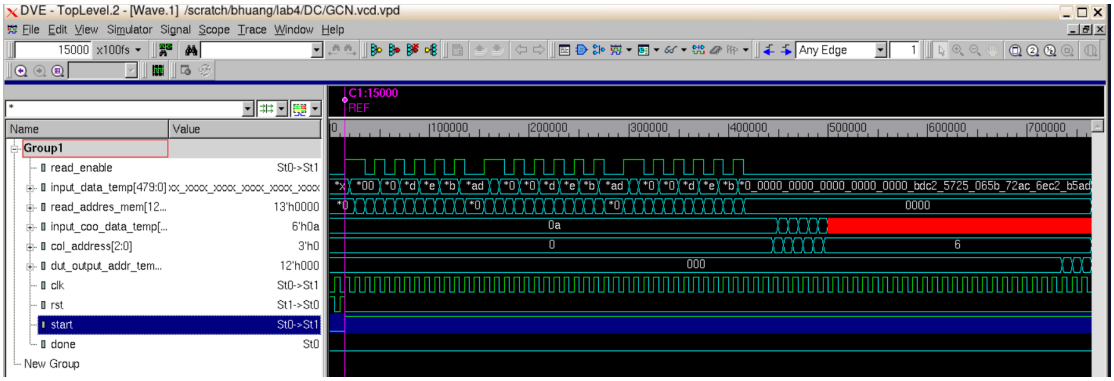
Behavior Verilog Simulation：



Transcript：



Post-syn Simulation：



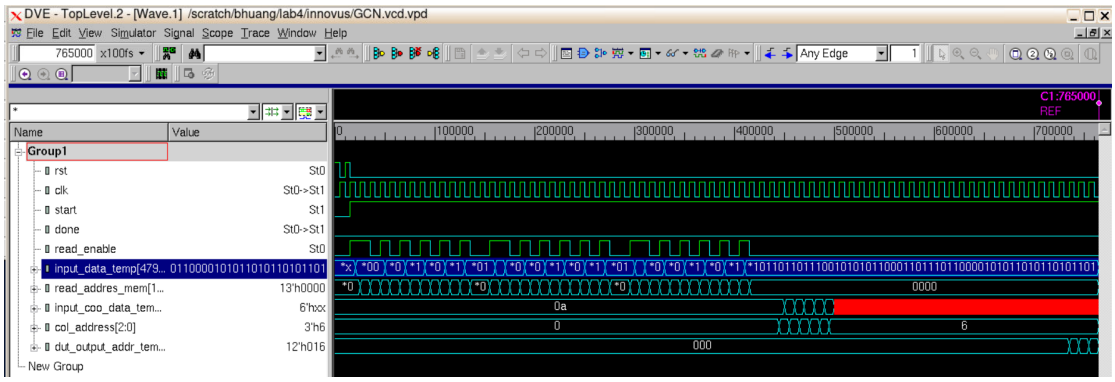
Transcript：

```
bhuang@toolsession-0156-5cd8464d69-zdwk2:/scratch...
Info: [VCS_SAVE_RESTORE_INFO] ASLR (Address Space Layout Randomization) is detec
ted on the machine. To enable $save functionality, ASLR will be switched off and
 simv re-executed.
Please use '-no_save' simv switch to avoid re-execution or '-suppress=ASLR_DETEC
TED_INFO' to suppress this message.
Chronologic VCS simulator copyright 1991-2023
Contains Synopsys proprietary information.
Compiler version V-2023.12-SP1-1_Full64; Runtime version V-2023.12-SP1-1_Full64;
  Dec  4 22:17 2025
max_addi_answer[0]     DUT: 0       GOLD: 0
max_addi_answer[1]     DUT: 0       GOLD: 0
max_addi_answer[2]     DUT: 0       GOLD: 0
max_addi_answer[3]     DUT: 1       GOLD: 1
max_addi_answer[4]     DUT: 1       GOLD: 1
max_addi_answer[5]     DUT: 2       GOLD: 2


$finish called from file "GCN_TB_post_syn_apr.sv", line 124.
$finish at simulation time                765020
           V C S   S i m u l a t i o n   R e p o r t
Time: 76502000 fs
CPU Time:      0.680 seconds;       Data structure size:   2.7Mb
```

Total latency： 75 ns at the clock frequency of 1000 MHz

Post-APR simulation：



Transcript：

```
bhuang@toolsession-0156-5cd8464d69-zdwk2:/scratch...
Info: [VCS_SAVE_RESTORE_INFO] ASLR (Address Space Layout Randomization) is detec
ted on the machine. To enable $save functionality, ASLR will be switched off and
 simv re-executed.
Please use '-no_save' simv switch to avoid re-execution or '-suppress=ASLR_DETEC
TED_INFO' to suppress this message.
Chronologic VCS simulator copyright 1991-2023
Contains Synopsys proprietary information.
Compiler version V-2023.12-SP1-1_Full64; Runtime version V-2023.12-SP1-1_Full64;
  Dec  7 16:03 2025
max_addi_answer[0]     DUT: 0       GOLD: 0
max_addi_answer[1]     DUT: 0       GOLD: 0
max_addi_answer[2]     DUT: 0       GOLD: 0
max_addi_answer[3]     DUT: 1       GOLD: 1
max_addi_answer[4]     DUT: 1       GOLD: 1
max_addi_answer[5]     DUT: 2       GOLD: 2


$finish called from file "GCN_TB_post_syn_apr.sv", line 124.
$finish at simulation time                765020
           V C S   S i m u l a t i o n   R e p o r t
Time: 76502000 fs
CPU Time:      0.780 seconds;       Data structure size:   3.6Mb
Sun Dec  7 16:03:13 2025
[bhuang@toolsession-0156-5cd8464d69-zdwk2 innovus]$
```

Total Power (From Innovus)： 8.115 mW

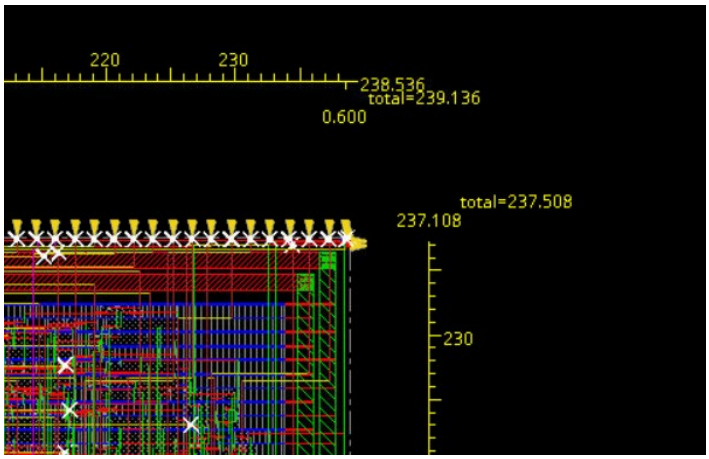
```
Total Power
--------------------------------------------------------------------------------------
Total Internal Power:        3.78770687            46.6775%
Total Switching Power:       4.32487041            53.2972%
Total Leakage Power:         0.00205256             0.0253%
Total Power:                 8.11462984
--------------------------------------------------------------------------------------
```

Innovus density：Before filler cell insertion 0.7329

```
Density: 73.729%
---------------------------------------------------------------
**optDesign ... cpu = 0:00:25, real = 0:00:25, mem = 4955.4M, totSessionCpu=2:23
:47 **
```

Area：Standard cells + Filler cells 0.052273 mm^2

```
==============================
Floorplan/Placement Information
==============================
Total area of Standard cells: 52273.849 um^2
Total area of Standard cells(Subtracting Physical Cells): 36291.136 um^2
Total area of Macros: 0.000 um^2
Total area of Blockages: 0.000 um^2
Total area of Pad cells: 0.000 um^2
Total area of Core: 52273.849 um^2
Total area of Chip: 57001.999 um^2
```



Number of gates：

Gate = 51856

Cells = 24107

```
innovus 180> reportGateCount
Gate area 0.6998 um^2
[0] GCN Gates=51856 Cells=24107 Area=36291.1 um^2
```

Post_APR – DRC Check：

```
##############################################################
#  Generated by:      Cadence Innovus 23.12-s091 1
#  OS:                Linux x86 64(Host ID toolsession-0156-5cd8464d69-zdwk2)
#  Generated on:      Sun Dec  7 17:35:56 2025
#  Design:            GCN
#  Command:           verify drc
##############################################################

OFFGRID: ( Off Grid or Wrong Way ) Special Wire of Net VSS  ( M2 )
Bounds : ( 1.044, 1.044 ) ( 238.428, 2.268 )


OFFGRID: ( Off Grid or Wrong Way ) Special Wire of Net VDD  ( M2 )
Bounds : ( 2.768, 2.768 ) ( 236.704, 3.992 )


OFFGRID: ( Off Grid or Wrong Way ) Special Wire of Net VSS  ( M3 )
Bounds : ( 1.044, 1.044 ) ( 2.268, 236.952 )


OFFGRID: ( Off Grid or Wrong Way ) Special Wire of Net VDD  ( M3 )
Bounds : ( 2.768, 2.768 ) ( 3.992, 235.228 )


  Total Violations : 4 Viols.
```

Post_APR – LVS Check：

```
#########################################################################
#  Generated by:      Cadence Innovus 23.12-s091 1
#  OS:                Linux x86 64(Host ID toolsession-0156-5cd8464d69-zdwk2)
#  Generated on:      Sun Dec  7 06:50:16 2025
#  Design:            GCN
#  Command:           verifyConnectivity
#########################################################################
Verify Connectivity Report is created on Sun Dec  7 06:50:16 2025



Begin Summary
    Found no problems or warnings.
End Summary
```

Screenshot of your timing report for the worstcase setup path：

```
Path Groups: {clk}
Analysis View: default_setup_view
Other End Arrival Time        168.000
- Setup                         6.783
+ Phase Shift                1000.000
- Uncertainty                   0.010
= Required Time              1161.207
- Arrival Time               1146.619
= Slack Time                   14.588
     Clock Rise Edge                0.000
     + Clock Network Latency (Prop)  -36.081
     = Beginpoint Arrival Time       -36.081
```

Screenshot of your timing report for the worstcase hold path：

```
#########################################################################
Path 1: MET Hold Check with Pin coo_row_reg_0__1_/CLK
Endpoint:   coo_row_reg_0__1_/D (v) checked with  leading edge of 'clk'
Beginpoint: coo_in[3]           (^) triggered by  leading edge of '@'
Path Groups: {clk}
Analysis View: default_hold_view
Other End Arrival Time         38.913
+ Hold                         28.067
+ Phase Shift                   0.000
+ Uncertainty                   0.010
= Required Time                66.990
  Arrival Time                 68.200
  Slack Time                    1.210
     Clock Rise Edge                      0.000
     + Input Delay                        0.000
     = Beginpoint Arrival Time            0.000
     +-------------------------------------------------------------------------------------------+
     |     Instance      |     Arc      |          Cell           |  Delay | Arrival | Required |
     |                   |              |                         |        |  Time   |   Time   |
     |-------------------+--------------+-------------------------+--------+---------+----------|
     |                   | coo_in[3] ^  |                         |        |   0.000 |   -1.210 |
     | U9215             | A1 ^ -> Y v  | OAI21xp33_ASAP7_75t_R   | 34.200 |  34.200 |   32.990 |
     | U16409            | B v -> Y ^   | NAND3xp33_ASAP7_75t_R   | 21.900 |  56.100 |   54.890 |
     | U16410            | C ^ -> Y v   | A2O1A1Ixp33_ASAP7_75t_R | 12.100 |  68.200 |   66.990 |
     | coo_row_reg_0__1_ | D v          | ASYNC_DFFHx1_ASAP7_75t_R |  0.000 |  68.200 |   66.990 |
     +-------------------------------------------------------------------------------------------+
```