Summary of Research

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Supervisors:
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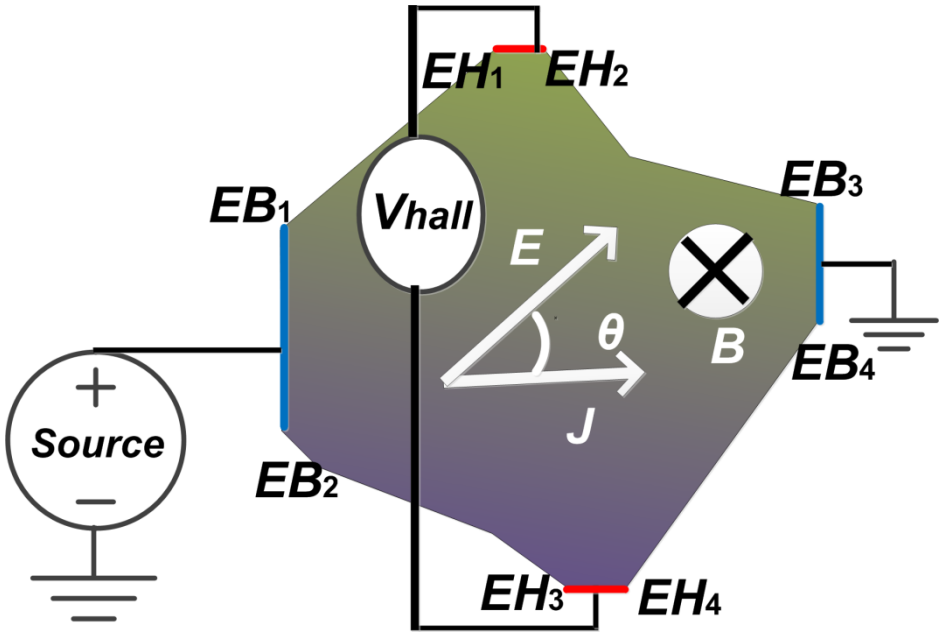
Xiangfeng Duan (UCLA)

Outline

- Modeling and Optimization of Planar Hall Devices
- Modeling of Vertical Layered Heterostructures (Graphene-Silicon-Graphene “GSG” structure)
- Modeling of CBRAM And RRAM/CBRAM’s Application on Brain-inspired Computing (on-going)
- Questions

I. Modeling and Optimization of Planar Hall Devices --- Backgrounds



The sensitivity of a Hall device is determined both by its material properties and its geometry

$$S_I = \left| \frac{\partial V_{out}}{\partial B} \bullet \frac{1}{I_{bias}} \right| = G_I \frac{|R_H|}{t} (0 < G_I < 1)$$

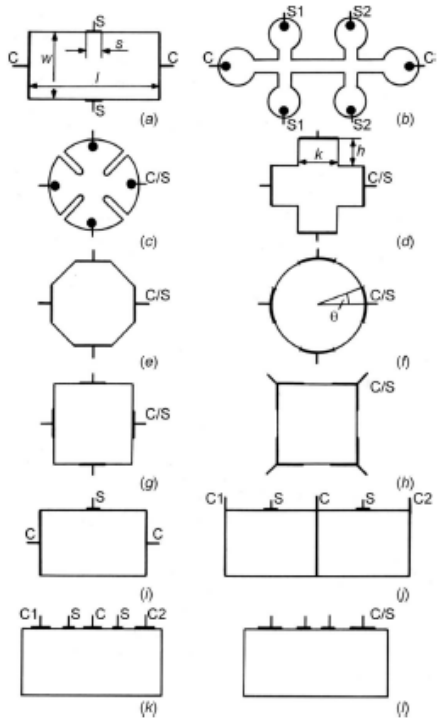
$$S_V = \left| \frac{\partial V_{out}}{\partial B} \bullet \frac{1}{V_{bias}} \right| = G_V \mu_H (0 < G_V < 0.74)$$

$$R_H = \frac{1}{en_h}$$

Guo, Zhang, et al. "Geometry Optimization of Planar Hall Devices under Voltage Biasing " *Electron Devices, IEEE Transactions on* 61 (12), 2014, PP. 4216-4223 Supervisor: Prof. ZP Yu and JY Zhang

I. Modeling and Optimization of Planar Hall Devices --- Backgrounds

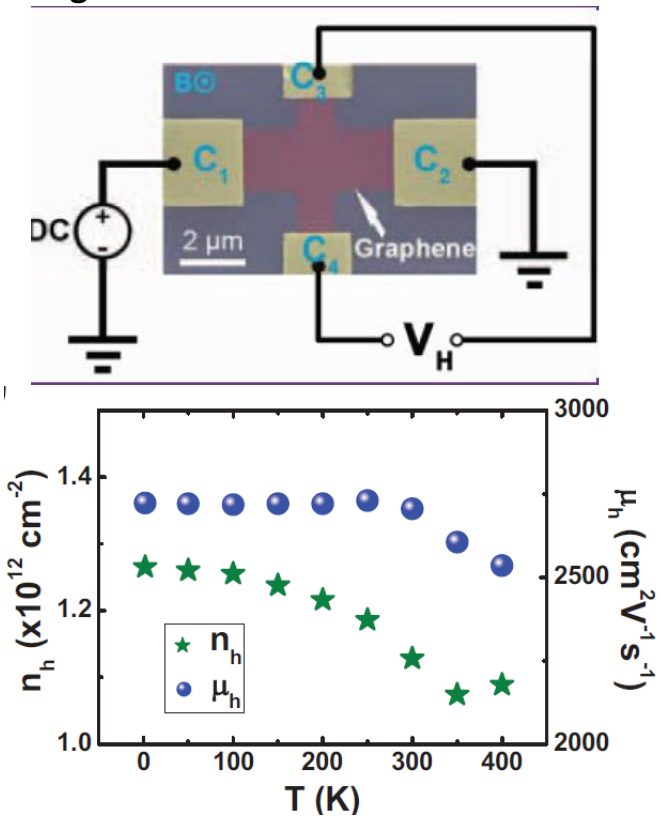
Previous study most focused on current biasing mode; The best result of voltage biasing mode only has G_V=0.47.



Popovic, Radivoje S. *Hall effect devices*. CRC Press, 2010.

O. Paul, "CMOS-integrated four-contact sensors for magnetic and mechanical signals: Novel devices, systems, and applications," in Proc. IEEE Sensors, 2012

2D materials like graphene needs voltage biasing mode



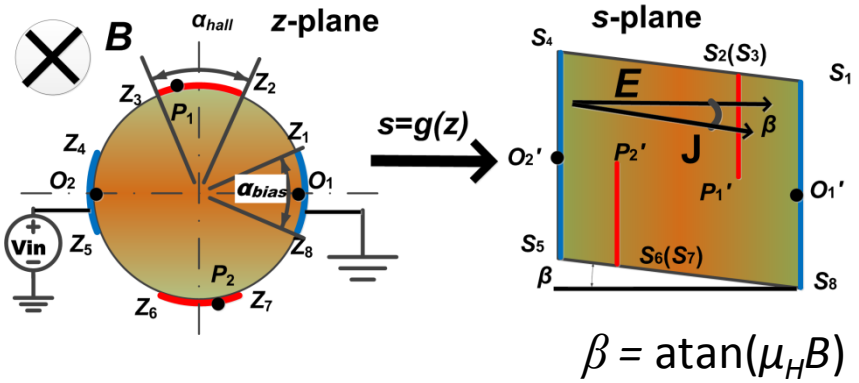
H. L. Xu et al., "Batch-fabricated high-performance graphene Hall elements," Sci. Rep.,2013

I. Modeling and Optimization of Planar Hall Devices --- Problem

- Under voltage biasing, for planar Hall devices, we want to find a good geometry.
  - Good geometry
    - no point like edges or contacts
    - large G_V (≈0.74)
  - How to compute the sensitivity
    - solve the Laplace equation (static potential) in 2D plane with complex boundaries

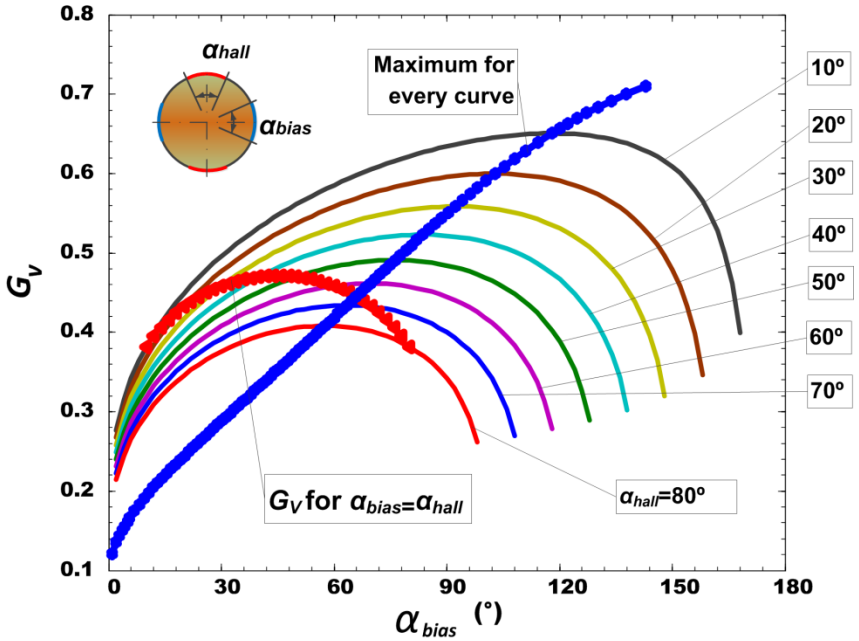
I. Modeling and Optimization of Planar Hall Devices --- Method

SCT for Calculation



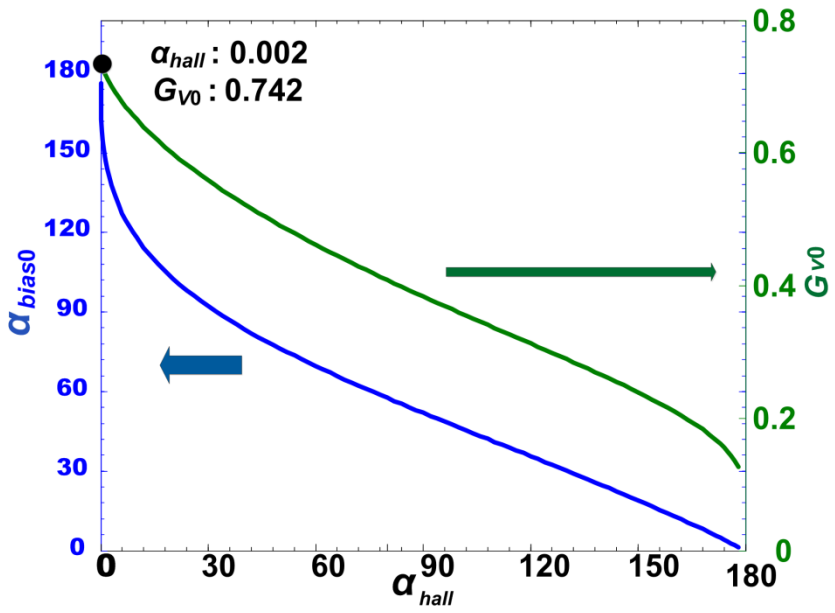
$$\beta = \text{atan}(\mu_H B)$$

$$G_V \approx \frac{|S_7S_8| - |S_1S_2|}{|S_1S_4|} \frac{1}{\mu_H B}$$

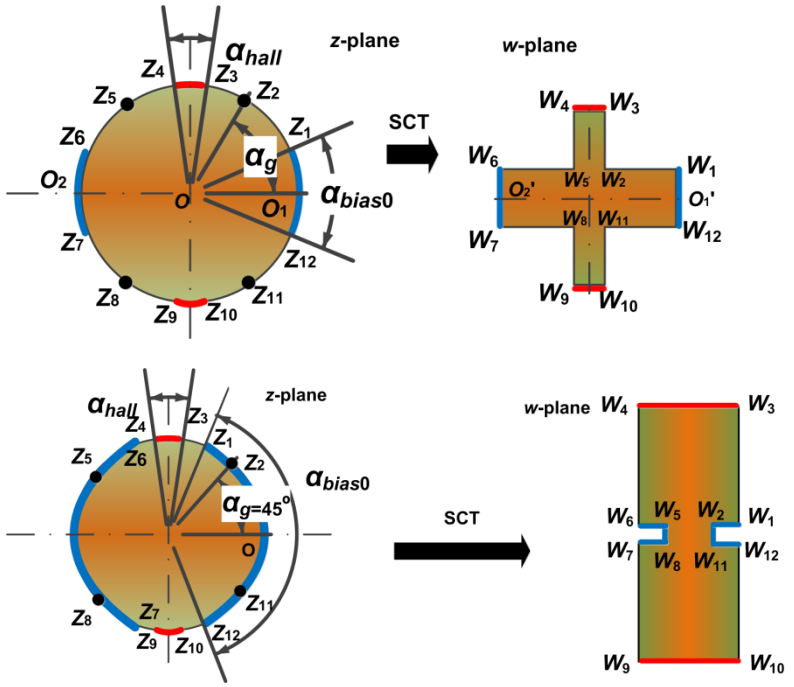


If two geometry can be connected by conformal mapping, then their G_I and G_V are the same. (SCT means Schwarz-Christoffel transformation)

I. Modeling and Optimization of Planar Hall Devices --- Method



SCT for Optimization



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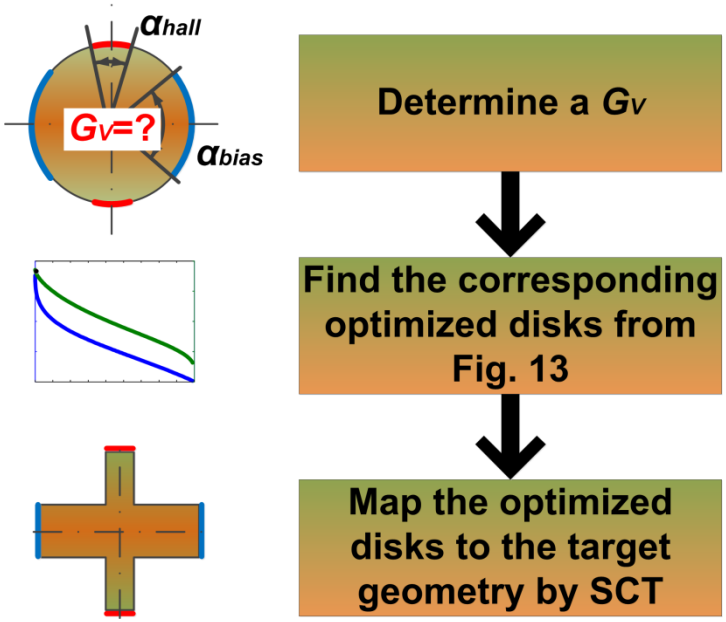
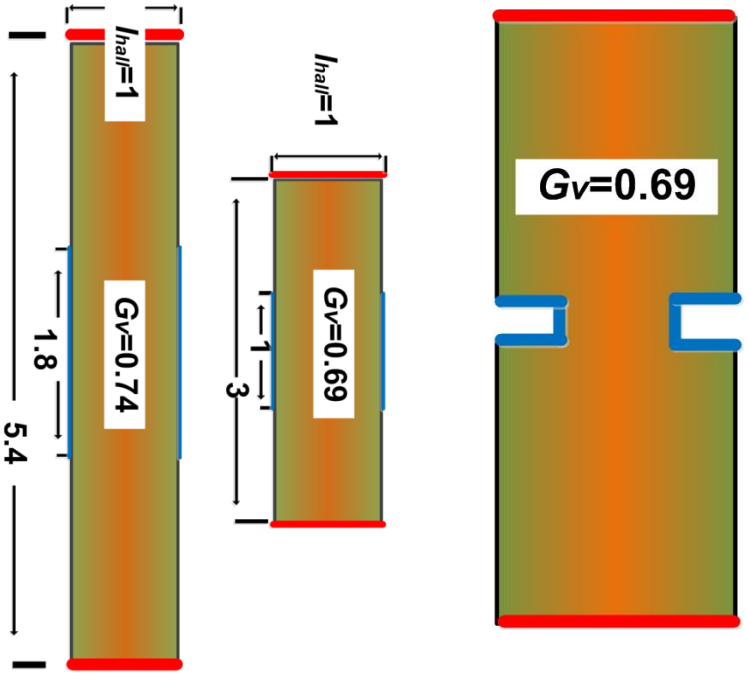
I. Modeling and Optimization of Planar Hall Devices --- Result

Method



Geometry



I. Modeling and Optimization of Planar Hall Devices --- Application and Contribution

Application

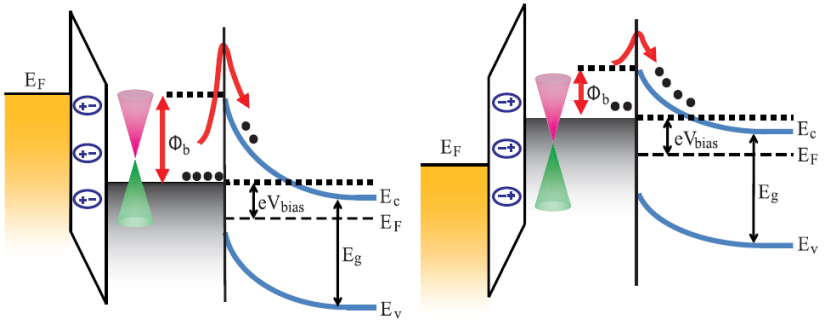
- These are geometry suitable for Hall Plan working under voltage biasing
- The geometry increase the G_V of the state of art design by 46.8% (for $G_V = 0.69$) and 57.4% (for $G_V = 0.74$)
- The design approximate the limit of G_V *(0.74)* predict by Popovic

Contribution

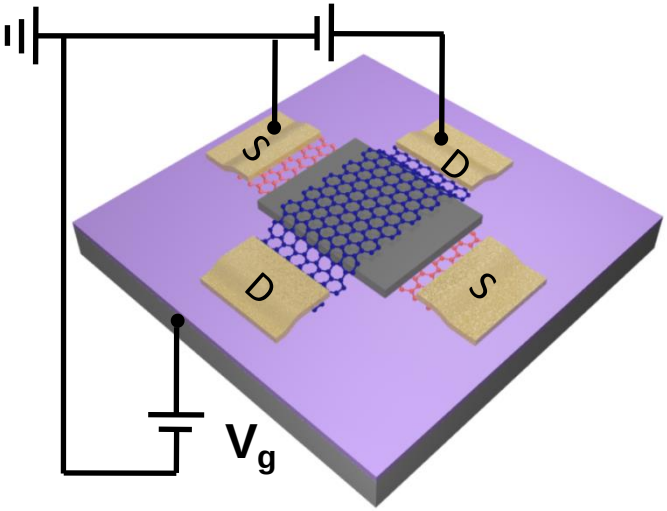
- Guo found the idea, developed the method and carried out the calculation
- Prof. Zhiping Yu and Prof. Jinyu Zhang supervised the work

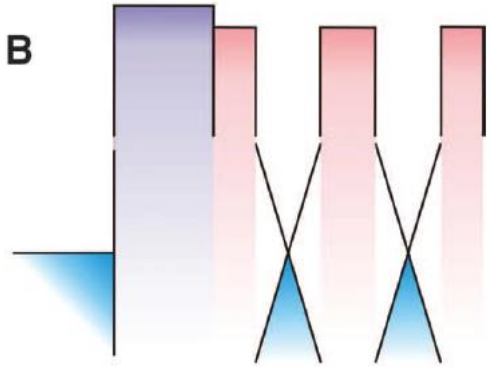
Guo, Zhang, et al. "Geometry Optimization of Planar Hall Devices under Voltage Biasing " *Electron Devices, IEEE Transactions on* 61 (12), 2014, PP. 4216-4223 Supervisor: Prof. ZP Yu and JY Zhang

II. Theory of GSG Structure --- Background & Experiment

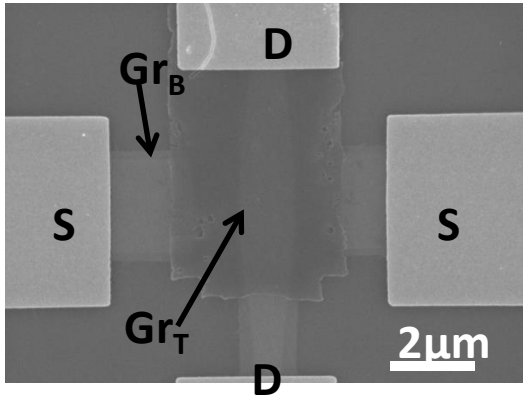


Science 336.6085 (2012): 1140-1143





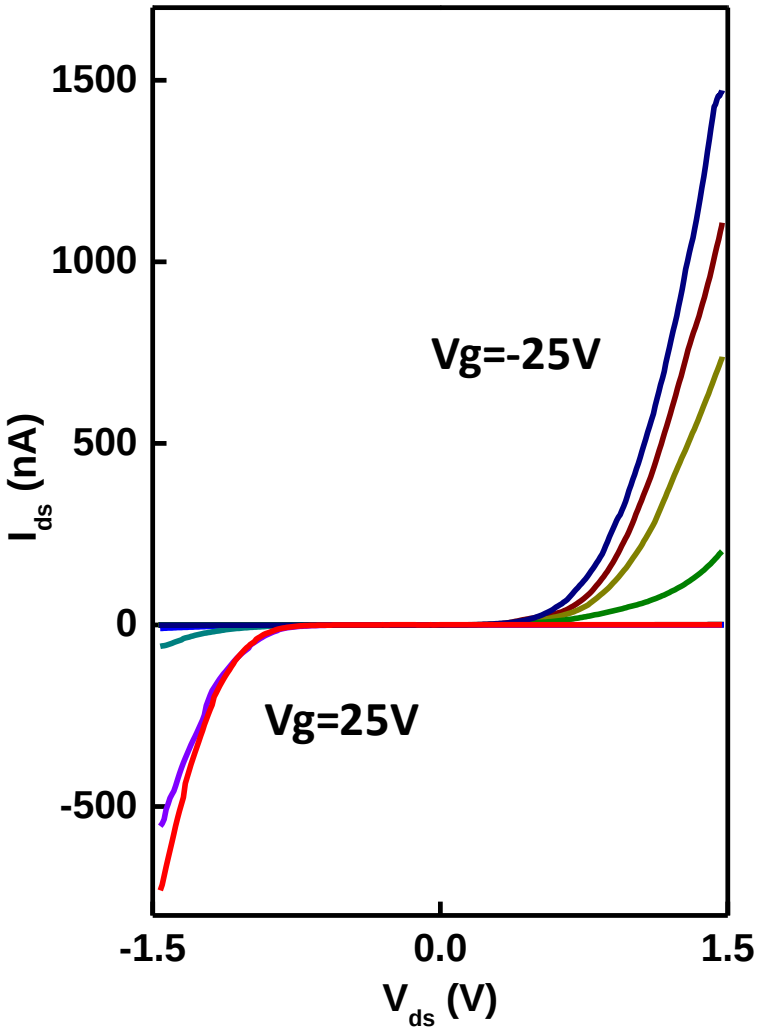
Science 335.6071 (2012): 947-950



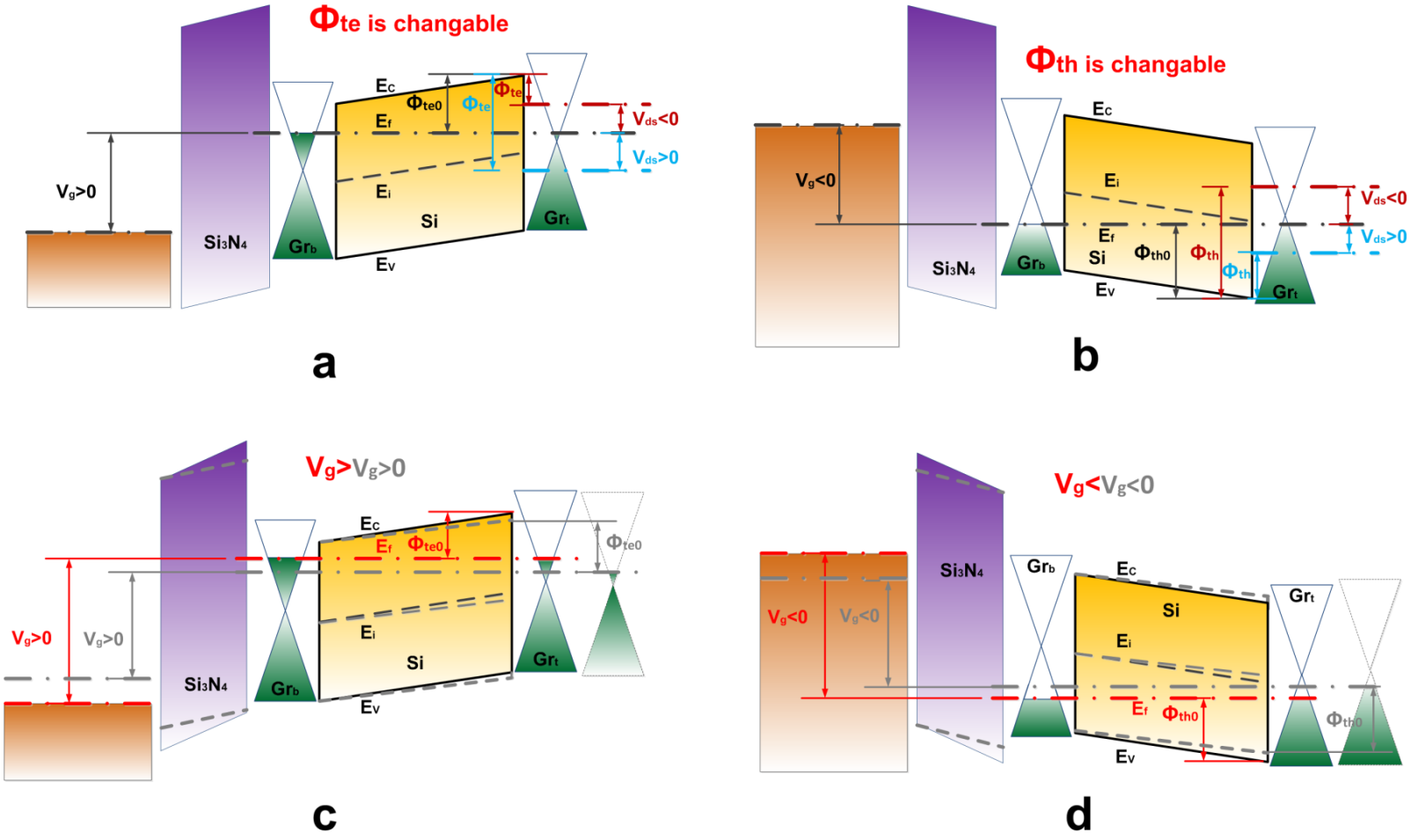
Liu, Yuan, Guo Zhang, et al. "Ambipolar barristors for re-configurable logic circuits" (manuscript for *Nature communications* finished) Supervisor: Prof. Xiangfeng Duan

II. Theory of GSG Structure --- Problem

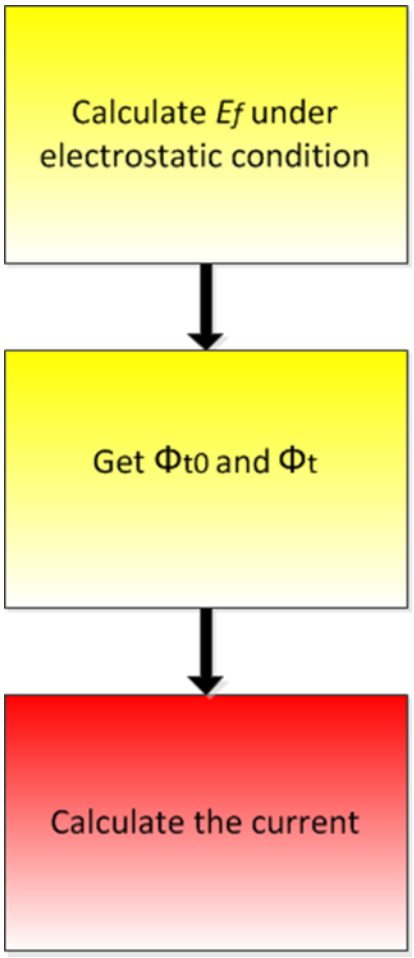
- We have to explain the strange and unique electrical characteristics of the device
  - gate voltage
    - different signs have nearly inversed characteristics
    - different gate voltage has different strength of current
  - different V_{ds}
    - Rectifying characteristic at each given gate voltage

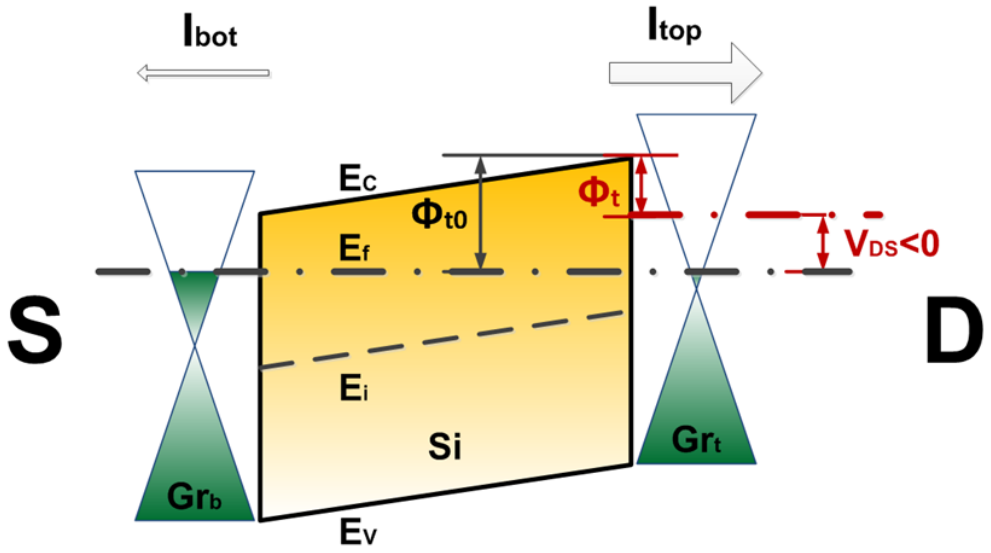


II. Theory of GSG Structure --- Explanation



II. Theory of GSG Structure --- Quantization



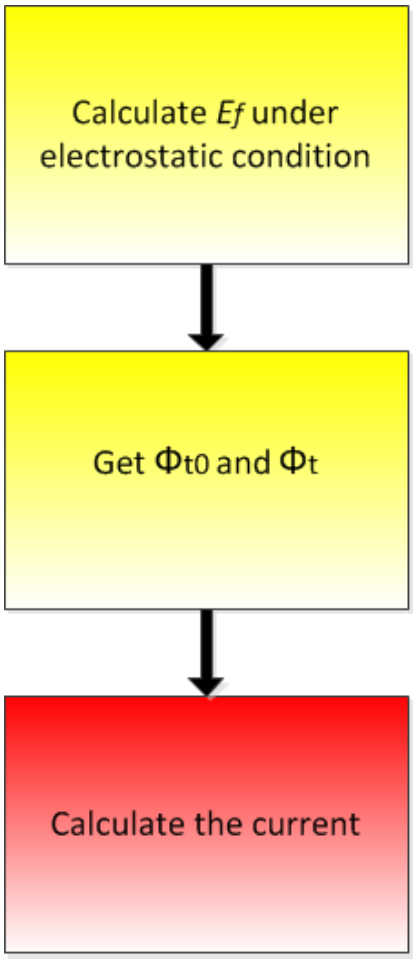


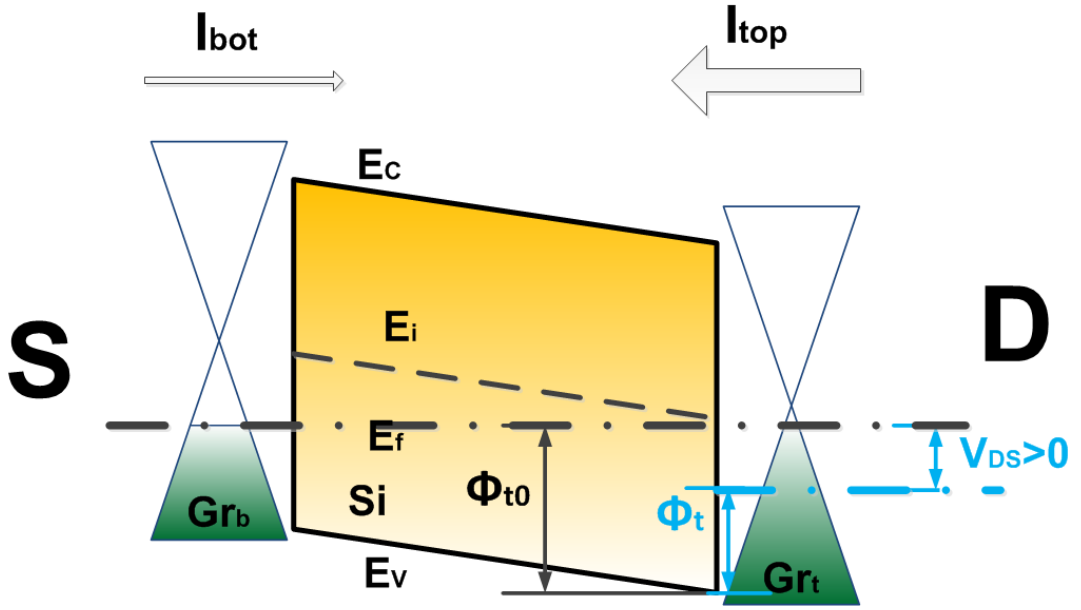
$$I_{ds} = I_{ds\_top} + I_{ds\_bot}$$

$$= -AR_{electron}T^2 e^{-\frac{e\Phi_{t\_electron}(V_g,V_{ds})}{kT}} + AR_{electron}T^2 e^{-\frac{e\Phi_{t\_electron}(V_g,0)}{kT}}$$

$$= -AR_{electron}T^2 e^{-\frac{e\Phi_{t0\_electron}(V_g)}{kT}} (e^{-\frac{emV_{ds}}{kT}} - 1)$$

II. Theory of GSG Structure --- Quantization



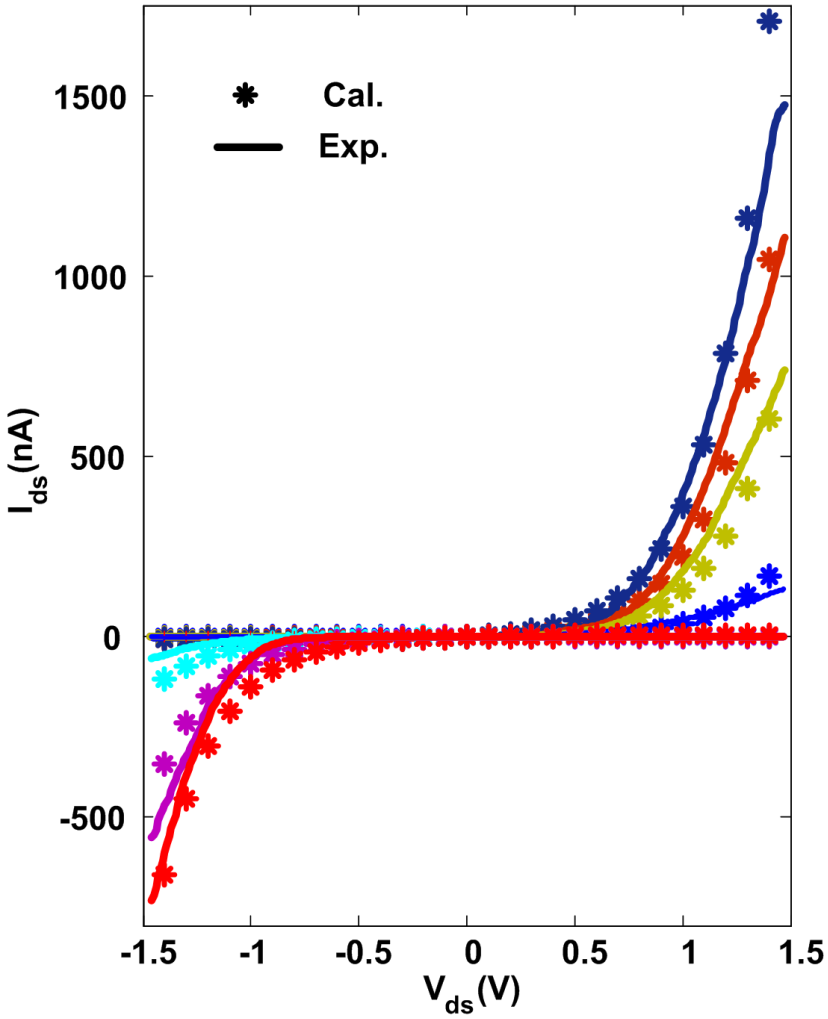


$$I_{ds} = I_{ds\_top} + I_{ds\_bot}$$

$$= AR_{hole}T^2 e^{-\frac{e\Phi_{t\_hole}(V_g, V_{ds})}{kT}} - AR_{hole}T^2 e^{-\frac{e\Phi_{t\_hole}(V_g, 0)}{kT}}$$

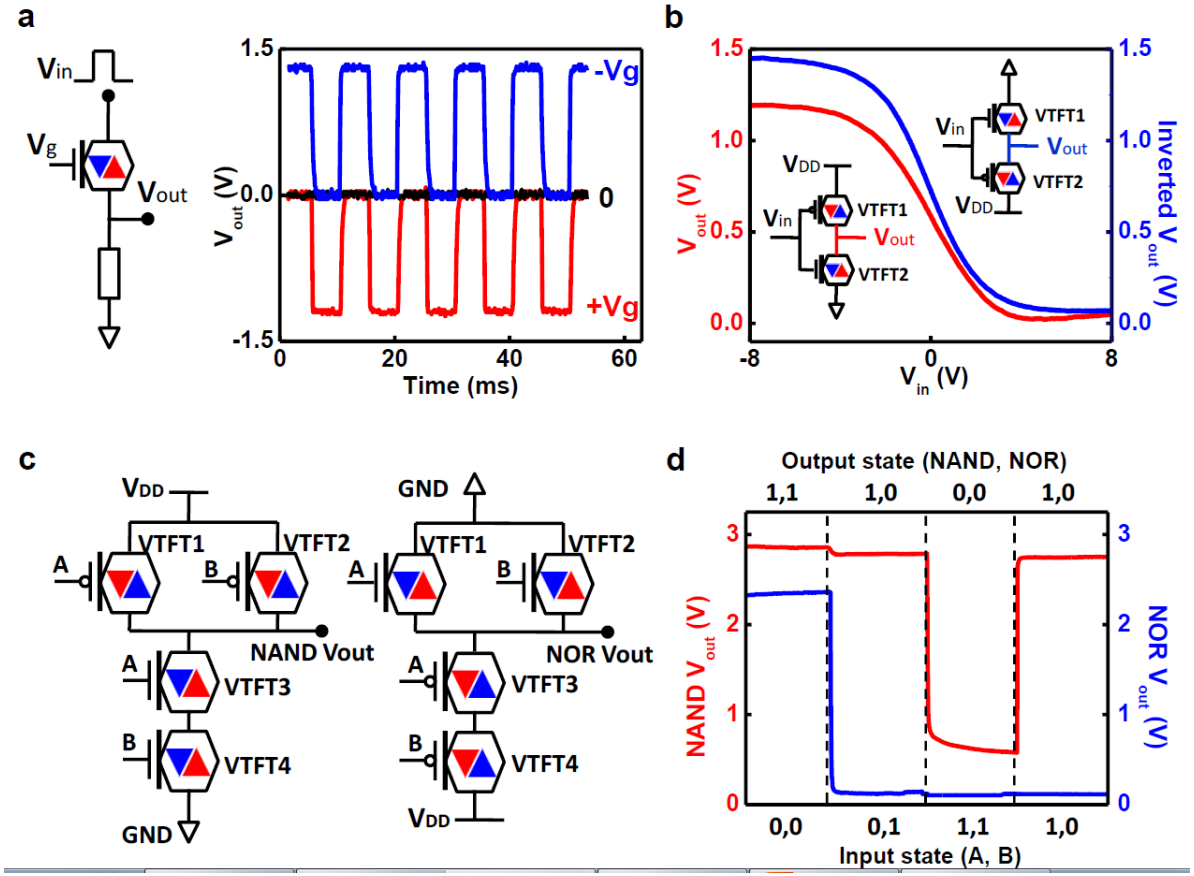
$$= AR_{hole}T^2 e^{-\frac{e\Phi_{t0\_hole}(V_g)}{kT}} (e^{\frac{emV_{ds}}{kT}} - 1)$$

II. Theory of GSG Structure --- Results



- Important part of this device
  - Completely novel working principle
  - Large area vertical device with graphene used as electrodes
  - Can be used for re-configurable logic circuits (be p or n transistors controlled by the gate)

II. Theory of GSG Structure --- Application and Contribution



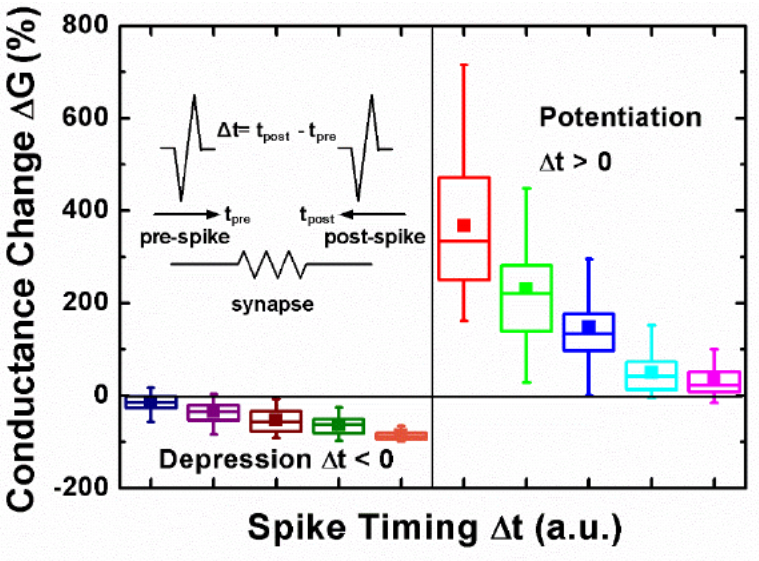
- Contribution
  - Guo for the theory and simulation
  - Yuan for the experiment
  - Prof. Duan is the supervisor

Liu, Yuan, Guo Zhang, et al. "Ambipolar barristors for re-configurable logic circuits" (manuscript for *Nature communications* finished) Supervisor: Prof. Xiangfeng Duan

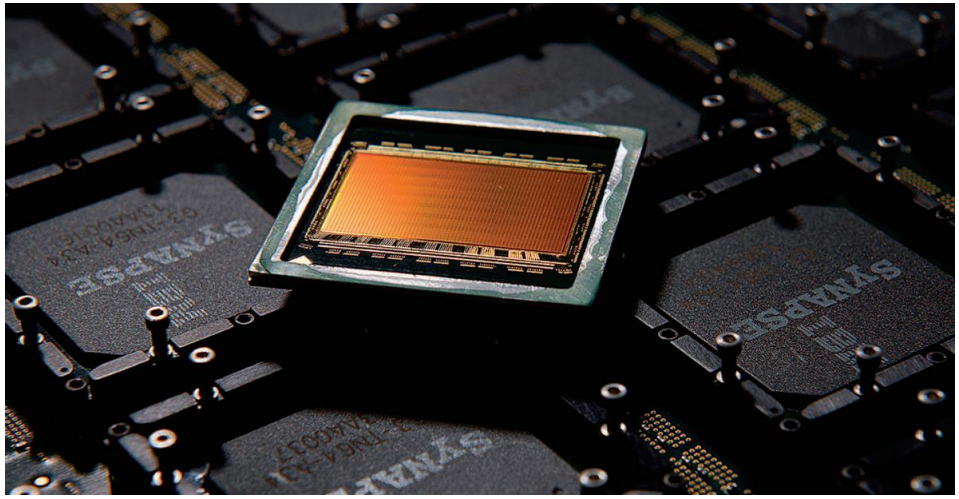
III. Brain-inspired Computation --- Background

Killer applications besides memory have to be found for RRAM/CBRAM; And people are beginning to think about its application on brain-inspired computation.

IBM's True North based on 5.4 billion CMOS has demonstrated the most frontier result in this area.



Yu, Shimeng, et al. ISCAS, 2014



Merolla, Paul A., et al. "A million spiking-neuron integrated circuit with a scalable communication network and interface." Science 345.6197 (2014): 668-673.

III. Brain-inspired Computation --- Problem & Things to Do

- Problem
  - What RRAM/CBRAM can do?
  - The comparison between CMOS-based and RRAM/CBRAM-based brain-inspired circuits
- Things to Do (Initial Stage)
  - Find a typical brain-inspired circuit or unit by CMOS
  - Realize it again by introduce RRAM/CBRAM into it
  - Comparing its performance

Questions

- What is the future of 2D materials?
- The difference of flexible devices made by different method(2D, Organic, Silicon)?
- The use for Van der Waals hetero junctions?
- what kind of career you want your student to pursue, academia or entrepreneurship?
- Theory or experiment?