

								Note (1
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U324	DQS for X8
2A	VREFB2AN0	Ю			DIFFIO_TX_L9n	DIFFOUT_L9n	E2	
2A	VREFB2AN0	10			DIFFIO_RX_L10n	DIFFOUT_L10n	J4	DQ1L
2A	VREFB2AN0	10			DIFFIO_TX_L9p	DIFFOUT_L9p	D1	DQ1L
2A	VREFB2AN0	10			DIFFIO_RX_L10p	DIFFOUT_L10p	J3	DQ1L
2A	VREFB2AN0	10			DIFFIO_RX_L11n	DIFFOUT_L11n	K2	DQSn1L
2A	VREFB2AN0	10			DIFFIO_TX_L12n	DIFFOUT_L12n	E3	DQ1L
2A	VREFB2AN0	10			DIFFIO_RX_L11p	DIFFOUT_L11p	K3	DQS1L
2A	VREFB2AN0	10			DIFFIO_TX_L12p	DIFFOUT_L12p	F2	
2A	VREFB2AN0	10			DIFFIO_TX_L13n	DIFFOUT_L13n	E1	DQ1L
2A	VREFB2AN0	10			DIFFIO_RX_L14n	DIFFOUT_L14n	F4	DQ1L
2A	VREFB2AN0	10			DIFFIO_TX_L13p	DIFFOUT_L13p	F1	DQ1L
2A	VREFB2AN0	10			DIFFIO_RX_L14p	DIFFOUT_L14p	G3	DQ1L
2A	VREFB2AN0	10			DIFFIO_RX_L15n	DIFFOUT_L15n	K1	
2A	VREFB2AN0	IO			DIFFIO_TX_L16n	DIFFOUT_L16n	H2	DQ1L
2A	VREFB2AN0	10			DIFFIO_RX_L15p	DIFFOUT_L15p	L1	
2A	VREFB2AN0	10			DIFFIO_TX_L16p	DIFFOUT_L16p	G2	DQ1L
2A	VREFB2AN0	10		1	DIFFIO TX L17n	DIFFOUT L17n	J1	1
2A	VREFB2AN0	IO		†	DIFFIO_RX_L18n	DIFFOUT_L18n	L2	DQ2L
2A	VREFB2AN0	10		+	DIFFIO TX L17p	DIFFOUT L17p	H1	DQ2L
2A 2A	VREFB2AN0	IO		+	DIFFIO_TX_L17p	DIFFOUT_L18p	M2	DQ2L DQ2L
2A 2A	VREFB2AN0	10		+	DIFFIO_RX_L19n	DIFFOUT_L19n	L5	DQSn2L
2A 2A	VREFB2AN0	10		+	DIFFIO_TX_L20n	DIFFOUT_L20n	R1	DQ3H2L DQ2L
2A 2A				-				
	VREFB2AN0	10			DIFFIO_RX_L19p	DIFFOUT_L19p	M4	DQS2L
2A	VREFB2AN0	IO			DIFFIO_TX_L20p	DIFFOUT_L20p	P1	DOOL
2A	VREFB2AN0	10			DIFFIO_TX_L21n	DIFFOUT_L21n	R2	DQ2L
2A	VREFB2AN0	10			DIFFIO_RX_L22n	DIFFOUT_L22n	N2	DQ2L
2A	VREFB2AN0	IO			DIFFIO_TX_L21p	DIFFOUT_L21p	T1	DQ2L
2A	VREFB2AN0	IO			DIFFIO_RX_L22p	DIFFOUT_L22p	N3	DQ2L
2A	VREFB2AN0	10			DIFFIO_RX_L23n	DIFFOUT_L23n	L4	
2A	VREFB2AN0	10			DIFFIO_TX_L24n	DIFFOUT_L24n	T2	DQ2L
2A	VREFB2AN0	10			DIFFIO_RX_L23p	DIFFOUT_L23p	M3	
2A	VREFB2AN0	10			DIFFIO_TX_L24p	DIFFOUT_L24p	R3	DQ2L
3A		TDO		TDO			P5	
3A		nCSO		DATA4			P3	
3A		TMS		TMS			P6	
3A		AS_DATA3		DATA3			M5	
3A		TCK		TCK			L6	
3A		AS_DATA2		DATA2			U3	
3A		TDI		TDI			N6	
3A		AS_DATA1		DATA1			U2	
3A		DCLK		DCLK			K6	
3A		AS_DATA0,ASDO		DATA0			V1	
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	M7	DQ1B
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	V2	
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	N7	DQ1B
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	V3	DQ1B
3A	VREFB3AN0	10		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	M10	DQSn1B
3A	VREFB3AN0	10		DATA9	DIFFIO TX B4n	DIFFOUT B4n	U7	DQ1B
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	N10	DQS1B
3A	VREFB3AN0	10		DATA12 DATA11	DIFFIO TX B4p	DIFFOUT B4p	T7	24010
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B5n	M8	DQ1B
3A 3A	VREFB3AN0	IO		DATA14 DATA13	DIFFIO_RX_B6n	DIFFOUT_B6n	P4	DQ1B DQ1B
							M9	DQ1B DQ1B
3A	VREFB3AN0	10		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p		
3A	VREFB3AN0	10		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	R4	DQ1B
3A	VREFB3AN0	10		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	N11	2012
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	P8	DQ1B



								Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U324	DQS for X8
3A	VREFB3AN0	Ю		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	P11	
3A	VREFB3AN0	10			DIFFIO_TX_B8p	DIFFOUT_B8p	N8	DQ1B
3B	VREFB3BN0	10			DIFFIO_TX_B17n	DIFFOUT_B17n	V6	
3B	VREFB3BN0	10			DIFFIO_RX_B18n	DIFFOUT_B18n	U5	DQ2B
3B	VREFB3BN0	10			DIFFIO_TX_B17p	DIFFOUT_B17p	V7	DQ2B
3B	VREFB3BN0	10			DIFFIO_RX_B18p	DIFFOUT_B18p	U4	DQ2B
3B	VREFB3BN0	10			DIFFIO_RX_B19n	DIFFOUT_B19n	P9	DQSn2B
3B	VREFB3BN0	10			DIFFIO_TX_B20n	DIFFOUT_B20n	T4	DQ2B
3B	VREFB3BN0	10			DIFFIO_RX_B19p	DIFFOUT_B19p	P10	DQS2B
3B	VREFB3BN0	10			DIFFIO_TX_B20p	DIFFOUT_B20p	T5	
3B	VREFB3BN0	10	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	V8	DQ2B
3B	VREFB3BN0	10			DIFFIO_RX_B22n	DIFFOUT_B22n	Т9	DQ2B
3B	VREFB3BN0	10	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	U8	DQ2B
3B	VREFB3BN0	IO		i	DIFFIO_RX_B22p	DIFFOUT_B22p	R9	DQ2B
3B	VREFB3BN0	10	CLK1n		DIFFIO_RX_B23n	DIFFOUT_B23n	T11	
3B	VREFB3BN0	10			DIFFIO_TX_B24n	DIFFOUT_B24n	U9	DQ2B
3B	VREFB3BN0	10	CLK1p		DIFFIO_RX_B23p	DIFFOUT B23p	R11	
3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	V10	DQ2B
4A	VREFB4AN0	10	RZQ_0		DIFFIO TX B25n	DIFFOUT B25n	U13	DQZD
4A	VREFB4AN0	10	NZQ_0		DIFFIO_RX_B26n	DIFFOUT_B26n	V13	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	U14	DQ3B
4A 4A	VREFB4AN0	10			DIFFIO_TX_B25p	DIFFOUT_B26p	V12	DQ3B DQ3B
4A 4A	VREFB4AN0	10			DIFFIO_RX_B26p	DIFFOUT B27n	M14	DQSn3B
4A	VREFB4AN0	10			DIFFIO_TX_B28n	DIFFOUT_B28n	U18	DQ3B
4A	VREFB4AN0	10	 		DIFFIO_RX_B27p	DIFFOUT_B27p	L13	DQS3B
4A	VREFB4AN0	10			DIFFIO_TX_B28p	DIFFOUT_B28p	V17	
4A	VREFB4AN0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	U17	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	V16	DQ3B
4A	VREFB4AN0	10			DIFFIO_TX_B29p	DIFFOUT_B29p	T17	DQ3B
4A	VREFB4AN0	10			DIFFIO_RX_B30p	DIFFOUT_B30p	V15	DQ3B
4A	VREFB4AN0	10	CLK2n		DIFFIO_RX_B31n	DIFFOUT_B31n	U12	
4A	VREFB4AN0	10			DIFFIO_TX_B32n	DIFFOUT_B32n	R18	DQ3B
4A	VREFB4AN0	10	CLK2p		DIFFIO_RX_B31p	DIFFOUT_B31p	T12	
4A	VREFB4AN0	10			DIFFIO_TX_B32p	DIFFOUT_B32p	P18	DQ3B
4A	VREFB4AN0	10			DIFFIO_TX_B33n	DIFFOUT_B33n	T16	
4A	VREFB4AN0	10			DIFFIO_RX_B34n	DIFFOUT_B34n	P14	DQ4B
4A	VREFB4AN0	10			DIFFIO_TX_B33p	DIFFOUT_B33p	R17	DQ4B
4A	VREFB4AN0	10			DIFFIO_RX_B34p	DIFFOUT_B34p	P15	DQ4B
4A	VREFB4AN0	10			DIFFIO_RX_B35n	DIFFOUT_B35n	M13	DQSn4B
4A	VREFB4AN0	10			DIFFIO_TX_B36n	DIFFOUT_B36n	R16	DQ4B
4A	VREFB4AN0	10			DIFFIO_RX_B35p	DIFFOUT_B35p	N12	DQS4B
4A	VREFB4AN0	Ю			DIFFIO_TX_B36p	DIFFOUT_B36p	P16	
4A	VREFB4AN0	10			DIFFIO_TX_B37n	DIFFOUT_B37n	N17	DQ4B
4A	VREFB4AN0	10			DIFFIO_RX_B38n	DIFFOUT_B38n	R13	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	N16	DQ4B
4A	VREFB4AN0	10			DIFFIO_RX_B38p	DIFFOUT_B38p	T14	DQ4B
4A	VREFB4AN0	IO	CLK3n		DIFFIO RX B39n	DIFFOUT B39n	N13	
4A	VREFB4AN0	10			DIFFIO_TX_B40n	DIFFOUT B40n	U15	DQ4B
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B39p	DIFFOUT_B39p	P13	
4A	VREFB4AN0	10	- 4		DIFFIO TX B40p	DIFFOUT B40p	T15	DQ4B
5A	VREFB5AN0	10	RZQ 1		DIFFIO_TX_B40p	DIFFOUT_R1p	L16	DQ4B DQ1R
5A	VREFB5AN0	10	1	INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	L14	2411
5A	VREFB5AN0	10		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	L15	DQ1R
5A	VREFB5AN0	10		CRC_ERROR	DIFFIO_TX_RTII	DIFFOUT_R2n	K13	שעווע
5A	VREFB5AN0	IO		nCEO	DIFFIO_RX_R2n	DIFFOUT_R3p	M18	DQ1R
				IICLU				
5A	VREFB5AN0	10			DIFFIO_RX_R4p	DIFFOUT_R4p	J13	DQ1R



								Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U324	DQS for X8
5A	VREFB5AN0	10		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	N18	DQ1R
δA	VREFB5AN0	10			DIFFIO_RX_R4n	DIFFOUT_R4n	J14	DQ1R
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	K17	
5A	VREFB5AN0	10			DIFFIO_RX_R6p	DIFFOUT_R6p	G13	DQS1R
5A	VREFB5AN0	10		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	K16	DQ1R
5A	VREFB5AN0	10			DIFFIO_RX_R6n	DIFFOUT_R6n	H13	DQSn1R
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	L17	DQ1R
5A	VREFB5AN0	10			DIFFIO_RX_R8p	DIFFOUT_R8p	J16	DQ1R
5A	VREFB5AN0	10			DIFFIO_TX_R7n	DIFFOUT_R7n	K18	
5A	VREFB5AN0	10			DIFFIO_RX_R8n	DIFFOUT_R8n	J15	DQ1R
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R9p	DIFFOUT_R9p	F14	
5B	VREFB5BN0	10			DIFFIO_TX_R10p	DIFFOUT_R10p	H17	DQ2R
5B	VREFB5BN0	10	CLK6n		DIFFIO_RX_R9n	DIFFOUT_R9n	G14	
5B	VREFB5BN0	10			DIFFIO_TX_R10n	DIFFOUT_R10n	G17	DQ2R
5B	VREFB5BN0	10			DIFFIO_RX_R11p	DIFFOUT_R11p	G15	DQ2R
5B	VREFB5BN0	10	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R12p	DIFFOUT_R12p	J18	DQ2R
5B	VREFB5BN0	10	, ,		DIFFIO_RX_R11n	DIFFOUT_R11n	H16	DQ2R
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R12n	DIFFOUT_R12n	H18	DQ2R
5B	VREFB5BN0	IO	,		DIFFIO RX R13p	DIFFOUT R13p	E16	DQS2R
5B	VREFB5BN0	IO			DIFFIO_TX_R14p	DIFFOUT_R14p	E18	
5B	VREFB5BN0	IO			DIFFIO_RX_R13n	DIFFOUT_R13n	F16	DQSn2R
5B	VREFB5BN0	IO			DIFFIO_TX_R14n	DIFFOUT_R14n	D18	DQ2R
5B	VREFB5BN0	IO			DIFFIO_RX_R15p	DIFFOUT_R15p	G18	DQ2R
5B	VREFB5BN0	IO			DIFFIO_TX_R16p	DIFFOUT_R16p	C18	DQ2R
5B	VREFB5BN0	IO			DIFFIO_RX_R15n	DIFFOUT_R15n	F17	DQ2R
5B	VREFB5BN0	IO			DIFFIO_TX_R16n	DIFFOUT_R16n	C17	
7A		GND					D15	
7A	VREFB7AN0	IO	CLK11p		DIFFIO_RX_T9p	DIFFOUT_T9p	F12	
7A	VREFB7AN0	IO			DIFFIO_TX_T10p	DIFFOUT_T10p	D16	DQ1T
7A	VREFB7AN0	IO	CLK11n		DIFFIO_RX_T9n	DIFFOUT T9n	F11	
7A	VREFB7AN0	IO			DIFFIO_TX_T10n	DIFFOUT_T10n	C16	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T11p	DIFFOUT_T11p	C13	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T12p	DIFFOUT_T12p	B14	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T11n	DIFFOUT_T11n	C12	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T12n	DIFFOUT_T12n	B15	DQ1T
7A	VREFB7AN0	10			DIFFIO_RX_T13p	DIFFOUT T13p	E12	DQS1T
7A	VREFB7AN0	IO			DIFFIO_TX_T14p	DIFFOUT T14p	B17	540
7A	VREFB7AN0	IO			DIFFIO_RX_T13n	DIFFOUT_T13n	E11	DQSn1T
7A	VREFB7AN0	10			DIFFIO TX T14n	DIFFOUT T14n	B18	DQ1T
7A	VREFB7AN0	10			DIFFIO_RX_T15p	DIFFOUT_T15p	D13	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T16p	DIFFOUT_T16p	A16	DQ1T
7A	VREFB7AN0	10			DIFFIO_RX_T15n	DIFFOUT_T15n	E14	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T16n	DIFFOUT_T16n	A17	7
7A	VREFB7AN0	10	CLK10p		DIFFIO_RX_T17p	DIFFOUT_T17p	F9	+
7A	VREFB7AN0	IO	ouop		DIFFIO_TX_T18p	DIFFOUT_T18p	A14	DQ2T
7A	VREFB7AN0	IO	CLK10n		DIFFIO_TX_T16p	DIFFOUT_T17n	F10	טעב ו
7A	VREFB7AN0	10	02.110.1		DIFFIO TX T18n	DIFFOUT T18n	A15	DQ2T
7A	VREFB7AN0	10			DIFFIO_RX_T19p	DIFFOUT T19p	C11	DQ2T
7A	VREFB7AN0	10			DIFFIO_TX_T20p	DIFFOUT_T20p	A12	DQ2T
7A	VREFB7AN0	10			DIFFIO_TX_T20p	DIFFOUT T19n	B10	DQ2T
7A 7A	VREFB7AN0	10			DIFFIO_RX_T19II	DIFFOUT_T20n	B12	DQ2T
7A	VREFB7AN0	10			DIFFIO_TX_T20f	DIFFOUT_T21p	D9	DQS2T
7A	VREFB7AN0	IO			DIFFIO_RX_121p	DIFFOUT_T22p	A11	ואסצו
								DOSpot
7A 7A	VREFB7ANO	10			DIFFIO_RX_T21n	DIFFOUT_T21n	E9 A10	DQSn2T
		10			DIFFIO_TX_T22n	DIFFOUT_T22n		DQ2T
'A	VREFB7AN0	10			DIFFIO_RX_T23p	DIFFOUT_T23p	D11	DQ2T



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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U324	DQS for X8		
7A	VREFB7AN0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	A9	DQ2T		
7A	VREFB7AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	D10	DQ2T		
7A	VREFB7AN0	IO	RZQ_2		DIFFIO_TX_T24n	DIFFOUT_T24n	B9			
8A	VREFB8AN0	IO	CLK9p		DIFFIO_RX_T25p	DIFFOUT_T25p	G6			
8A	VREFB8AN0	10			DIFFIO_TX_T26p	DIFFOUT_T26p	A7	DQ3T		
8A	VREFB8AN0	IO	CLK9n		DIFFIO_RX_T25n	DIFFOUT_T25n	F6			
8A	VREFB8AN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	A6	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	B7	DQ3T		
8A	VREFB8AN0	10	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T28p	DIFFOUT_T28p	A4	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	B8	DQ3T		
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T28n	DIFFOUT_T28n	A5	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	E8	DQS3T		
8A	VREFB8AN0	10			DIFFIO_TX_T30p	DIFFOUT_T30p	C1			
8A	VREFB8AN0	10			DIFFIO_RX_T29n	DIFFOUT_T29n	F7	DQSn3T		
8A	VREFB8AN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	C2	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	B4	DQ3T		
8A	VREFB8AN0	10			DIFFIO_TX_T32p	DIFFOUT_T32p	B3	DQ3T		
8A	VREFB8AN0	10		1	DIFFIO_TX_T32p	DIFFOUT_T32p	B5	DQ3T		
8A	VREFB8AN0	10		+	DIFFIO_RX_T31n	DIFFOUT_T31fi	C3	ונאסו		
	VKEFBOANU	MSEL0		MSEL0	DIFFIO_IX_I3ZII	DIFFOUT_132ft	J6			
9A	+			CONF DONE						
9A		CONF_DONE					C6			
9A		MSEL1		MSEL1			H5			
9A		nSTATUS		nSTATUS			D6			
9A		nCE		nCE			E4			
9A		MSEL2		MSEL2			D3			
9A		MSEL3		MSEL3			G5			
9A		nCONFIG		nCONFIG			D4			
9A		MSEL4		MSEL4			G4			
9A		GND					D5			
		GND					D12			
		GND					V18			
		GND					V14			
		GND					V4			
		GND					U1			
		GND					T13			
		GND					T3			
		GND					R10			
		GND					P17			
		GND					P12			
		GND					P7			
	1	GND					N14	1		
	+	GND		- 		 	N9	+		
	+	GND		- 		 	N4	+		
	+	GND		1		1	M12	+		
	+	GND		1			M6	+		
	+	GND		+		+	M1	+		
	+	GND		+		+	L18	+		
	+	GND				+		+		
	+						L11	+		
	+	GND					L9	+		
	+	GND					L7			
		GND					K12			
		GND					K10			
		GND					K8			
		GND					K5			
		GND					J17			
		GND					J11			



Version 1.1 Note (1)

								Note (1	
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U324	DQS for X8	
		GND					J9		
		GND					J7		
		GND					H14		
		GND					H12		
		GND					H10		
		GND					H8		
		GND					H6		
		GND					G11		
		GND					G9		
		GND					G7		
		GND					G1		
		GND					F13		
		GND					F8		
		GND					F3		
		GND					E10		
		GND		+			E5		
		GND		+			D17		
		GND					D7		
		GND					D2		
		GND			+		C4		
	_	GND					B11		
	_	GND							
		GND		+			B1		
		GND					A18		
		GND					A8		
		GND					A3		
		VCC					M11		
		VCC					L12		
		VCC					L10		
		VCC					L8		
		VCC					K11		
		VCC					K9		
		VCC					K7		
		VCC					J12		
		VCC					J10		
		VCC					J8		
		VCC					H11		
		VCC					H9		
		VCC					H7		
		VCC					G12		
		VCC					G10		
		VCC					G8		
		DNU					A2		
		DNU					B2		
		DNU					C15		
	+	DNU			+		C8		
	+	VCCPGM			+		T6		
	+	VCCPGM			+		M15		
	+	VCCPGM			+		E7	+	
		VCCBAT			+		CF.	+	
	+	VCCBAT			+		C5	+	
		VCCIO2A			+		H4	1	
		VCCIO2A			_		P2	1	
		VCCIO2A			1		L3		
		VCCIO2A			<u> </u>		J2		
		VCCIO3A					R5		
		VCCIO3A					U6		
		VCCIO3B					T8		



Note (1)

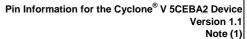
						Mote (1		
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U324	DQS for X8
		VCCIO3B					V9	
		VCCIO4A					T18	
		VCCIO4A					U16	
		VCCIO4A					U11	
		VCCIO4A					R15	
		VCCIO5A					K15	
		VCCIO5A					M16	
		VCCIO5B					F18	
		VCCIO5B					G16	
		VCCIO7A					B16	
		VCCIO7A					E15	
		VCCIO7A					C14	
		VCCIO7A					A13	
		VCCIO8A					C9	
		VCCIO8A					B6	
		VCCPD1A2A					K4	
		VCCPD1A2A					J5	
		VCCPD3A					R7	
		VCCPD3B4A					R12	
		VCCPD3B4A					R8	
		VCCPD5A					K14	
		VCCPD5B					H15	
		VCCPD7A8A					D8	
		VCCPD7A8A					E13	
2A	VREFB2AN0	VREFB2AN0					N1	
3A	VREFB3AN0	VREFB3AN0					V5	
3B	VREFB3BN0	VREFB3BN0					U10	
4A	VREFB4AN0	VREFB4AN0					V11	
5A	VREFB5AN0	VREFB5AN0					M17	
5B	VREFB5BN0	VREFB5BN0					E17	
7A	VREFB7AN0	VREFB7AN0					B13	
3A	VREFB8AN0	VREFB8AN0					C7	
		RREF_TL					A1	
		VCCA_FPLL					H3	
		VCCA_FPLL					N5	
		VCCA_FPLL					F5	
		VCCA FPLL					N15	
		VCCA_FPLL					F15	
		VCC_AUX					E6	
		VCC_AUX					C10	
		VCC_AUX					D14	
	1	VCC_AUX					R14	
		VCC_AUX					T10	
		VCC_AUX				1	R6	

Note:

(1) For more information about pin definition and pin connection guidelines, refer to the

Cyclone V Device Family Pin Connection Guidelines.

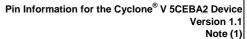
Pin List U15





									Note (1)
Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16
Number					Channel				
2A	VREFB2AN0	10			DIFFIO_TX_L9n	DIFFOUT_L9n	C1		
2A	VREFB2AN0	IO			DIFFIO_RX_L10n	DIFFOUT_L10n	L1	DQ1L	
2A	VREFB2AN0	10			DIFFIO_TX_L9p	DIFFOUT_L9p	C2	DQ1L	
2A	VREFB2AN0	IO			DIFFIO_RX_L10p	DIFFOUT_L10p	L2	DQ1L	
2A	VREFB2AN0	10			DIFFIO_RX_L11n	DIFFOUT_L11n	N1	DQSn1L	
2A	VREFB2AN0	10			DIFFIO_TX_L12n	DIFFOUT_L12n	E2	DQ1L	
2A	VREFB2AN0	10			DIFFIO_RX_L11p	DIFFOUT_L11p	N2	DQS1L	
2A	VREFB2AN0	10			DIFFIO_TX_L12p	DIFFOUT_L12p	D3		
2A	VREFB2AN0	IO			DIFFIO_TX_L13n	DIFFOUT_L13n	G1	DQ1L	
2A	VREFB2AN0	10			DIFFIO_RX_L14n	DIFFOUT_L14n	U1	DQ1L	
2A	VREFB2AN0	IO			DIFFIO_TX_L13p	DIFFOUT_L13p	G2	DQ1L	
2A	VREFB2AN0	10			DIFFIO_RX_L14p	DIFFOUT_L14p	U2	DQ1L	
								DQTL	
2A	VREFB2AN0	10			DIFFIO_RX_L15n	DIFFOUT_L15n	W2	2011	
2A	VREFB2AN0	10			DIFFIO_TX_L16n	DIFFOUT_L16n	AA1	DQ1L	
2A	VREFB2AN0	10			DIFFIO_RX_L15p	DIFFOUT_L15p	Y3		
2A	VREFB2AN0	10			DIFFIO_TX_L16p	DIFFOUT_L16p	AA2	DQ1L	
3A		TDO		TDO			V3		
3A		nCSO		DATA4			AB6		
3A		TMS		TMS			R4		
3A		AS_DATA3		DATA3			AA5		
3A	İ	TCK		TCK			V5		
3A	1	AS_DATA2		DATA2			T5	l	1
3A		TDI		TDI		 	P5		
	1					 		1	1
3A	1	AS_DATA1		DATA1			W5	 	
3A		DCLK		DCLK			M5		
3A		AS_DATA0,ASDO		DATA0			AB4		
3A		10		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	P6	DQ1B	
3A	VREFB3AN0	10		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7		
3A	VREFB3AN0	10		DATA8	DIFFIO RX B1p	DIFFOUT_B1p	N6	DQ1B	
3A	VREFB3AN0	10		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	U6	DQ1B	
3A	VREFB3AN0	IO		DATA10	DIFFIO RX B3n	DIFFOUT_B3n	M6	DQSn1B	
3A	VREFB3AN0	10		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	R5	DQ1B	
3A	VREFB3AN0	10		DATA12	DIFFIO RX B3p	DIFFOUT_B3p	M7	DQS1B	
								DQSIB	
3A	VREFB3AN0	10		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	R6		
3A	VREFB3AN0	Ю		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	R7	DQ1B	
3A	VREFB3AN0	10		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	L7	DQ1B	
3A	VREFB3AN0	10		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	T7	DQ1B	
3A	VREFB3AN0	10		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	L8	DQ1B	
3A	VREFB3AN0	10		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	T8		
3A	VREFB3AN0	10		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	P7	DQ1B	
3A	VREFB3AN0	10		PR ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	T9		
3A	VREFB3AN0	10			DIFFIO_TX_B8p	DIFFOUT_B8p	P8	DQ1B	
3B	VREFB3BN0	IO			DIFFIO_TX_B9n	DIFFOUT_B9n	V8		
3B	VREFB3BN0				DIFFIO_RX_B10n	DIFFOUT_B10n	N8	DQ2B	
		10							
3B	VREFB3BN0	IO			DIFFIO_TX_B9p	DIFFOUT_B9p	W8	DQ2B	
3B	VREFB3BN0	10			DIFFIO_RX_B10p	DIFFOUT_B10p	M8	DQ2B	
3B	VREFB3BN0	10			DIFFIO_RX_B11n	DIFFOUT_B11n	N9	DQSn2B	
3B	VREFB3BN0	10			DIFFIO_TX_B12n	DIFFOUT_B12n	AA7	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	N10	DQS2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AB7		
3B	VREFB3BN0	10			DIFFIO_TX_B13n	DIFFOUT_B13n	Y7	DQ2B	
3B	VREFB3BN0	Ю			DIFFIO_RX_B14n	DIFFOUT_B14n	U8	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B13p	DIFFOUT_B13p	W7	DQ2B	
3B	VREFB3BN0	IO			DIFFIO RX B14p	DIFFOUT B14p	V9	DQ2B	
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B15n	DIFFOUT_B15n	R9		
3B	VREFB3BN0	10	02.10.iji i EE_DE_1 Dii		DIFFIO_RX_B15II	DIFFOUT_B16n	AB8	DQ2B	
		••	OLIVA- EDILL DI ED-					DWZD	1
3B	VREFB3BN0	10	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B15p	DIFFOUT_B15p	P9	DOOD.	
3B	VREFB3BN0	10			DIFFIO_TX_B16p	DIFFOUT_B16p	AA8	DQ2B	
3B	VREFB3BN0	10			DIFFIO_TX_B17n	DIFFOUT_B17n	Y10		
3B	VREFB3BN0	10			DIFFIO_RX_B18n	DIFFOUT_B18n	AA9	DQ3B	
3B	VREFB3BN0	10			DIFFIO_TX_B17p	DIFFOUT_B17p	AA10	DQ3B	
3B	VREFB3BN0	10			DIFFIO_RX_B18p	DIFFOUT_B18p	Y9	DQ3B	
3B	VREFB3BN0	10			DIFFIO_RX_B19n	DIFFOUT_B19n	L9	DQSn3B	
3B	VREFB3BN0	IO			DIFFIO TX B20n	DIFFOUT B20n	W11	DQ3B	
3B	VREFB3BN0	10			DIFFIO_RX_B19p	DIFFOUT_B19p	M10	DQS3B	
3B	VREFB3BN0	IO				DIFFOUT_B20p	Y11	D 400D	1
3B	VREFB3BN0 VREFB3BN0		EDIT DI CINOLITA EDIT DI CINOLIT		DIFFIO_TX_B20p	DIFFOUT DOA-		DOOD	
		10	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	AB10	DQ3B	
	VDEEE				DIFFIO_RX_B22n	DIFFOUT_B22n	U10	DQ3B	1
3B	VREFB3BN0	IO							
3B 3B	VREFB3BN0	Ю	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	AB11	DQ3B	
3B			FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB CLK1n			DIFFOUT_B21p DIFFOUT_B22p DIFFOUT_B23n		DQ3B DQ3B	

Pin List U19





									Note (1)
Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16
Number					Channel				
3B	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	R11	DQ3B	
3B	VREFB3BN0	10	CLK1p		DIFFIO_RX_B23p	DIFFOUT B23p	R10		
3B	VREFB3BN0	IO			DIFFIO TX B24p	DIFFOUT B24p	P12	DQ3B	
4A	VREFB4AN0	10	RZQ 0		DIFFIO TX B25n	DIFFOUT B25n	AA13	DQOD	
			1/2/4_0					DO 4D	
4A	VREFB4AN0	10			DIFFIO_RX_B26n	DIFFOUT_B26n	W12	DQ4B	
4A	VREFB4AN0	10			DIFFIO_TX_B25p	DIFFOUT_B25p	AB13	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	Y12	DQ4B	
4A	VREFB4AN0	10			DIFFIO RX B27n	DIFFOUT_B27n	U12	DQSn4B	
4A	VREFB4AN0	10			DIFFIO_TX_B28n	DIFFOUT_B28n	R12	DQ4B	
4A	VREFB4AN0	10			DIFFIO RX B27p	DIFFOUT_B27p	T12	DQS4B	
								DQ34B	-
4A	VREFB4AN0	10			DIFFIO_TX_B28p	DIFFOUT_B28p	T13		
4A	VREFB4AN0	10			DIFFIO_TX_B29n	DIFFOUT_B29n	AB15	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	W13	DQ4B	
4A	VREFB4AN0	10			DIFFIO_TX_B29p	DIFFOUT_B29p	AB16	DQ4B	
4A	VREFB4AN0	10			DIFFIO_RX_B30p	DIFFOUT_B30p	V13	DQ4B	
4A	VREFB4AN0	IO	CLK2n		DIFFIO RX B31n	DIFFOUT_B31n	T14	DQ+D	
			CLRZN						
4A	VREFB4AN0	10			DIFFIO_TX_B32n	DIFFOUT_B32n	AB18	DQ4B	
4A	VREFB4AN0	10	CLK2p		DIFFIO_RX_B31p	DIFFOUT_B31p	U13		
4A	VREFB4AN0	10			DIFFIO_TX_B32p	DIFFOUT_B32p	AA18	DQ4B	
4A	VREFB4AN0	10			DIFFIO TX B33n	DIFFOUT_B33n	AA19		
4A	VREFB4AN0	10			DIFFIO_RX_B34n	DIFFOUT_B34n	Y14	DQ5B	DQ1B
			 						
4A	VREFB4AN0	10			DIFFIO_TX_B33p	DIFFOUT_B33p	Y19	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	W14	DQ5B	DQ1B
4A	VREFB4AN0	10			DIFFIO_RX_B35n	DIFFOUT_B35n	P14	DQSn5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO TX B36n	DIFFOUT B36n	AA20	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO RX B35p	DIFFOUT B35p	R14	DQS5B	DQ1B
4A	VREFB4AN0				DIFFIO TX B36p	DIFFOUT B36p	Y20	DQSSB	DQID
		10							
4A	VREFB4AN0	10			DIFFIO_TX_B37n	DIFFOUT_B37n	AA15	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	U15	DQ5B	DQ1B
4A	VREFB4AN0	10			DIFFIO_TX_B37p	DIFFOUT_B37p	Y15	DQ5B	DQ1B
4A	VREFB4AN0	IO			DIFFIO RX B38p	DIFFOUT B38p	V15	DQ5B	DQ1B
4A	VREFB4AN0	10	CLK3n		DIFFIO_RX_B39n	DIFFOUT_B39n	R15	DQUD	DQID
		-	CLRSII						_
4A	VREFB4AN0	10			DIFFIO_TX_B40n	DIFFOUT_B40n	AB20	DQ5B	DQ1B
4A	VREFB4AN0	10	CLK3p		DIFFIO_RX_B39p	DIFFOUT_B39p	T15		
4A	VREFB4AN0	10			DIFFIO TX B40p	DIFFOUT_B40p	AB21	DQ5B	DQ1B
4A	VREFB4AN0	10			DIFFIO_TX_B41n	DIFFOUT_B41n	AB22		
4A	VREFB4AN0	10			DIFFIO_RX_B42n	DIFFOUT_B42n	Y16	DQ6B	DQ1B
4A	VREFB4AN0	10			DIFFIO_TX_B41p	DIFFOUT_B41p	AA22	DQ6B	DQ1B
4A	VREFB4AN0	10			DIFFIO_RX_B42p	DIFFOUT_B42p	Y17	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	U16	DQSn6B	DQSn1B
4A	VREFB4AN0	10			DIFFIO_TX_B44n	DIFFOUT_B44n	AA17	DQ6B	DQ1B
4A	VREFB4AN0	10			DIFFIO_RX_B43p	DIFFOUT_B43p	U17	DQS6B	DQS1B
4A	VREFB4AN0				DIFFIO_TX_B44p	DIFFOUT_B44p	AB17	DQCOD	DQOID
		10							
4A	VREFB4AN0	10			DIFFIO_TX_B45n	DIFFOUT_B45n	Y22	DQ6B	DQ1B
4A	VREFB4AN0	10			DIFFIO_RX_B46n	DIFFOUT_B46n	V18	DQ6B	DQ1B
4A	VREFB4AN0	10			DIFFIO TX B45p	DIFFOUT B45p	Y21	DQ6B	DQ1B
4A	VREFB4AN0	10			DIFFIO_RX_B46p	DIFFOUT_B46p	W18	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO RX B47n	DIFFOUT B47n	W16	† ·	<u> </u>
			 					DOCD	DOAD
4A	VREFB4AN0	10			DIFFIO_TX_B48n		W21	DQ6B	DQ1B
4A	VREFB4AN0	10			DIFFIO_RX_B47p	DIFFOUT_B47p	W17	 	
4A	VREFB4AN0	IO			DIFFIO_TX_B48p		W22	DQ6B	DQ1B
5A	VREFB5AN0	10	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	U22	DQ1R	
5A	VREFB5AN0	10		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	V20		
5A	VREFB5AN0	10		PR REQUEST	DIFFIO TX R1n	DIFFOUT R1n	U21	DQ1R	t
		••	 					DAIL.	
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	V19	 	
5A	VREFB5AN0	10		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	T19	DQ1R	
5A	VREFB5AN0	10	<u> </u>		DIFFIO_RX_R4p	DIFFOUT_R4p	T17	DQ1R	<u> </u>
5A	VREFB5AN0	10		CvP CONFDONE	DIFFIO TX R3n	DIFFOUT R3n	T20	DQ1R	
5A	VREFB5AN0	IO		_ ` ` ` ` ` ` ` ` ` ` ` ` ` ` ` ` ` ` `	DIFFIO RX R4n	DIFFOUT R4n	T18	DQ1R	
5A	VREFB5AN0	IO	 	DEV_OE	DIFFIO TX R5p	DIFFOUT R5p	T22		
5.4			 	DL V_UE				D004D	
5A	VREFB5AN0	Ю			DIFFIO_RX_R6p	DIFFOUT_R6p	R16	DQS1R	.
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	R22	DQ1R	
5A	VREFB5AN0	10			DIFFIO_RX_R6n	DIFFOUT_R6n	R17	DQSn1R	
5A	VREFB5AN0	10			DIFFIO TX R7p	DIFFOUT R7p	R20	DQ1R	
5A	VREFB5AN0	10			DIFFIO_RX_R8p	DIFFOUT_R8p	R19	DQ1R	t
4			 					PAII/	
5A	VREFB5AN0	10			DIFFIO_TX_R7n	DIFFOUT_R7n	R21	 	.
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	P19	DQ1R	
	VIDEEDEDING	10	CLK6p		DIFFIO_RX_R9p	DIFFOUT_R9p	L17	1	
5B	VREFB5BN0								
	VREFB5BN0 VREFB5BN0	IO			DIFFIO TX R10p	DIFFOUT_R10p	E20	DQ2R	l i
5B			CLK6n		DIFFIO_TX_R10p DIFFIO_RX_R9n	DIFFOUT_R10p DIFFOUT_R9n	E20 K17	DQ2R	





									Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16
5B	VREFB5BN0	10			DIFFIO_RX_R11p	DIFFOUT_R11p	H20	DQ2R	
5B	VREFB5BN0	10	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R12p	DIFFOUT_R12p	G18	DQ2R	1
5B	VREFB5BN0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	H19	DQ2R	
5B		IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R12n	DIFFOUT R12n	G17	DQ2R	
5B	VREFB5BN0	IO			DIFFIO_RX_R13p	DIFFOUT_R13p	K16	DQS2R	
5B		IO			DIFFIO_TX_R14p	DIFFOUT_R14p	F19	1	
5B	VREFB5BN0	10			DIFFIO_RX_R13n	DIFFOUT_R13n	J16	DQSn2R	+
5B	VREFB5BN0	10			DIFFIO_TX_R14n	DIFFOUT R14n	F18	DQ2R	+
5B	VREFB5BN0	10			DIFFIO_RX_R15p	DIFFOUT_R15p	J17	DQ2R	+
5B	VREFB5BN0	10			DIFFIO_TX_R16p	DIFFOUT R16p	J19	DQ2R DQ2R	+
		••							+
5B	VREFB5BN0	IO			DIFFIO_RX_R15n	DIFFOUT_R15n	J18	DQ2R	
5B	VREFB5BN0	10			DIFFIO_TX_R16n	DIFFOUT_R16n	H18		
7A		GND				<u> </u>	F17		
7A	VREFB7AN0	Ю			DIFFIO_RX_T1p	DIFFOUT_T1p	H16		
7A	VREFB7AN0	10			DIFFIO_TX_T2p	DIFFOUT_T2p	C21	DQ1T	DQ1T
7A	VREFB7AN0	10		1	DIFFIO_RX_T1n	DIFFOUT_T1n	G16		
7A	VREFB7AN0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	C20	DQ1T	DQ1T
7A	VREFB7AN0	10			DIFFIO_RX_T3p	DIFFOUT_T3p	D18	DQ1T	DQ1T
7A	VREFB7AN0	10			DIFFIO_TX_T4p	DIFFOUT_T4p	B20	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO RX T3n	DIFFOUT_T3n	E17	DQ1T	DQ1T
7A	VREFB7AN0	10			DIFFIO TX T4n	DIFFOUT_T4n	B21	DQ1T	DQ1T
7A		IO			DIFFIO RX T5p	DIFFOUT T5p	G15	DQS1T	DQS1T
7A	VREFB7AN0	10			DIFFIO_TX_T6p	DIFFOUT_T6p	B22	24011	154511
7A 7A		IO			DIFFIO_TX_T6p	DIFFOUT_T5n	G14	DQSn1T	DQSn1T
									
7A	VREFB7AN0	IO		└	DIFFIO_TX_T6n	DIFFOUT_T6n	A22	DQ1T	DQ1T
7A		10			DIFFIO_RX_T7p	DIFFOUT_T7p	E16	DQ1T	DQ1T
7A	VREFB7AN0	10			DIFFIO_TX_T8p	DIFFOUT_T8p	A20	DQ1T	DQ1T
7A		10			DIFFIO_RX_T7n	DIFFOUT_T7n	D17	DQ1T	DQ1T
7A	VREFB7AN0	10		1	DIFFIO_TX_T8n	DIFFOUT_T8n	A19		
7A	VREFB7AN0	10	CLK11p		DIFFIO_RX_T9p	DIFFOUT_T9p	G13		
7A	VREFB7AN0	10			DIFFIO TX T10p	DIFFOUT_T10p	C19	DQ2T	DQ1T
7A	VREFB7AN0	10	CLK11n		DIFFIO_RX_T9n	DIFFOUT_T9n	F14		1
7A		IO			DIFFIO TX T10n	DIFFOUT_T10n	C18	DQ2T	DQ1T
7A	VREFB7AN0	10			DIFFIO_RX_T11p	DIFFOUT_T11p	C16	DQ2T	DQ1T
7A	VREFB7AN0	10		 	DIFFIO_TX_T12p	DIFFOUT_T12p	B16	DQ2T	DQ1T
7A		IO IO			DIFFIO_RX_T11n	DIFFOUT_T11n	C15		DQ1T
7A 7A					DIFFIO_RX_T11h	DIFFOUT_T12n	B15	DQ2T DQ2T	DQ1T
		IO							
7A		10			DIFFIO_RX_T13p	DIFFOUT_T13p	G12	DQS2T	DQ1T
7A	VREFB7AN0	10			DIFFIO_TX_T14p	DIFFOUT_T14p	A18		
7A	VREFB7AN0	10			DIFFIO_RX_T13n	DIFFOUT_T13n	H12	DQSn2T	DQ1T
7A	VREFB7AN0	10			DIFFIO_TX_T14n	DIFFOUT_T14n	A17	DQ2T	DQ1T
7A	VREFB7AN0	10			DIFFIO_RX_T15p	DIFFOUT_T15p	F15	DQ2T	DQ1T
7A	VREFB7AN0	10		1	DIFFIO_TX_T16p	DIFFOUT_T16p	B18	DQ2T	DQ1T
7A	VREFB7AN0	IO		1	DIFFIO_RX_T15n	DIFFOUT_T15n	E14	DQ2T	DQ1T
7A	VREFB7AN0	10			DIFFIO_TX_T16n	DIFFOUT_T16n	B17		
7A	VREFB7AN0	10	CLK10p		DIFFIO RX T17p	DIFFOUT_T17p	H10	1	1
7A	VREFB7AN0	10			DIFFIO_TX_T18p	DIFFOUT_T18p	A15	DQ3T	1
7A	VREFB7AN0	10	CLK10n		DIFFIO_RX_T17n	DIFFOUT_T17n	G11	1	1
7A	VREFB7AN0	10			DIFFIO_TX_T18n	DIFFOUT_T18n	A14	DQ3T	†
7A	VREFB7AN0	IO	<u> </u>		DIFFIO_TX_T18II	DIFFOUT_T19p	D13	DQ3T	+
7A	VREFB7AN0	10			DIFFIO_TX_T20p	DIFFOUT_T20p	C14	DQ3T	+
7A 7A			 					DQ3T	+
	VREFB7AN0	10			DIFFIO_RX_T19n	DIFFOUT_T19n	C13		+
7A	VREFB7AN0	IO		└	DIFFIO_TX_T20n	DIFFOUT_T20n	D14	DQ3T	
7A	VREFB7AN0	10		└	DIFFIO_RX_T21p	DIFFOUT_T21p	H9	DQS3T	
7A	VREFB7AN0				DIFFIO_TX_T22p	DIFFOUT_T22p	A13	↓	4
7A	VREFB7AN0	10			DIFFIO_RX_T21n	DIFFOUT_T21n	G8	DQSn3T	1
7A	VREFB7AN0	10		<u> </u>	DIFFIO_TX_T22n	DIFFOUT_T22n	B13	DQ3T	<u> </u>
7A	VREFB7AN0	10		1	DIFFIO_RX_T23p	DIFFOUT_T23p	E12	DQ3T	
7A	VREFB7AN0	10			DIFFIO_TX_T24p	DIFFOUT_T24p	B12	DQ3T	
7A	VREFB7AN0	10			DIFFIO_RX_T23n	DIFFOUT_T23n	F12	DQ3T	
7A	VREFB7AN0	IO	RZQ_2		DIFFIO_TX_T24n	DIFFOUT_T24n	A12	1	1
8A	VREFB8AN0	IO	CLK9p		DIFFIO RX T25p	DIFFOUT T25p	G10	1	1
8A	VREFB8AN0	10	02.100		DIFFIO_TX_T26p	DIFFOUT_T26p	C11	DQ4T	†
8A	VREFB8AN0	10	CLK9n			DIFFOUT_T25n	F10	DQ-11	+
			OLINOII		DIFFIO_RX_T25n			DOAT	+
8A	VREFB8AN0	10			DIFFIO_TX_T26n	DIFFOUT_T26n	B11	DQ4T	+
8A	VREFB8AN0	IO		├	DIFFIO_RX_T27p	DIFFOUT_T27p	D11	DQ4T	
8A	VREFB8AN0	10	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T28p	DIFFOUT_T28p	A8	DQ4T	
8A	VREFB8AN0	10			DIFFIO_RX_T27n	DIFFOUT_T27n	E11	DQ4T	
	LUDEEDOANIO	10	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn	1	DIFFIO TX T28n	DIFFOUT_T28n	A7	DQ4T	I
8A	VREFB8AN0		11 EE_1E_0E10011,11 EE_1E_0E100111						
8A 8A	VREFB8AN0 VREFB8AN0	10	THE TE OF THE TEST		DIFFIO_RX_T29p	DIFFOUT_T29p	J9	DQS4T	



									Note (1)
Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16
umber		-			Channel				
A		IO			DIFFIO_RX_T29n	DIFFOUT_T29n	J8	DQSn4T	
A		IO			DIFFIO_TX_T30n	DIFFOUT_T30n	E7	DQ4T	
Α		10			DIFFIO_RX_T31p	DIFFOUT_T31p	C10	DQ4T	
A		IO			DIFFIO_TX_T32p	DIFFOUT_T32p	C6	DQ4T	
A .		10			DIFFIO_RX_T31n	DIFFOUT_T31n	C9	DQ4T	
A		10	OLIVO EDILI TI ED		DIFFIO_TX_T32n	DIFFOUT_T32n	D7		
A	VREFB8AN0	IO IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T33p	DIFFOUT_T33p	K7	DOST	
A A	VREFB8AN0	10	CLK8n,FPLL_TL_FBn		DIFFIO_TX_T34p DIFFIO_RX_T33n	DIFFOUT_T34p	A10 J7	DQ5T	
BA		10	CLK8n,FPLL_TL_FBn		DIFFIO_RX_133n DIFFIO_TX_T34n	DIFFOUT_T33n DIFFOUT_T34n	A9	DQ5T	
BA	VREFB8AN0	10			DIFFIO_TX_T34n DIFFIO_RX_T35p	DIFFOUT_T34n	D9	DQ5T	
BA		10			DIFFIO_RX_T35p DIFFIO_TX_T36p	DIFFOUT_T36p	B6	DQ5T	
BA	VREFB8AN0	10			DIFFIO_TX_T35p	DIFFOUT_T35n	D8	DQ5T	
A		10			DIFFIO_RX_T35II	DIFFOUT_T36n	B5	DQ5T	
A	VREFB8AN0	10			DIFFIO_TX_T36II	DIFFOUT_T37p	H8	DQS5T	
A	VREFB8AN0	10			DIFFIO_TX_T38p	DIFFOUT_T38p	C8	DQSST	
A	VREFB8AN0	10			DIFFIO_TX_T35p	DIFFOUT_T37n	G7	DQSn5T	
A	VREFB8AN0	10			DIFFIO_TX_T38n	DIFFOUT_T38n	B8	DQ5T5T	
A	VREFB8AN0	10			DIFFIO_TX_T38II DIFFIO_RX_T39p	DIFFOUT_T39p	H6	DQ5T	
A	VREFB8AN0	10			DIFFIO_TX_T40p	DIFFOUT_T40p	E6	DQ5T	
A A	VREFB8AN0	10			DIFFIO_TX_T40p DIFFIO_RX_T39n	DIFFOUT_T39n	G6	DQ5T DQ5T	
A A	VREFB8AN0 VREFB8AN0	10			DIFFIO_RX_139n DIFFIO_TX_T40n	DIFFOUT_T40n	F7	ופשטו	1
A A	AIVEL DOWING	MSEL0		MSEL0	DII 1 10_1 A_14011	DIT 001_140II	L6	1	
)A	1	CONF_DONE		CONF_DONE	 		J6	1	
A	1	MSEL1		MSEL1	 		K6		
A A	 				-		G5		-
A A		nSTATUS nCE		nSTATUS nCE			H5		
							A2		
A A		MSEL2 MSEL3		MSEL2 MSEL3			E5		
							A4		
A		nCONFIG		nCONFIG					
A		MSEL4		MSEL4			C5 F3		
Α		GND					A21		
		GND GND					AB19		
		GND					AB2		
		GND			-		AB1		
		GND					AA16		
		GND					AA11		
		GND					AA4		
		GND					AA3		
		GND			-		Y13		
		GND					Y8		
		GND					Y5		
		GND					Y2		
		GND					Y1		
	1	GND			1		W20	1	-
	1	GND			1		W4		
	ļ	GND			ļ		W3	ļ	ļ
	1	GND			1		V22	1	-
		GND			1		V17	1	
	1	GND			1		V4		
	ļ	GND			ļ		V2	ļ	ļ
	ļ	GND			ļ		V1	ļ	ļ
		GND					U19		
		GND					U14		
		GND					U9		
		GND					U5		
		GND					U4		
		GND					U3		
		GND					T11		
		GND					T2		
		GND					T1		
		GND					R13		
		GND					R3		
		GND					P10		
		GND					P4		
		GND					P2		
		GND					P1		
		GND					N22		
		GND					N15		
•		GND					N13		



Emulated LVDS Output Channel DQS for X16 Pin Name/Function Optional Function(s) Configuration Function Dedicated Tx/Rx U484 DQS for X8 GND GND N5 GND GND N3 GND M19 M14 M12 GND GND GND М9 M4 GND M2 M1 GND GND GND L16 GND L13 GND GND GND K14 GND GND K12 GND K10 GND GND K4 K2 GND GND GND J20 GND J15 GND J13 GND J11 J5 GND GND J3 GND H14 GND GND GND H2 H1 GND GND G9 GND GND G4 G3 GND GND F16 F11 GND GND F6 GND F5 F2 GND GND GND E13 GND E4 GND E3 D20 D10 GND GND GND D5 GND GND D2 D1 GND C22 GND C7 GND GND GND GND C3 B14 GND B2 GND A11 GND GND L4 P15 VCC VCC VCC P13 VCC P3 N14 VCC N4 VCC M15



									14016 (1)
	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16
Number					Channel				
		VCC					M13		
		VCC					M11		
		VCC					L14		
		VCC					L12		
		VCC					L10		
		VCC					K13		
		VCC					K11		
		VCC					K9		
		VCC					K5		
		VCC					КЗ		
		VCC					J14		
		VCC		1			J12		
		VCC					J12		
		VCC					J4		
		VCC					H15		
		VCC					H13		
		VCC					H11		
		DNU					B3		
		DNU					B4		
-		DNU					D21		
	1	DNU					E10		
		VCCPGM					Y6		
	İ	VCCPGM			1		U20		
		VCCPGM			İ		B7		
	1	VCCBAT		1	1		A3	1	1
		VCCIO2A			†		D4	1	
		VCCIO2A VCCIO2A		+			Y4		
							R1		
		VCCIO2A					J1		
		VCCIO2A							
		VCCIO3A					T6		
		VCCIO3A					AA6		
		VCCIO3B					R8		
		VCCIO3B					AB9		
		VCCIO3B					W10		
		VCCIO3B					V7		
		VCCIO4A					T16		
		VCCIO4A					AB14		
		VCCIO4A					AA21		
		VCCIO4A					Y18		
		VCCIO4A					W15		
		VCCIO4A					V12		
		VCCIO5A					T21		
		VCCIOSA VCCIOSA		1			R18		
				1					
		VCCIO5B					G19		
		VCCIO5B					P20		
		VCCIO5B					N17		
		VCCIO5B					L21		
		VCCIO5B					K18		
		VCCIO5B		ļ			H22		
		VCCIO7A					B19		
-		VCCIO7A					H17		
		VCCIO7A					E18		
		VCCIO7A					D15		
	İ	VCCIO7A			1		C12		
		VCCIO7A			İ		A16		
	1	VCCIO8A		1	1		B9	1	1
	1	VCCIOSA VCCIOSA		†	1		H7	1	1
	 	VCCIOSA VCCIOSA	<u> </u>		†		E8		
	1	VCCIOSA VCCIOSA	 	+	1		A6	1	1
	1	VCCIOSA VCCPD1A2A	 	+	1		R2	1	1
	 	VOORDAAA			 		J2	-	
	-	VCCPD1A2A		1	_			1	-
	ļ	VCCPD1A2A			ļ		E1		
		VCCPD3A					V6		
		VCCPD3B4A					W9		
		VCCPD3B4A					V16		
		VCCPD3B4A					V14		
		VCCPD3B4A					V10		
		VCCPD5A					P17		
	İ	VCCPD5B					M18		
		VCCPD5B			İ		N19		
	1	VCCPD7A8A		†	1		E15	1	
	1	DINON	l .	I	1	l .	- 10	1	



									Note (1)
	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16
Number					Channel				
		VCCPD7A8A					F13		
		VCCPD7A8A					F9		
		VCCPD7A8A					E9		
2A	VREFB2AN0	VREFB2AN0					W1		
3A	VREFB3AN0	VREFB3AN0					W6		
3B	VREFB3BN0	VREFB3BN0					AB12		
	VREFB4AN0	VREFB4AN0					AA14		†
	VREFB5AN0	VREFB5AN0					V21		
	VREFB5BN0	VREFB5BN0		1			K20		
3D	VREFB7AN0	VREFB7AN0							
7A	VREFB/ANU	VREFB/ANU					D16		
8A	VREFB8AN0	VREFB8AN0					B10		
		NC					AB3		
		NC					V11		
		NC					P22		
		NC					P21		
		NC				1	P18		
		NC					P16		
		NC			İ	İ	N21		
		NC					N20		
	 	NC	<u> </u>		†	†	N18		
		NC NC		1	 	1	N16		
	-	NC		-	-	+	M22	-	
		NC					M21		
		NC					M20		
		NC					M17		
		NC					M16		
		NC					L22		
		NC					L20		
		NC					L19		
		NC					L18		
		NC					L15		
		NC					K22		
		NC					K21		†
		NC					K19		†
		NC					K15		
							100		
		NC					J22 J21		
		NC							
		NC					H21		
		NC					G22		
		NC					G21		
		NC					G20		
		NC					F22		
		NC					E22		
		NC					E21		
		NC					D22		
		RREF_TL					A1		
		VCCA_FPLL			İ	İ	M3		
	1	VCCA_FPLL		†	†	†	T3	1	t
		VCCA_FPLL				1	T4	<u> </u>	
		VCCA_FPLL VCCA_FPLL		1	 	1	F4		
	-	VCCA_FPLL VCCA_FPLL		-	-	+	U18	-	
	 	VOCA FRIL		 	 			-	
		VCCA_FPLL				1	E19	ļ	-
		VCC_AUX			ļ		D6		
		VCC_AUX					D12		
		VCC_AUX					D19		
		VCC_AUX					W19		
		VCC_AUX VCC_AUX					AA12		

Pin List U19

Note

(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.



						Emulated LVDS Output Channel F355 DOS for					
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F256	DQS for X8			
A	VREFB2AN0	Ю			DIFFIO_TX_L9n	DIFFOUT_L9n	F3				
4	VREFB2AN0	IO			DIFFIO_RX_L10n	DIFFOUT_L10n	G3	DQ1L			
1	VREFB2AN0	IO			DIFFIO_TX_L9p	DIFFOUT_L9p	F4	DQ1L			
	VREFB2AN0	Ю			DIFFIO_RX_L10p	DIFFOUT_L10p	H3	DQ1L			
١	VREFB2AN0	Ю			DIFFIO_RX_L11n	DIFFOUT_L11n	H4	DQSn1L			
A	VREFB2AN0	10			DIFFIO_TX_L12n	DIFFOUT L12n	E2	DQ1L			
4	VREFB2AN0	10			DIFFIO_RX_L11p	DIFFOUT_L11p	H5	DQS1L			
A	VREFB2AN0	10			DIFFIO TX L12p	DIFFOUT L12p	F2				
١	VREFB2AN0	IO			DIFFIO_TX_L13n	DIFFOUT_L13n	G1	DQ1L			
١	VREFB2AN0	IO			DIFFIO RX L14n	DIFFOUT L14n	J2	DQ1L			
4	VREFB2AN0	IO			DIFFIO_TX_L13p	DIFFOUT_L13p	G2	DQ1L			
A	VREFB2AN0	IO			DIFFIO_RX_L14p	DIFFOUT_L14p	J3	DQ1L			
<u>. </u>	VREFB2AN0	IO			DIFFIO RX L15n	DIFFOUT L15n	K4	54.2			
\ \	VREFB2AN0	IO			DIFFIO_TX_L16n	DIFFOUT_L16n	H1	DQ1L			
,	VREFB2AN0	10			DIFFIO_RX_L15p	DIFFOUT_L15p	K5	DQTE			
\	VREFB2AN0	IO IO			DIFFIO_TX_L16p	DIFFOUT_L16p	J1	DQ1L			
\	VILLI DZANO	TDO		TDO	Dil LIO_LV_F10h	DII 1 001_L10p	M6	DOIL			
\	+	nCSO		DATA4	1		L3	+			
	+	TMS		TMS	+	+	L3 L6				
4	 				+	+					
<u> </u>	+	AS_DATA3		DATA3	1		M2				
Α		TCK		TCK			M3				
4		AS_DATA2		DATA2			L2				
١		TDI		TDI			L4				
١		AS_DATA1		DATA1			K1				
١		DCLK		DCLK			M5				
4		AS_DATA0,ASDO		DATA0			M1				
4	VREFB3AN0	Ю		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	N4	DQ1B			
4	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	N1				
4	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	P4	DQ1B			
A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	P1	DQ1B			
Ą	VREFB3AN0	Ю		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	M7	DQSn1B			
4	VREFB3AN0	Ю		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	R1	DQ1B			
4	VREFB3AN0	10		DATA12	DIFFIO RX B3p	DIFFOUT B3p	L7	DQS1B			
4	VREFB3AN0	10		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	P2				
١	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	P3	DQ1B			
\	VREFB3AN0	IO		DATA13	DIFFIO TX B6n	DIFFOUT B6n	T2	DQ1B			
<u>. </u>	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	N3	DQ1B			
\	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	R2	DQ1B			
\ \	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	R6	54.5			
\	VREFB3AN0	lo		PR_READY	DIFFIO_RX_B/II DIFFIO_TX_B8n	DIFFOUT B8n	T3	DQ1B			
١	VREFB3AN0	lo		PR_ERROR	DIFFIO_TX_B6ff DIFFIO_RX_B7p	DIFFOUT_B80	P7	סוטט			
\	VREFB3AN0	lo		FIX_ERROR	DIFFIO_TX_B8p	DIFFOUT_B8p	R4	DQ1B			
3								סואט			
	VREFB3BN0	10			DIFFIO_TX_B17n	DIFFOUT_B17n	T5	DOOD			
3	VREFB3BN0	10			DIFFIO_RX_B18n	DIFFOUT_B18n	R7	DQ2B			
3	VREFB3BN0	10			DIFFIO_TX_B17p	DIFFOUT_B17p	T4	DQ2B			
3	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B18p	P8	DQ2B			
1	VREFB3BN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	M8	DQSn2B			
3	VREFB3BN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	T7	DQ2B			
3	VREFB3BN0	Ю			DIFFIO_RX_B19p	DIFFOUT_B19p	L9	DQS2B			
3	VREFB3BN0	Ю			DIFFIO_TX_B20p	DIFFOUT_B20p	T8				
3	VREFB3BN0	Ю	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFOUT_B21n	R11	DQ2B			
3	VREFB3BN0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	T12	DQ2B			
3	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	R12	DQ2B			
В	VREFB3BN0	10			DIFFIO_RX_B22p	DIFFOUT_B22p	T13	DQ2B			



								Note (1
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F256	DQS for X8
3B	VREFB3BN0	Ю	CLK1n		DIFFIO_RX_B23n	DIFFOUT B23n	R9	
3B	VREFB3BN0	IO			DIFFIO TX B24n	DIFFOUT B24n	T10	DQ2B
BB	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B23p	DIFFOUT_B23p	P9	
3B	VREFB3BN0	10			DIFFIO_TX_B24p	DIFFOUT B24p	R10	DQ2B
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B25n	DIFFOUT_B25n	R15	
1A	VREFB4AN0	IO	1.124_0		DIFFIO_RX_B26n	DIFFOUT B26n	T15	DQ3B
1A	VREFB4AN0	IO			DIFFIO TX B25p	DIFFOUT B25p	P16	DQ3B
1A	VREFB4AN0	10			DIFFIO_RX_B26p	DIFFOUT_B26p	R16	DQ3B
1A	VREFB4AN0	10			DIFFIO RX B27n	DIFFOUT B27n	M10	DQSn3B
1A	VREFB4AN0	IO			DIFFIO_TX_B28n	DIFFOUT B28n	M13	DQ3B
1A	VREFB4AN0	IO			DIFFIO RX B27p	DIFFOUT B27p	L10	DQS3B
1A	VREFB4AN0	10			DIFFIO_TX_B28p	DIFFOUT_B28p	N14	DQOOD
1A	VREFB4AN0	10			DIFFIO_TX_B29n	DIFFOUT_B29n	P14	DQ3B
1A	VREFB4AN0	10			DIFFIO RX B30n	DIFFOUT B30n	M12	DQ3B
1A	VREFB4AN0	IO			DIFFIO_TX_B29p	DIFFOUT_B29p	P13	DQ3B
1A	VREFB4AN0	10			DIFFIO_RX_B30p	DIFFOUT_B30p	M11	DQ3B
1A	VREFB4AN0	10	CLK2n		DIFFIO_RX_B31n	DIFFOUT B31n	P11	ראים
1A	VREFB4AN0	10	OLIVAII	+	DIFFIO_RX_B31fi DIFFIO_TX_B32n	DIFFOUT_B31fi	T14	DQ3B
1A	VREFB4AN0	10	CLK2p	+	DIFFIO_TX_B32ff DIFFIO_RX_B31p	DIFFOUT_B32ft	N11	ספאס
1A	VREFB4AN0	10	CLRZP		DIFFIO_RX_B31p	DIFFOUT B32p	R14	DQ3B
5A	VREFB5AN0	10	RZQ 1		DIFFIO_TX_B32p	DIFFOUT R1p	N15	DQ3B DQ1R
	VREFB5AN0		RZQ_I	INIT DONE	DIFFIO_TX_R1p	DIFFOUT_R2p	L13	DQIK
5A		10		_				DOAD
5A	VREFB5AN0	10		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	N16	DQ1R
5A	VREFB5AN0	10		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	K14	DOAD
5A	VREFB5AN0	10		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	H16	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	L14	DQ1R
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	J16	DQ1R
5A	VREFB5AN0	IO		5511.05	DIFFIO_RX_R4n	DIFFOUT_R4n	L15	DQ1R
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	G15	
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	K12	DQS1R
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	G16	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	J12	DQSn1R
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	J14	DQ1R
5A	VREFB5AN0	Ю			DIFFIO_RX_R8p	DIFFOUT_R8p	K15	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	H15	
5A	VREFB5AN0	Ю			DIFFIO_RX_R8n	DIFFOUT_R8n	K16	DQ1R
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R9p	DIFFOUT_R9p	F12	
5B	VREFB5BN0	IO			DIFFIO_TX_R10p	DIFFOUT_R10p	E16	DQ2R
5B	VREFB5BN0	Ю	CLK6n		DIFFIO_RX_R9n	DIFFOUT_R9n	G12	
5B	VREFB5BN0	Ю			DIFFIO_TX_R10n	DIFFOUT_R10n	D16	DQ2R
5B	VREFB5BN0	Ю			DIFFIO_RX_R11p	DIFFOUT_R11p	E12	DQ2R
5B	VREFB5BN0	Ю	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R12p	DIFFOUT_R12p	B16	DQ2R
5B	VREFB5BN0	Ю			DIFFIO_RX_R11n	DIFFOUT_R11n	D13	DQ2R
5B	VREFB5BN0	Ю	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R12n	DIFFOUT_R12n	C16	DQ2R
5B	VREFB5BN0	Ю			DIFFIO_RX_R13p	DIFFOUT_R13p	H13	DQS2R
5B	VREFB5BN0	Ю			DIFFIO_TX_R14p	DIFFOUT_R14p	B15	
5B	VREFB5BN0	Ю			DIFFIO_RX_R13n	DIFFOUT_R13n	G13	DQSn2R
5B	VREFB5BN0	Ю			DIFFIO_TX_R14n	DIFFOUT_R14n	C15	DQ2R
5B	VREFB5BN0	Ю			DIFFIO_RX_R15p	DIFFOUT_R15p	F14	DQ2R
5B	VREFB5BN0	Ю			DIFFIO_TX_R16p	DIFFOUT_R16p	D14	DQ2R
5B	VREFB5BN0	Ю			DIFFIO_RX_R15n	DIFFOUT_R15n	F15	DQ2R
5B	VREFB5BN0	Ю			DIFFIO_TX_R16n	DIFFOUT_R16n	E15	
7A		GND					C14	
7A	VREFB7AN0	IO	CLK10p		DIFFIO_RX_T17p	DIFFOUT_T17p	F11	



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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F256	DQS for X8					
'A	VREFB7AN0	Ю			DIFFIO_TX_T18p	DIFFOUT_T18p	A15	DQ1T					
Ą	VREFB7AN0	Ю	CLK10n		DIFFIO_RX_T17n	DIFFOUT_T17n	F10						
4	VREFB7AN0	Ю			DIFFIO_TX_T18n	DIFFOUT_T18n	A14	DQ1T					
4	VREFB7AN0	10			DIFFIO_RX_T19p	DIFFOUT_T19p	D11	DQ1T					
4	VREFB7AN0	Ю			DIFFIO_TX_T20p	DIFFOUT_T20p	A13	DQ1T					
A	VREFB7AN0	IO			DIFFIO_RX_T19n	DIFFOUT T19n	C11	DQ1T					
λ	VREFB7AN0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	A12	DQ1T					
<u>. </u>	VREFB7AN0	10			DIFFIO RX T21p	DIFFOUT T21p	E10	DQS1T					
<u>.</u> \	VREFB7AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	B12	240					
<u>, </u>	VREFB7AN0	10			DIFFIO_RX_T21n	DIFFOUT_T21n	E9	DQSn1T					
A	VREFB7AN0	IO			DIFFIO_TX_T22n	DIFFOUT T22n	B11	DQ1T					
Α	VREFB7AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	C10	DQ1T					
Α	VREFB7AN0	10			DIFFIO TX T24p	DIFFOUT T24p	B10	DQ1T					
4	VREFB7AN0	10		+	DIFFIO_TX_T24p	DIFFOUT_T23n	C9	DQ1T					
4	VREFB7AN0	10	RZQ 2		DIFFIO_RX_123II DIFFIO_TX_T24n	DIFFOUT_T24n	A10	DQTT					
			_										
Α	VREFB8AN0	IO IO	CLK9p		DIFFIO_RX_T25p	DIFFOUT_T25p	F8	DOOT					
Α	VREFB8AN0	IO .	laure.		DIFFIO_TX_T26p	DIFFOUT_T26p	A8	DQ2T					
Α	VREFB8AN0	IO	CLK9n		DIFFIO_RX_T25n	DIFFOUT_T25n	F7						
4	VREFB8AN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	A9	DQ2T					
4	VREFB8AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	B8	DQ2T					
A	VREFB8AN0	Ю	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T28p	DIFFOUT_T28p	A5	DQ2T					
4	VREFB8AN0	Ю			DIFFIO_RX_T27n	DIFFOUT_T27n	A7	DQ2T					
١	VREFB8AN0	Ю	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T28n	DIFFOUT_T28n	A4	DQ2T					
4	VREFB8AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	D8	DQS2T					
4	VREFB8AN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	B3						
4	VREFB8AN0	Ю			DIFFIO_RX_T29n	DIFFOUT_T29n	D7	DQSn2T					
A	VREFB8AN0	Ю			DIFFIO_TX_T30n	DIFFOUT_T30n	A3	DQ2T					
A	VREFB8AN0	10			DIFFIO_RX_T31p	DIFFOUT_T31p	B7	DQ2T					
A	VREFB8AN0	10			DIFFIO_TX_T32p	DIFFOUT_T32p	C3	DQ2T					
A	VREFB8AN0	Ю			DIFFIO_RX_T31n	DIFFOUT_T31n	В6	DQ2T					
A	VREFB8AN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	C4						
A		MSEL0		MSEL0			E5						
Α		CONF DONE		CONF DONE			C1						
A		MSEL1		MSEL1			E4						
Α		nSTATUS		nSTATUS			D1						
<u> </u>		nCE		nCE			E1						
4		MSEL2		MSEL2			D2						
	-												
<u> </u>		MSEL3		MSEL3			E6						
<u> </u>		nCONFIG		nCONFIG			D3						
<u> </u>	1	MSEL4		MSEL4			F6						
4	-	GND					D4						
	1	GND					H12						
	1	GND					T16						
		GND					T6						
		GND					T1						
		GND					R13						
		GND					P10						
		GND					P5						
		GND					N2						
		GND					M14						
	1	GND					M9						
	1	GND					M4						
	+	GND					L11	+					
	111	10.10	1	i			1-11	1					



Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F256	DQS for X8
		GND					K13	
		GND					K10	
		GND					K8	
		GND					K6	
		GND					J11	
		GND					J9	
		GND					J7	
		GND					J5	
		GND					H10	
		GND					H8	
		GND					H6	
		GND					G11	
		GND					G9	
		GND					G7	
		GND					G4	
		GND					F16	
		GND					F1	
		GND		1		<u> </u>	E13	1
		GND					E8	
		GND					E3	
		GND						
		GND					D10	
		GND					D5	
		GND					C2	
		GND					B9	
		GND					B1	
		GND					A16	
		GND					A11	
		GND					A6	
		VCC					F9	
		VCC					L8	
		VCC					K11	
		vcc					K9	
		VCC VCC					K7	
		VCC					J10	
		VCC					J8	
		VCC					J6	
		VCC					H11	
		VCC					H9	
		VCC					H7	
		VCC					G10	
		VCC					G8	
	-	VCC					00	
		VCC					G6	
		DNU					B2	
		DNU					A2	
		DNU		-			C13	
		DNU					C8	
		VCCPGM					P6	
		VCCPGM					M15	
		VCCPGM					C6	
		VCCBAT					C5	
		VCCIO2A					H2	
		VCCIO2A					K3	
		VCCIO3A					N7	
		VCCIO3A					R3	



Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F256	DQS for X8
		VCCIO3B					R8	
		VCCIO3B					T11	
		VCCIO4A					N12	
		VCCIO4A					P15	
		VCCIO5A					J15	
		VCCIO5A					L16	
		VCCIO5B					D15	
		VCCIO5B					G14	
		VCCIO7A					B14	
		VCCIO7A					C12	
		VCCIO8A					C7	
		VCCIO8A					B4	
		VCCPD1A2A					J4	
		VCCPD3A					N6	
		VCCPD3B4A					N10	
		VCCPD3B4A					N8	
		VCCPD5A					J13	
		VCCPD5B					H14	
		VCCPD7A8A					E7	
		VCCPD7A8A					E11	
A	VREFB2AN0	VREFB2AN0					K2	
A	VREFB3AN0	VREFB3AN0					R5	
В	VREFB3BN0	VREFB3BN0					T9	
A	VREFB4AN0	VREFB4AN0					P12	
A	VREFB5AN0	VREFB5AN0					M16	
В	VREFB5BN0	VREFB5BN0					E14	
4	VREFB7AN0	VREFB7AN0					B13	
4	VREFB8AN0	VREFB8AN0					B5	
		RREF_TL					A1	
		VCCA_FPLL					G5	
		VCCA_FPLL					L5	
		VCCA_FPLL					F5	
		VCCA_FPLL					L12	
		VCCA_FPLL					F13	
		VCC_AUX					D6	
		VCC_AUX					D9	
		VCC_AUX					D12	
		VCC_AUX					N13	
		VCC_AUX					N9	
		VCC_AUX					N5	

Note:

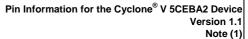
(1) For more information about pin definition and pin connection guidelines, refer to the

Cyclone V Device Family Pin Connection Guidelines.





									Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16
2A	VREFB2AN0	IO			DIFFIO_TX_L9n	DIFFOUT L9n	C1		
2A		IO			DIFFIO_RX_L10n	DIFFOUT_L10n	G1	DQ1L	
2A		10			DIFFIO_TX_L9p	DIFFOUT_L9p	C2	DQ1L	
2A		IO			DIFFIO_RX_L10p	DIFFOUT_L10p	G2	DQ1L	
2A	VREFB2AN0	10			DIFFIO_RX_L11n	DIFFOUT_L11n	E2	DQSn1L	
2A		IO			DIFFIO_TX_L12n	DIFFOUT_L12n	L1	DQ1L	
2A	VREFB2AN0	10			DIFFIO_RX_L11p	DIFFOUT_L11p	D3	DQS1L	
2A	VREFB2AN0	10			DIFFIO TX L12p	DIFFOUT L12p	L2	DQSTL	
2A	VREFB2AN0	IO			DIFFIO_TX_L13n	DIFFOUT_L13n	N1	DQ1L	
24	VREFB2AN0	10			DIFFIO_TX_L13II	DIFFOUT_L13n	U1	DQ1L DQ1L	
2A 2A		10					N2		
2A 2A		-			DIFFIO_TX_L13p	DIFFOUT_L13p		DQ1L DQ4L	
	VREFB2AN0	10			DIFFIO_RX_L14p	DIFFOUT_L14p	U2	DQ1L	
2A	VREFB2AN0	10			DIFFIO_RX_L15n	DIFFOUT_L15n	W2	2011	
2A		IO			DIFFIO_TX_L16n	DIFFOUT_L16n	AA1	DQ1L	
2A	VREFB2AN0	10			DIFFIO_RX_L15p	DIFFOUT_L15p	Y3		
2A	VREFB2AN0	10			DIFFIO_TX_L16p	DIFFOUT_L16p	AA2	DQ1L	
3A		TDO		TDO			M5		
3A		nCSO		DATA4			R4		
3A		TMS		TMS			P5		
3A		AS_DATA3		DATA3			T4		
3A		TCK		TCK			V5		
3A		AS_DATA2		DATA2			AA5		
3A		TDI		TDI			W5		
3A		AS_DATA1		DATA1			AB3		
3A		DCLK		DCLK			V3		
3A	ĺ	AS_DATA0,ASDO		DATA0			AB4		
3A		IO		DATA6	DIFFIO_RX_B1n	DIFFOUT B1n	R6	DQ1B	
3A		10		DATA5	DIFFIO TX B2n	DIFFOUT B2n	U7		
3A		IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	R5	DQ1B	
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	U8	DQ1B	
3A		IO		DATA10	DIFFIO RX B3n	DIFFOUT B3n	P6	DQSn1B	
3A	VREFB3AN0	IO		DATA9	DIFFIO_RX_B3II DIFFIO_TX_B4n	DIFFOUT_B4n	W8	DQ1B	
3A		10		DATA12	DIFFIO_IX_B4II	DIFFOUT_B3p	N6		
3A	VREFB3AN0 VREFB3AN0	10					W9	DQS1B	
				DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p		2012	
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	T7	DQ1B	
3A		10		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	U6	DQ1B	
3A		10		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	T8	DQ1B	
3A		10		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	V6	DQ1B	
3A	VREFB3AN0	10		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	M6		
3A	VREFB3AN0	10		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	R7	DQ1B	
3A	VREFB3AN0	10		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	M7		
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	P7	DQ1B	
3B	VREFB3BN0	10			DIFFIO_TX_B9n	DIFFOUT_B9n	AB6		
3B	VREFB3BN0	10			DIFFIO_RX_B10n	DIFFOUT_B10n	V9	DQ2B	
3B	VREFB3BN0	10			DIFFIO_TX_B9p	DIFFOUT_B9p	AB5	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B10p	DIFFOUT_B10p	V10	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	P8	DQSn2B	
3B	VREFB3BN0	10			DIFFIO_TX_B12n	DIFFOUT_B12n	AA7	DQ2B	
3B	VREFB3BN0	10		1	DIFFIO_RX_B11p	DIFFOUT_B11p	N8	DQS2B	
3B	VREFB3BN0	10			DIFFIO_TX_B12p	DIFFOUT_B12p	AB7	54525	
3B	VREFB3BN0	IO IO	<u> </u>		DIFFIO_TX_B13n	DIFFOUT_B13n	AA8	DQ2B	
3B	VREFB3BN0	IO			DIFFIO_TX_B13II DIFFIO_RX_B14n	DIFFOUT_B14n	T9	DQ2B DQ2B	
3B	VREFB3BN0	10		 	DIFFIO_RX_B14II DIFFIO_TX_B13p	DIFFOUT_B13p	AB8	DQ2B DQ2B	
									-
3B	VREFB3BN0	10	CLK0n,FPLL BL FBn		DIFFIO_RX_B14p	DIFFOUT_B14p	U10	DQ2B	
3B	VREFB3BN0	10	ULNUII,FFLL_BL_FBII		DIFFIO_RX_B15n	DIFFOUT_B15n	M8	DOOD	
3B	VREFB3BN0	10			DIFFIO_TX_B16n	DIFFOUT_B16n	AA10	DQ2B	
3B	VREFB3BN0	10	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B15p	DIFFOUT_B15p	M9		
3B	VREFB3BN0	10			DIFFIO_TX_B16p	DIFFOUT_B16p	AA9	DQ2B	
3B	VREFB3BN0	10		ļ	DIFFIO_TX_B17n	DIFFOUT_B17n	Y10		
3B	VREFB3BN0	Ю			DIFFIO_RX_B18n	DIFFOUT_B18n	T10	DQ3B	
3B	VREFB3BN0	10			DIFFIO_TX_B17p	DIFFOUT_B17p	Y9	DQ3B	
3B	VREFB3BN0	10			DIFFIO_RX_B18p	DIFFOUT_B18p	R9	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	U11	DQSn3B	
3B	VREFB3BN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	R12	DQ3B	
3B	VREFB3BN0	10			DIFFIO_RX_B19p	DIFFOUT_B19p	U12	DQS3B	
3B	VREFB3BN0	10			DIFFIO_TX_B20p	DIFFOUT_B20p	P12		
3B	VREFB3BN0	IO	FPLL BL CLKOUT1,FPLL BL CLKOUTn		DIFFIO TX B21n	DIFFOUT_B21n	AB10	DQ3B	
3B	VREFB3BN0	10			DIFFIO RX B22n	DIFFOUT B22n	R10	DQ3B	
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFOUT_B21p	AB11	DQ3B	
3B	VREFB3BN0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	R11	DQ3B	
3B	VREFB3BN0	IO	CLK1n		DIFFIO RX B23n	DIFFOUT_B23n	P9		
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									Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16
3B	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT B24n	Y11	DQ3B	
3B	VREFB3BN0		CLK1p		DIFFIO_RX_B23p		N9	5 405	
3B	VREFB3BN0		OEATP		DIFFIO_TX_B24p		AA12	DQ3B	
4A	VREFB4AN0		RZQ_0		DIFFIO_TX_B25n		AB13	DQOD	
4A	VREFB4AN0		1124_0		DIFFIO_RX_B26n		V13	DQ4B	
4A	VREFB4AN0				DIFFIO_TX_B25p		AB12	DQ4B	
4A	VREFB4AN0				DIFFIO_RX_B26p		U13	DQ4B	
4A 4A	VREFB4AN0				DIFFIO_RX_B26p		T12	DQSn4B	
4A 4A	VREFB4AN0				DIFFIO_TX_B28n		AA14	DQ3114B DQ4B	
4A 4A	VREFB4AN0				DIFFIO_TX_B28II		T13	DQ\$4B	<u> </u>
4A 4A							AA13	DQ54B	+
	VREFB4AN0				DIFFIO_TX_B28p			DO 4D	
4A	VREFB4AN0				DIFFIO_TX_B29n		AB15	DQ4B	
4A	VREFB4AN0				DIFFIO_RX_B30n		Y14	DQ4B	.
4A	VREFB4AN0				DIFFIO_TX_B29p		AA15	DQ4B	
4A	VREFB4AN0				DIFFIO_RX_B30p		Y15	DQ4B	
4A	VREFB4AN0		CLK2n		DIFFIO_RX_B31n		V14		
4A	VREFB4AN0				DIFFIO_TX_B32n		AB17	DQ4B	
4A	VREFB4AN0		CLK2p		DIFFIO_RX_B31p		V15		
4A	VREFB4AN0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	AB18	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AB20		
4A	VREFB4AN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	Y16	DQ5B	DQ1B
4A	VREFB4AN0	10			DIFFIO_TX_B33p	DIFFOUT_B33p	AB21	DQ5B	DQ1B
4A	VREFB4AN0				DIFFIO_RX_B34p		Y17	DQ5B	DQ1B
4A	VREFB4AN0				DIFFIO RX B35n		T14	DQSn5B	DQ1B
4A	VREFB4AN0				DIFFIO_TX_B36n		AA17	DQ5B	DQ1B
4A		10			DIFFIO RX B35p		U15	DQS5B	DQ1B
4A	VREFB4AN0				DIFFIO_TX_B36p		AA18	DQOOD	DQID
4A	VREFB4AN0				DIFFIO TX B37n		AA19	DQ5B	DQ1B
4A	VREFB4AN0				DIFFIO RX B38n		V20	DQ5B	DQ1B
4A 4A	VREFB4AN0				DIFFIO_RX_B30II		AA20	DQ5B	DQ1B
4A		10	OLIVO		DIFFIO_RX_B38p		W19	DQ5B	DQ1B
4A		10	CLK3n		DIFFIO_RX_B39n		V16		
4A	VREFB4AN0				DIFFIO_TX_B40n		AB22	DQ5B	DQ1B
4A		10	CLK3p		DIFFIO_RX_B39p		W16		
4A	VREFB4AN0				DIFFIO_TX_B40p		AA22	DQ5B	DQ1B
4A		IO			DIFFIO_TX_B41n		Y22		
4A	VREFB4AN0				DIFFIO_RX_B42n		Y20	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_TX_B41p		W22	DQ6B	DQ1B
4A	VREFB4AN0	10			DIFFIO_RX_B42p	DIFFOUT_B42p	Y19	DQ6B	DQ1B
4A	VREFB4AN0	IO			DIFFIO_RX_B43n		P14	DQSn6B	DQSn1B
4A	VREFB4AN0	Ю			DIFFIO_TX_B44n	DIFFOUT_B44n	Y21	DQ6B	DQ1B
4A	VREFB4AN0				DIFFIO_RX_B43p		R14	DQS6B	DQS1B
4A		10			DIFFIO_TX_B44p		W21		
4A		IO			DIFFIO_TX_B45n		U22	DQ6B	DQ1B
4A		10			DIFFIO_RX_B46n		V19	DQ6B	DQ1B
4A		10			DIFFIO_TX_B45p		V21	DQ6B	DQ1B
4A 4A		10			DIFFIO_TX_B45p		V21 V18	DQ6B	DQ1B DQ1B
4A 4A		10			DIFFIO_RX_B46p		U16	D40D	מושט
								DOCE	DO4B
4A		10			DIFFIO_TX_B48n	DIFFOUT_B48n	U21	DQ6B	DQ1B
4A		10			DIFFIO_RX_B47p		U17	D00D	2012
4A		10	070 4		DIFFIO_TX_B48p		U20	DQ6B	DQ1B
5A		10	RZQ_1		DIFFIO_TX_R1p		T19	DQ1R	
5A		10		INIT_DONE	DIFFIO_RX_R2p		T18		
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n		T20	DQ1R	
5A		IO		CRC_ERROR	DIFFIO_RX_R2n		T17		
5A		IO		nCEO	DIFFIO_TX_R3p		T22	DQ1R	
5A		IO			DIFFIO_RX_R4p	DIFFOUT_R4p	T15	DQ1R	1
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n		R22	DQ1R	
5A		10			DIFFIO_RX_R4n		R15	DQ1R	
5A	VREFB5AN0			DEV_OE	DIFFIO_TX_R5p		R21		
5A		10		_	DIFFIO_RX_R6p		R16	DQS1R	
5A		10		DEV_CLRn	DIFFIO TX R5n		P22	DQ1R	
5A	VREFB5AN0				DIFFIO_RX_R6n		R17	DQSn1R	
5A	VREFB5AN0				DIFFIO TX R7p		P19	DQ1R	1
5A	VREFB5AN0				DIFFIO_TX_R/p		P16	DQ1R DQ1R	
5A 5A	VREFB5AN0				DIFFIO_RX_R8p		P18	שאמווע	1
								DO4D	1
5A 5B	VREFB5AN0		OLIVO-		DIFFIO_RX_R8n		P17	DQ1R	
215	VREFB5BN0		CLK6p		DIFFIO_RX_R9p DIFFIO_TX_R10p		N16	B00B	
						DIFFOUT R10p	N20	DQ2R	1
5B	VREFB5BN0		la					DQLIT	
5B 5B 5B		IO	CLK6n		DIFFIO_RX_R9n	DIFFOUT_R9n	M16 N21	DQ2R	





									Note (1)
Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16
Number					Channel				_
5B	VREFB5BN0	10			DIFFIO_RX_R11p	DIFFOUT_R11p	N19	DQ2R	_
5B	VREFB5BN0	10	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R12p	DIFFOUT_R12p	M22	DQ2R	_
5B	VREFB5BN0	10	FRU DR GUYGUTA FRU DR GUYGUT		DIFFIO_RX_R11n	DIFFOUT_R11n	M18	DQ2R	_
5B	VREFB5BN0	10	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R12n	DIFFOUT_R12n	L22	DQ2R	_
5B 5B	VREFB5BN0	10			DIFFIO_RX_R13p	DIFFOUT_R13p	K17 M20	DQS2R	
	VREFB5BN0				DIFFIO_TX_R14p	DIFFOUT_R14p		DOO 00	
5B	VREFB5BN0	10			DIFFIO_RX_R13n	DIFFOUT_R13n	L17	DQSn2R	_
5B	VREFB5BN0	10			DIFFIO_TX_R14n	DIFFOUT_R14n	M21	DQ2R	-
5B	VREFB5BN0	10			DIFFIO_RX_R15p	DIFFOUT_R15p	L19	DQ2R	_
5B	VREFB5BN0	10			DIFFIO_TX_R16p	DIFFOUT_R16p	K21	DQ2R	
5B	VREFB5BN0	10			DIFFIO_RX_R15n	DIFFOUT_R15n	L18	DQ2R	
5B	VREFB5BN0	10			DIFFIO_TX_R16n	DIFFOUT_R16n	K22		
7A		GND					F17		
7A	VREFB7AN0	Ю			DIFFIO_RX_T1p	DIFFOUT_T1p	K20		
7A	VREFB7AN0	10			DIFFIO_TX_T2p	DIFFOUT_T2p	B16	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	K19		
7A	VREFB7AN0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	C16	DQ1T	DQ1T
7A	VREFB7AN0	10			DIFFIO_RX_T3p	DIFFOUT_T3p	D17	DQ1T	DQ1T
7A	VREFB7AN0	10			DIFFIO_TX_T4p	DIFFOUT_T4p	G17	DQ1T	DQ1T
7A	VREFB7AN0	10			DIFFIO_RX_T3n	DIFFOUT_T3n	E16	DQ1T	DQ1T
7A	VREFB7AN0	10			DIFFIO_TX_T4n	DIFFOUT_T4n	G16	DQ1T	DQ1T
7A	VREFB7AN0	10			DIFFIO_RX_T5p	DIFFOUT_T5p	G18	DQS1T	DQS1T
7A	VREFB7AN0	IO			DIFFIO TX T6p	DIFFOUT T6p	J19	1	1
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T5n	H18	DQSn1T	DQSn1T
7A	VREFB7AN0	IO			DIFFIO_TX_T6n	DIFFOUT_T6n	J18	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO RX T7p	DIFFOUT T7p	E15	DQ1T	DQ1T
7A		IO			DIFFIO_TX_T8p	DIFFOUT T8p	A15	DQ1T	DQ1T
7A	VREFB7AN0	10		†	DIFFIO RX T7n	DIFFOUT T7n	F15	DQ1T	DQ1T
7A		IO		†	DIFFIO_TX_T8n	DIFFOUT T8n	A14	DQTI	DQTI
7A	VREFB7AN0	10	CLK11p		DIFFIO_RX_T9p	DIFFOUT_T9p	H16		_
7A	VREFB7AN0	10	CERTIP		DIFFIO_TX_T10p	DIFFOUT_T10p	J17	DQ2T	DQ1T
7A 7A	VREFB7AN0	10	CLK11n				H15	DQZI	DQTI
			CLKTIN	 	DIFFIO_RX_T9n	DIFFOUT_T9n		DOOT	DOLT
7A		10		 	DIFFIO_TX_T10n	DIFFOUT_T10n	K16	DQ2T	DQ1T
7A	VREFB7AN0	10			DIFFIO_RX_T11p	DIFFOUT_T11p	C15	DQ2T	DQ1T
7A	VREFB7AN0	10			DIFFIO_TX_T12p	DIFFOUT_T12p	G15	DQ2T	DQ1T
7A	VREFB7AN0	10			DIFFIO_RX_T11n	DIFFOUT_T11n	B15	DQ2T	DQ1T
7A		10			DIFFIO_TX_T12n	DIFFOUT_T12n	F14	DQ2T	DQ1T
7A	VREFB7AN0				DIFFIO_RX_T13p	DIFFOUT_T13p	H14	DQS2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T14p	DIFFOUT_T14p	B13		
7A	VREFB7AN0				DIFFIO_RX_T13n	DIFFOUT_T13n	J13	DQSn2T	DQ1T
7A	VREFB7AN0	10			DIFFIO_TX_T14n	DIFFOUT_T14n	A13	DQ2T	DQ1T
7A	VREFB7AN0	10			DIFFIO_RX_T15p	DIFFOUT_T15p	E14	DQ2T	DQ1T
7A	VREFB7AN0	10			DIFFIO_TX_T16p	DIFFOUT_T16p	J11	DQ2T	DQ1T
7A	VREFB7AN0	10			DIFFIO_RX_T15n	DIFFOUT_T15n	F13	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T16n	DIFFOUT_T16n	H10		
7A	VREFB7AN0	10	CLK10p		DIFFIO_RX_T17p	DIFFOUT_T17p	H13		
7A	VREFB7AN0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	G11	DQ3T	
7A	VREFB7AN0	10	CLK10n		DIFFIO_RX_T17n	DIFFOUT_T17n	G13		
7A	VREFB7AN0	10			DIFFIO_TX_T18n	DIFFOUT_T18n	F12	DQ3T	
7A	VREFB7AN0	10			DIFFIO_RX_T19p	DIFFOUT_T19p	D13	DQ3T	
7A	VREFB7AN0	10			DIFFIO_TX_T20p	DIFFOUT_T20p	B12	DQ3T	
7A	VREFB7AN0	10			DIFFIO_RX_T19n	DIFFOUT_T19n	C13	DQ3T	
7A	VREFB7AN0	10			DIFFIO_TX_T20n	DIFFOUT_T20n	A12	DQ3T	1
7A	VREFB7AN0	10			DIFFIO RX T21p	DIFFOUT_T21p	H11	DQS3T	1
7A	VREFB7AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	L8		1
7A	VREFB7AN0	10			DIFFIO RX T21n	DIFFOUT T21n	G12	DQSn3T	1
7A	VREFB7AN0	10			DIFFIO_TX_T22n	DIFFOUT T22n	K9	DQ3T	1
7A	VREFB7AN0	IO			DIFFIO RX T23p	DIFFOUT T23p	D12	DQ3T	1
7A	VREFB7AN0	In			DIFFIO_TX_T24p	DIFFOUT_T24p	C11	DQ3T	+
7A	VREFB7AN0	IO			DIFFIO RX T23n	DIFFOUT T23n	E12	DQ3T	+
7A	VREFB7AN0	IO	RZQ 2		DIFFIO_TX_T24n	DIFFOUT_T24n	B11		+
8A	VREFB/AN0	10	CLK9p		DIFFIO_TX_T24II	DIFFOUT_T25p	G10	+	+
8A 8A	VREFB8AN0 VREFB8AN0	10	CENSP		DIFFIO_RX_125p DIFFIO_TX_T26p	DIFFOUT_T26p	L7	DQ4T	+
8A	VREFB8AN0	lio	CLK9n		DIFFIO_TX_T26p DIFFIO_RX_T25n	DIFFOUT_126p	F10	DQ41	+
8A 8A	VREFB8AN0 VREFB8AN0	IO IO	CEVALI	-				DQ4T	+
				-	DIFFIO_TX_T26n	DIFFOUT_T26n	K7		+
8A	VREFB8AN0	10	FRU TI OLIKOUTS FRU TI SUUSIE TEU T		DIFFIO_RX_T27p	DIFFOUT_T27p	J7	DQ4T	+
8A	VREFB8AN0	10	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T28p	DIFFOUT_T28p	H8	DQ4T	
8A	VREFB8AN0	10			DIFFIO_RX_T27n	DIFFOUT_T27n	J8	DQ4T	
8A	VREFB8AN0	10	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T28n	DIFFOUT_T28n	G8	DQ4T	
		IO	1	1	LINEELO DY TOON	HINEROLIT TOOK	J9	DQS4T	
8A 8A	VREFB8AN0 VREFB8AN0	IO			DIFFIO_RX_T29p DIFFIO_TX_T30p	DIFFOUT_T29p DIFFOUT_T30p	A10	DQ341	



									Note (1)
Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16
Number				_	Channel				
8A	VREFB8AN0	10			DIFFIO_RX_T29n	DIFFOUT_T29n	H9	DQSn4T	
8A	VREFB8AN0	10			DIFFIO_TX_T30n	DIFFOUT_T30n	A9	DQ4T	
8A	VREFB8AN0	10			DIFFIO_RX_T31p	DIFFOUT_T31p	B10	DQ4T	
8A	VREFB8AN0	10			DIFFIO_TX_T32p	DIFFOUT_T32p	A5	DQ4T	
8A	VREFB8AN0	10			DIFFIO_RX_T31n	DIFFOUT_T31n	C9	DQ4T	
8A	VREFB8AN0	10			DIFFIO_TX_T32n	DIFFOUT_T32n	B5		
8A	VREFB8AN0	10	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T33p	DIFFOUT_T33p	E10		
8A	VREFB8AN0	10			DIFFIO_TX_T34p	DIFFOUT_T34p	B6	DQ5T	
8A	VREFB8AN0	10	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T33n	DIFFOUT_T33n	F9		
8A	VREFB8AN0	10			DIFFIO_TX_T34n	DIFFOUT_T34n	B7	DQ5T	
8A	VREFB8AN0	10			DIFFIO_RX_T35p	DIFFOUT_T35p	A8	DQ5T	
8A	VREFB8AN0	10			DIFFIO_TX_T36p	DIFFOUT_T36p	C6	DQ5T	
8A	VREFB8AN0	10			DIFFIO_RX_T35n	DIFFOUT_T35n	A7	DQ5T	
8A	VREFB8AN0	10			DIFFIO_TX_T36n	DIFFOUT_T36n	D6	DQ5T	
8A	VREFB8AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	E9	DQS5T	
8A	VREFB8AN0	10			DIFFIO_TX_T38p	DIFFOUT_T38p	D7	D00 5T	
8A	VREFB8AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	D9	DQSn5T	
8A	VREFB8AN0	10			DIFFIO_TX_T38n	DIFFOUT_T38n	C8	DQ5T	
8A	VREFB8AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	G6	DQ5T	
8A	VREFB8AN0	10			DIFFIO_TX_T40p	DIFFOUT_T40p	F7	DQ5T	
8A	VREFB8AN0	10			DIFFIO_RX_T39n	DIFFOUT_T39n	H6	DQ5T	
8A	VREFB8AN0	IO NOTICE		MOST	DIFFIO_TX_T40n	DIFFOUT_T40n	E7	ļ	
9A	1	MSEL0		MSEL0	1	-	L6	1	1
9A		CONF_DONE		CONF_DONE			K6	1	1
9A		MSEL1		MSEL1			J6		
9A	ļ	nSTATUS		nSTATUS	ļ		H5	ļ	ļ
9A		nCE		nCE			G5		
9A		MSEL2		MSEL2			A2		
9A		MSEL3		MSEL3			E5		
9A		nCONFIG		nCONFIG			A4		
9A		MSEL4		MSEL4			F3		
9A		GND					C5		
		GND					P2		
		GND					AB19		
		GND					AB14		
		GND					AB9		
		GND					AB2		
		GND					AB1		
		GND					AA11		
		GND					AA6		
		GND					AA4		
		GND					AA3		
		GND					Y18		
		GND					Y5		
		GND					Y2		
		GND					Y1		
		GND					W4		
		GND					W3		
		GND					V22		
		GND					V17		
		GND					V12		
		GND					V7		
		GND					V4		
		GND					V2		
		GND					V1		
		GND					U9		
		GND					U5		
		GND					U4		
		GND					U3		
		GND					T21		
		GND					T16		
		GND					T2		
		GND					T1		
		GND					R13		
		GND					R3		
		GND					P10		
		GND					P4		
	İ	GND					P1		
		GND					N22		
		GND					N17		
	İ	GND					N15		
		i -							

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GND

GND

VCC VCC VCC

VCC

VCC

VCC

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A21 A11

N4 P15 P13

P11

N14 N12

M15

M13

Note (1) Emulated LVDS Output Channel DQS for X8 DQS for X16 Pin Name/Function Optional Function(s) Configuration Function Dedicated Tx/Rx F484 GND N13 N11 GND N7 GND GND N5 GND N3 M14 M12 GND GND GND M10 M4 GND M2 M1 GND GND GND L21 GND L15 GND L13 GND L11 GND GND K14 GND GND K12 GND GND K8 K4 GND GND K2 GND K1 GND J20 GND J15 GND GND GND H22 GND H12 GND GND GND НЗ H2 GND GND H1 GND GND G19 G9 GND G4 GND F16 GND GND GND F5 F2 GND GND GND E13 GND E4 GND E3 D20 D10 GND GND GND D5 GND GND D2 D1 GND C17 GND C3 GND GND B14 GND GND B9 B2 GND В1



									Note (1)
	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16
Number					Channel				
		VCC					M11		
		VCC					L16		
		VCC					L14		
		VCC					L12		
		VCC					L10		
		VCC					L4		
		VCC			1		K15		
		VCC					K13		
		VCC					K11		
		VCC					K5		
		VCC					K3		
		VCC			 	 	J16	t	†
		VCC				 	J14		
		VCC				 	J12		
		VCC				 	J12 J10		
		VCC				 	J10		
		VCC					J4		
		DNU				1	B3		
		DNU					B4		
		DNU					E17		
		DNU					L9		
		VCCPGM					V8		
		VCCPGM					R19		
		VCCPGM			1		F8		
		VCCBAT					A3		
		VCCIO2A					D4		
		VCCIO2A VCCIO2A			 		Y4		
		VCCIO2A VCCIO2A			+		R1	 	
					 		J1		
		VCCIO2A							
		VCCIO3A					T6		
		VCCIO3A					Y8		
		VCCIO3B					T11		
		VCCIO3B			!	1	Y13		
		VCCIO3B			1		W10		
		VCCIO3B					R8		
		VCCIO4A					U19		
		VCCIO4A			+		AA21	<u> </u>	
		VCCIO4A			+	 	AA16	<u> </u>	
		VCCIO4A VCCIO4A					W20		
		VCCIO4A				 	VV20		-
		VCCIO4A					W15		
		VCCIO4A				1	U14		
		VCCIO5A					P20		
		VCCIO5A					R18		
		VCCIO5B					M19		
		VCCIO5B			!	1	K18		
		VCCIO7A			1		A16		
		VCCIO7A					H17		
		VCCIO7A					G14		
		VCCIO7A			†		F21	 	t
		VCCIO7A			 		F11		
		VCCIO7A VCCIO7A			 	 	E18		
					 				
		VCCIO7A			 		D15		
		VCCIO7A			 		C22		
		VCCIO7A			ļ		C12		
		VCCIO7A			ļ		B19		
		VCCIO8A					A6	L	
		VCCIO8A					G7		
		VCCIO8A					E8		
		VCCIO8A					C7		
		VCCPD1A2A		İ			E1		
		VCCPD1A2A VCCPD1A2A		1	†		R2	t	t
		VCCPD1A2A VCCPD1A2A			 		J2		
					 		W6		
		VCCPD3A			 				
		VCCPD3B4A			<u> </u>		W17		
		VCCPD3B4A			ļ		W14		
		VCCPD3B4A					W12		
		VCCPD3B4A				1	W11		
_		VCCPD5A					P21		
		VCCPD5B					N18		
		1			+			1	1
		VCCPD5B			1	l l	M17		
		VCCPD5B VCCPD7A8A			1		M17 D16	 	



									14016 (1)
Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16
Number					Channel	· ·			
		VCCPD7A8A					D14		
		VCCPD7A8A		İ			D8		
		VCCPD7A8A					C10		
2A	VREFB2AN0	VREFB2AN0					W1		
3A	VREFB3AN0	VREFB3AN0					Y7	+	-
3B	VREFB3BN0	VREFB3BN0					Y12		
4A	VREFB4AN0	VREFB4AN0					AB16		
5A	VREFB5AN0	VREFB5AN0					R20		
5B	VREFB5BN0	VREFB5BN0					L20		
7A	VREFB7AN0	VREFB7AN0					C14		
8A	VREFB8AN0	VREFB8AN0					B8		
		NC					Y6		
		NC					V11		
		NC					J22	+	-
		NC					J21		
		NC					H21		
		NC					H20		
		NC					G22		
		NC					G21		
		NC					G20	İ	İ
		NC					F22		
		NC NC					F20	+	-
		NC					F19		
		NC					F18		
		NC					E22		
		NC					E21		
		NC					E20		
		NC					E19		
		NC		İ			D22		
		NC					D21		
		NC					D19		
		NC NC					C21	+	-
		NC							
		NC					C20		
		NC					C19		
		NC					C18		
		NC					B22		
		NC					B21		
		NC		İ			B20		
		NC					B18		
		NC NC					B17		
			<u> </u>			 		-	-
		NC					A22	 	
		NC					A20		
		NC					A19	ļ	ļ
		NC					A18		
,		NC					A17		
		RREF_TL					A1		
		VCCA_FPLL					M3		
		VCCA_FPLL				i	T3	1	1
		VCCA_FPLL					T5	 	
		VCCA_FPLL VCCA_FPLL			1			 	
		VOCA_FPLL					F4	 	
		VCCA_FPLL			ļ		U18	-	-
	l	VCCA_FPLL			ļ		H19	ļ	1
		VCC_AUX					E6		
		VCC_AUX					D11		
		VCC_AUX					D18		
		VCC_AUX					W18	İ	İ
		VCC_AUX					W13	İ	İ
		VCC_AUX	 	i	<u> </u>		W7		
	l	VUU_NUN	l .	1	I	l .	vv /	I	L

Note

(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.



Version Number	Date	Changes Made
1.0	9/20/2012	Initial release.
1.1	10/5/2012	Removed nPERST* pins because Cyclone V E devices do not support PCIe interface.