ECE 346 HW # 1

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Question 1)

lui $s0, 0x1001

op	rs	rt	imm
001111	00000	10000	0001000000000001

xori $s1, $s0, -10

op	rs	rt	imm
001110	10000	10001	1111111111110111

lui $s2,0x222

op	rs	rt	imm
001111	00000	10010	0000001000100010

add $s3,$s1,$s2

op	rs	rt	rd	sham	funct
000000	10001	10010	10011	00000	100000

sw $s3,4($s0)

op	rs	rt	im
101011	10000	10011	0000000000000100

1.2)

Function Type	Register	address
lui	$s0	0x10010000
xori	$s1	0x1000FFF7
lui	$s2	0x02220000
add	$s3	0x1222FFF7
sw	all	take contents of $s3 offset it by 4 bits of the base address ($s0)

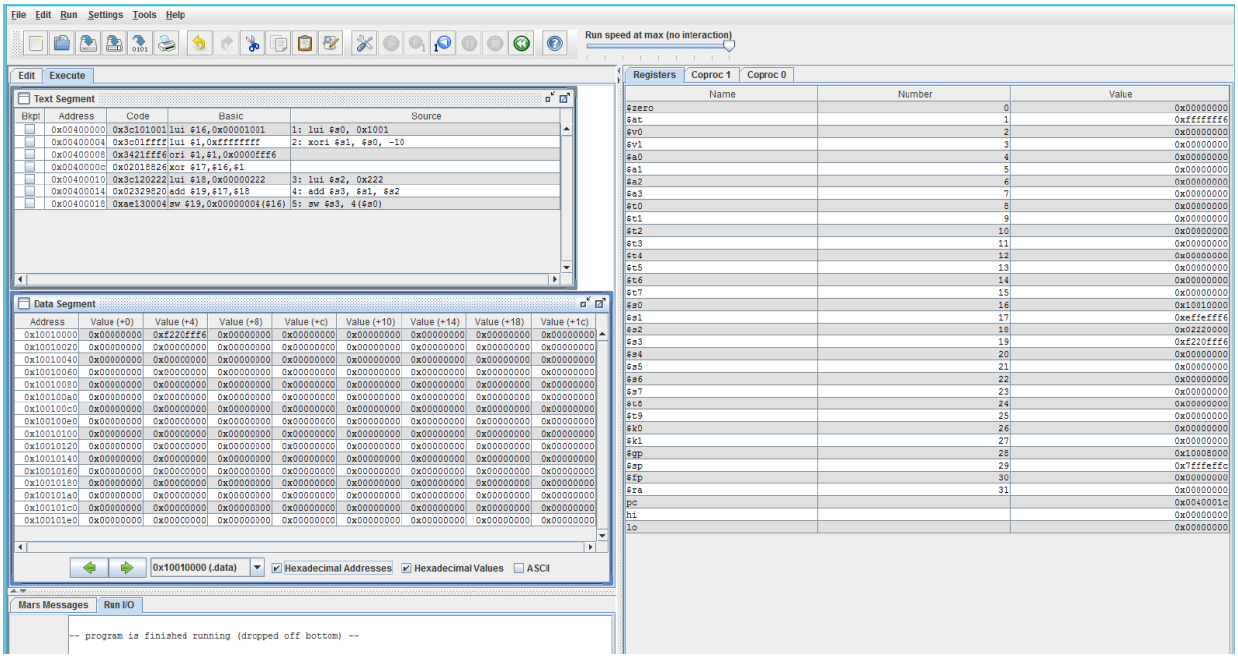
Final addresses:

$s0	0x00010000

$s1 0x1000FFF7

$s2 0x02220000

$s3 0x1222FFF7



1.3) The code doesn't match from my handwork, from what I noticed it had to break up the xori into 2 commands

1.4) after the program was done, $at is equivalent to $s3 which makes me believe that the register $at was kind of used as a temporary when executing through the different instructions.

Question 2)

0x20080000

0010 00|00 000|0 1000| 0000 0000 0000 0000

op rs rt imm

addi $t0,0

0x20090001

0010 00|00 000|0 1001| 0000 0000 0000 0001

op rs rt imm

addi $t1,0x1

0x0089502A

0000 00|00 100|0 1001| 0101 0|000 00|01 1010

op rs rt rd sham func

SLT $t2,$a0,$t1

0X15400003

0001 01|01 010|0 0000| 0000 0000 0000 0011

op rs rt imm

BNE $t2, $0,0x3

0X01094020

0000 00|01 000|0 1001| 0100 0|000 00|10 0000

Op rs rt rd sham func

add $t0, $t0, $t1

0X21290002

0010 00|01 001|0 1001| 0000 0000 0000 0010

Op rs rt imm

addi $t1,$t1,0x2

0X08100002

0000 10|00 0001 0000 0000 0000 0000 00010

op jump target address

j 0x00400008

0X01001020

0000 00|01 000|0 0000| 0001 0|000 00|10 0000

op rs rt rd shamt func

add $v0, $t0,$0

0X03E00008

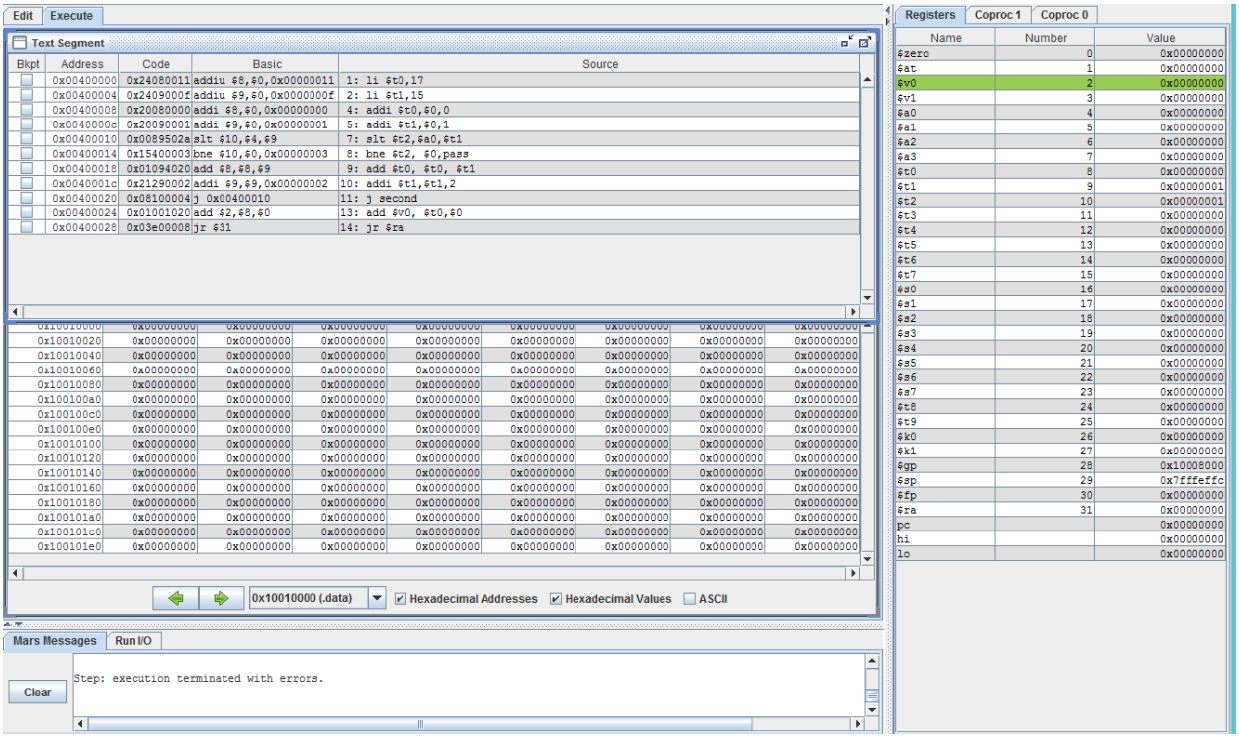
0000 00|11 111|0 0000| 0000 0|000 00|00 1000

op rs r t rd shamt func

jr $ra

2.3)

```
1  #Question 2
2  li $t0,17
3  li $t1,15
4
5  addi $t0,$0,0
6  addi $t1,$0,1
7  second:
8  slt $t2,$a0,$t1
9  bne $t2, $0,pass
10 add $t0, $t0, $t1
11 addi $t1,$t1,2
12 j second
13 pass:
14 add $v0, $t0,$0
15 jr $ra
16
17
18
```



The functionality of this program is to iterate through the values and when register $t2 is not equal to the value in register $0 (0), then it will pass to the adding line. Lastly, it will then jump to the register $ra then the program will terminate.

3a)

```
slt $t0,$s1,$s0
beq $t0,$0, ELSE
add $t1,$s0,$s1
J ENDPROGRAM
ELSE:
Sub $t1,$s0,$s1
ENDPROGRAM:
```

3b)

```
slt $t0,$s1,$s0
beq $s1,$s0, GLABEL
beq $t0,$0, HLABEL
GLABEL:
addi $s0,$s0,1
J ENDPROGRAM
HLABEL:
subi $s1,$s1,1
ENDPROGRAM:
```

3c)

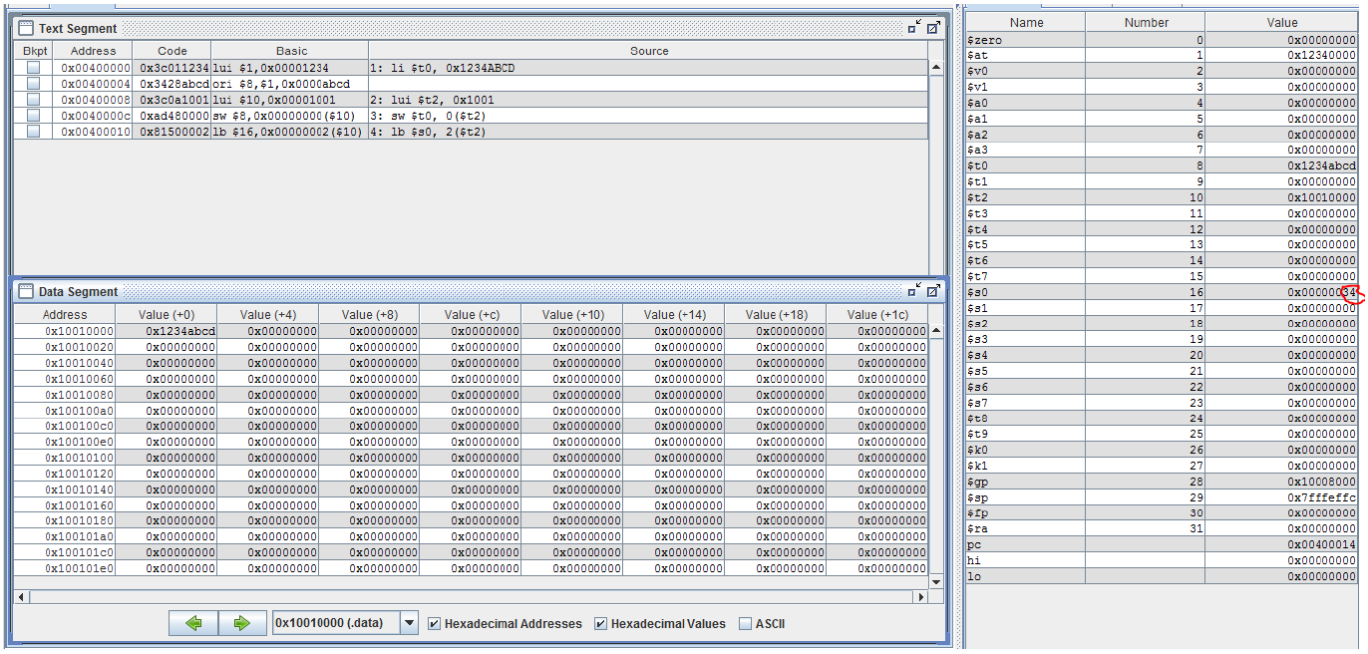
```
slt $t0, $s0,$s1
beq $s0,$s1, GLABEL
beq $t0,$0, HLABEL
GLABEL:
Add $s0, $0, $0
J ENDPROGRAM
HLABEL:
add $s1,$0, $0
ENDPROGRAM:
```

Question 4)

This will produce the output of the second byte from the stored address in $t2. Big-endian would be AB and little-endian would be 34.

4.2)

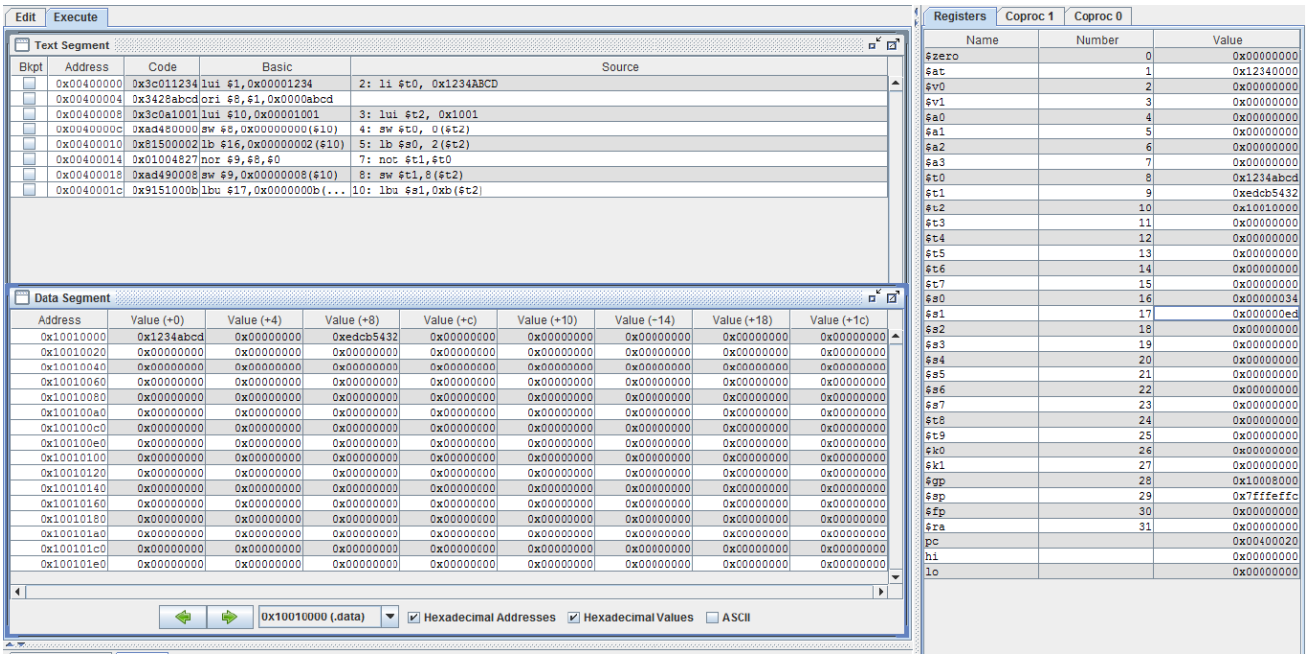
From the MIPS Simulation, it says that the second byte is 34, which would make MIPS a little-endian architecture.



4.3a/b)

mips3.asm

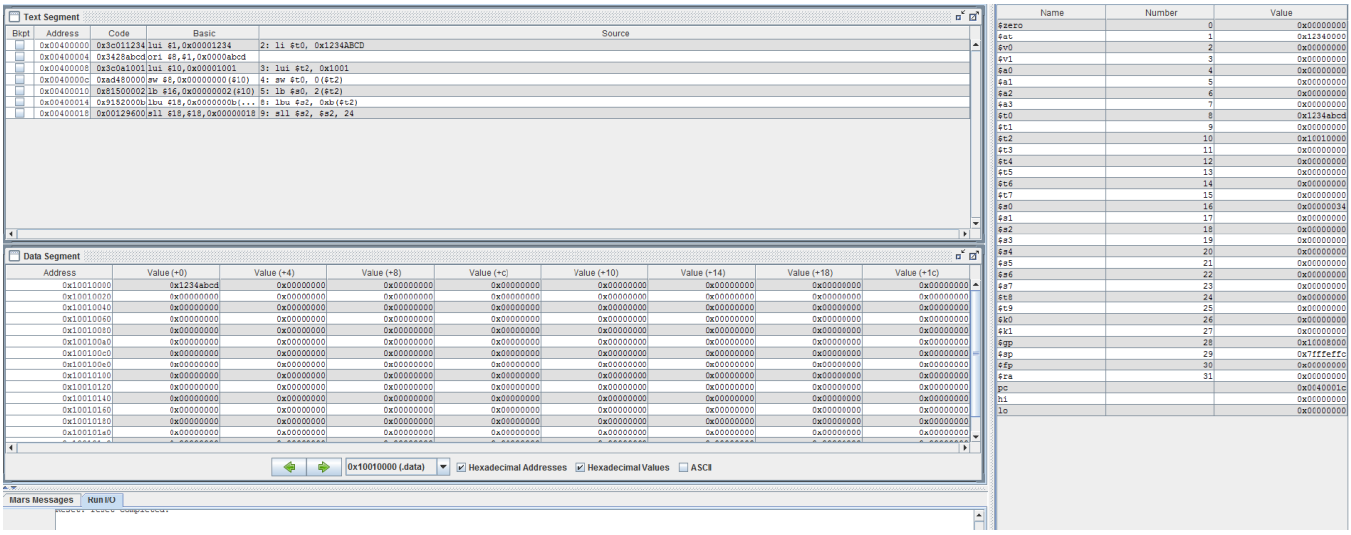
```
1  #Question 4
2  li $t0, 0x1234ABCD
3  lui $t2, 0x1001
4  sw $t0, 0($t2)
5  lb $s0, 2($t2)
6
7  not $t1,$t0
8  sw $t1,8($t2)
9
10 lbu $s1,0xb($t2)
```



4.3c)

```
#Question 4c
li $t0, 0x1234ABCD
lui $t2, 0x1001
sw $t0, 0($t2)
lb $s0, 2($t2)


lbu $s2, 0xb($t2)
sll $s2, $s2, 24
```

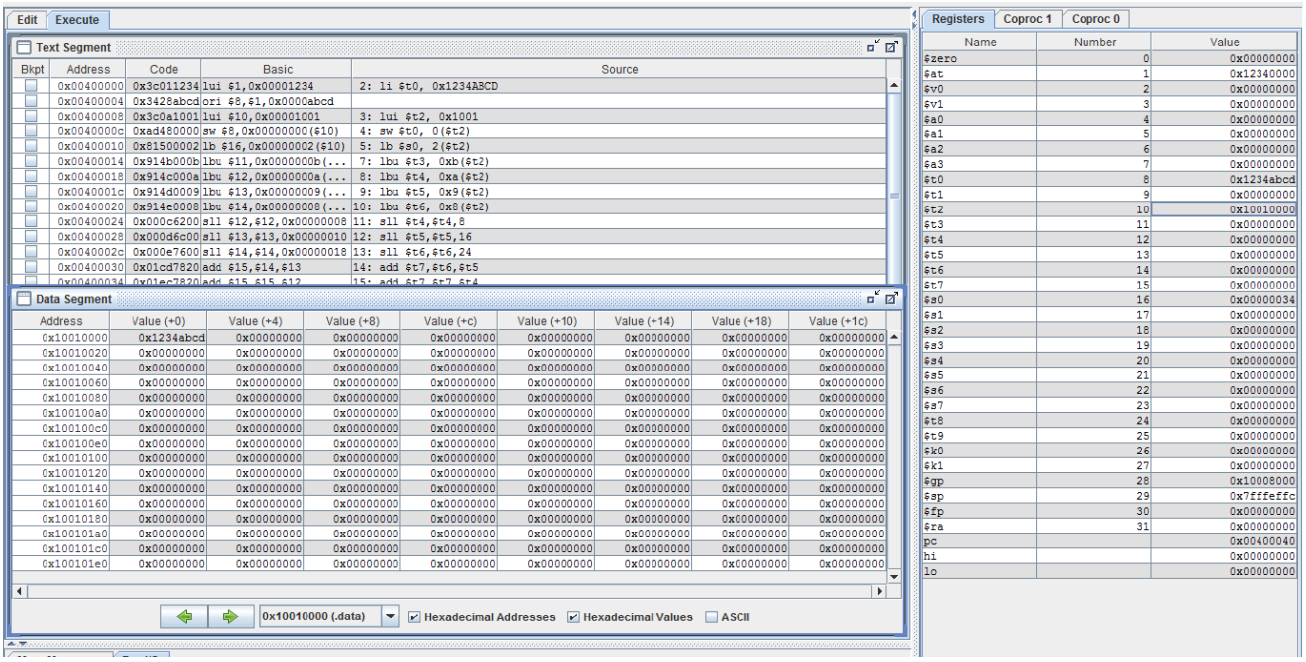


4.3d)

Edit Execute

mips3.asm Prob4d.asm

```
1  #Question 4d
2  li $t0, 0x1234ABCD
3  lui $t2, 0x1001
4  sw $t0, 0($t2)
5  lb $s0, 2($t2)
6
7  lbu $t3, 0xb($t2)
8  lbu $t4, 0xa($t2)
9  lbu $t5, 0x9($t2)
10 lbu $t6, 0x8($t2)
11 sll $t4,$t4,8
12 sll $t5,$t5,16
13 sll $t6,$t6,24
14 add $t7,$t6,$t5
15 add $t7,$t7,$t4
16 add $t7,$t7,$t3
17 sw $t1,20($t2)
18
```



Edit Execute

Text Segment

Bkpt	Address	Code	Basic	Source
	0x00400000	0x3c011234	lui $1,0x00001234	2: li $t0, 0x1234ABCD
	0x00400004	0x3428abcd	ori $8,$1,0x0000abcd	
	0x00400008	0x3c0a1001	lui $10,0x00001001	3: lui $t2, 0x1001
	0x0040000c	0xad480000	sw $8,0x00000000($10)	4: sw $t0, 0($t2)
	0x00400010	0x81500002	lb $16,0x00000002($10)	5: lb $s0, 2($t2)
	0x00400014	0x914b000b	lbu $11,0x0000000b(...	7: lbu $t3, 0xb($t2)
	0x00400018	0x914c000a	lbu $12,0x0000000a(...	8: lbu $t4, 0xa($t2)
	0x0040001c	0x914d0009	lbu $13,0x00000009(...	9: lbu $t5, 0x9($t2)
	0x00400020	0x914e0008	lbu $14,0x00000008(...	10: lbu $t6, 0x8($t2)
	0x00400024	0x000c6200	sll $12,$12,0x00000008	11: sll $t4,$t4,8
	0x00400028	0x000d6c00	sll $13,$13,0x00000010	12: sll $t5,$t5,16
	0x0040002c	0x000e7600	sll $14,$14,0x00000018	13: sll $t6,$t6,24
	0x00400030	0x01cd7820	add $15,$14,$13	14: add $t7,$t6,$t5
	0x00400034	0x01ec7820	add $15,$15,$12	15: add $t7,$t7,$t4

Data Segment

Address	Value (+0)	Value (+4)	Value (+8)	Value (+c)	Value (+10)	Value (+14)	Value (+18)	Value (+1c)
0x10010000	0x1234abcd	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010020	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010040	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010060	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010080	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x100100a0	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x100100c0	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x100100e0	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010100	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010120	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010140	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010160	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010180	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x100101a0	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x100101c0	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x100101e0	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000

0x10010000 (.data) Hexadecimal Addresses Hexadecimal Values ASCII

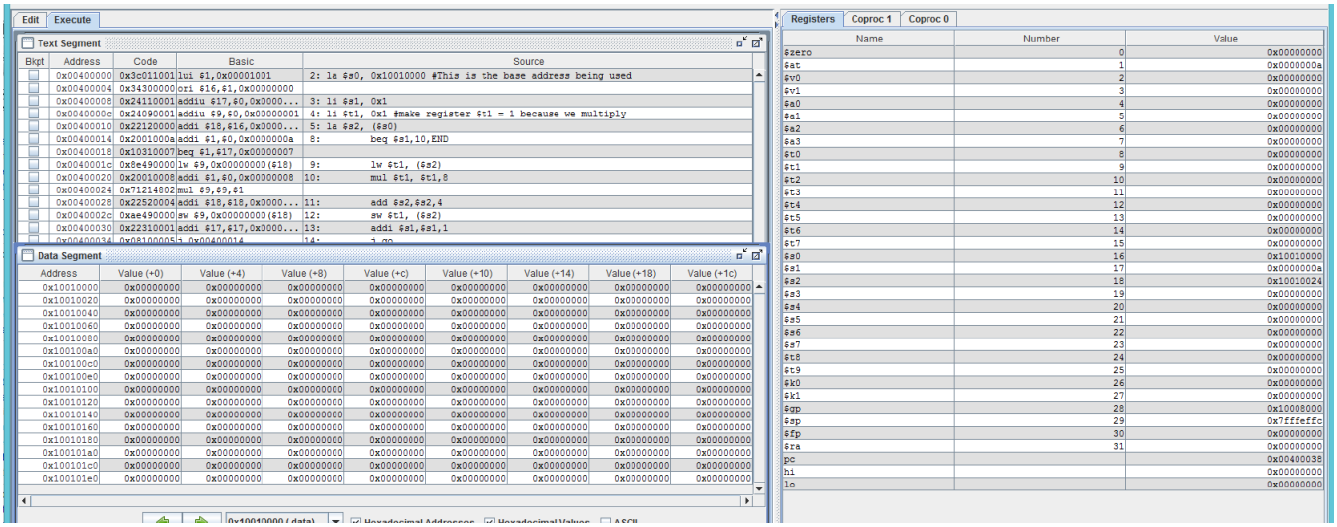
Registers Coproc 1 Coproc 0

Name	Number	Value
$zero	0	0x00000000
$at	1	0x12340000
$v0	2	0x00000000
$v1	3	0x00000000
$a0	4	0x00000000
$a1	5	0x00000000
$a2	6	0x00000000
$a3	7	0x00000000
$t0	8	0x1234abcd
$t1	9	0x00000000
$t2	10	0x10010000
$t3	11	0x00000000
$t4	12	0x00000000
$t5	13	0x00000000
$t6	14	0x00000000
$t7	15	0x00000000
$s0	16	0x00000034
$s1	17	0x00000000
$s2	18	0x00000000
$s3	19	0x00000000
$s4	20	0x00000000
$s5	21	0x00000000
$s6	22	0x00000000
$s7	23	0x00000000
$t8	24	0x00000000
$t9	25	0x00000000
$k0	26	0x00000000
$k1	27	0x00000000
$gp	28	0x10008000
$sp	29	0x7fffeffc
$fp	30	0x00000000
$ra	31	0x00000000
pc		0x00400040
hi		0x00000000
lo		0x00000000

5)

Question5

```
1  #Question 5
2  la $s0, 0x10010000 #This is the base address being used
3  li $s1, 0x1
4  li $t1, 0x1 #make register $t1 = 1 because we multiply
5  la $s2, ($s0)
6  go:
7          beq $s1,10,END
8          lw $t1, ($s2)
9          mul $t1, $t1,8
10         add $s2,$s2,4
11         sw $t1, ($s2)
12         addi $s1,$s1,1
13         j go
14 END:
```



6)

Regwrite: 1

RegDest: 1

ALUSrc: 01

Branch: 0

MemWrite: 0

MemtoReg: 0

ALUControl: 00 (whichever 2-bit binary makes the ALU add)