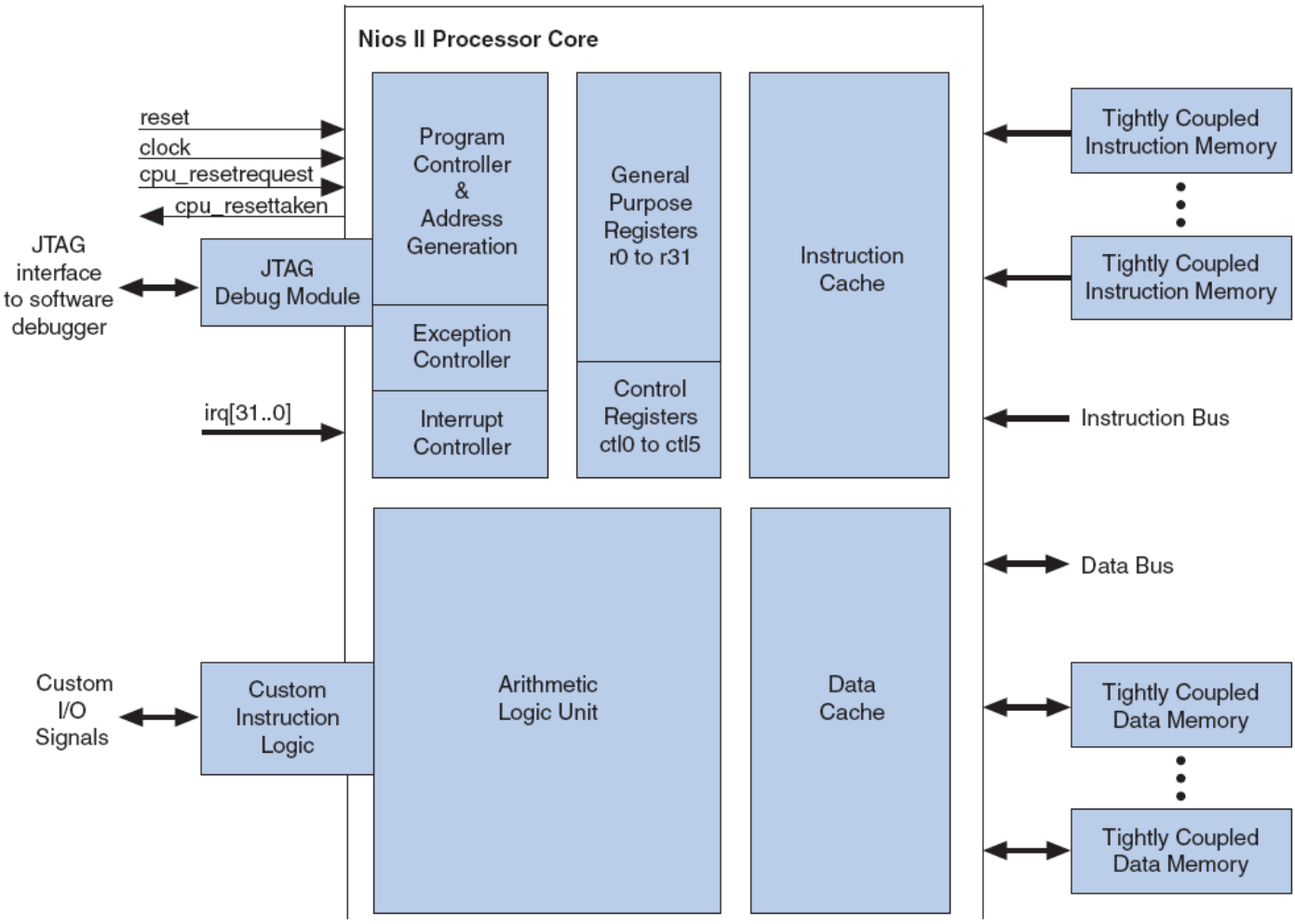
NIOS II Processor Summary
Calvin Engineering Department

Overall Architecture:

The NIOS II processor is a 32-bit soft core RISC (Reduced Instruction Set Computer) processor. Soft core processors are not fabricated as a processor by the manufacturer. Instead, programmable logic devices (PLDs) are used. Software (like Quartus) configures the programmable logic to function as a processor, allowing the designer to configure the CPU and additional components as necessary. The processor also uses a Load/Store approach to computing. The only instructions that access memory simply read (load) data into or write (store) data from the processor's internal registers. The amount of on-chip cache and tightly-coupled memory depends on how the processor is configured in Quartus.



Registers:

The NIOS II processor has 32 32-bit general purpose registers and 6 control registers. The general purpose registers are assigned various roles as shown in the table below. Compilers *must* conform to these conventions; assembly programs *should* conform to these conventions.