

## REVIEW

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## High-efficiency crystalline silicon solar cells: status and perspectives

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With a global market share of about 90%, crystalline silicon is by far the most important photovoltaic technology today. This article reviews the dynamic field of crystalline silicon photovoltaics from a device-engineering perspective. First, it discusses key factors responsible for the success of the classic dopant-diffused silicon homojunction solar cell. Next it analyzes two archetypal high-efficiency device architectures – the interdigitated back-contact silicon cell and the silicon heterojunction cell – both of which have demonstrated power conversion efficiencies greater than 25%. Last, it gives an up-to-date summary of promising recent pathways for further efficiency improvements and cost reduction employing novel carrier-selective passivating contact schemes, as well as tandem multi-junction architectures, in particular those that combine silicon absorbers with organic-inorganic perovskite materials.

### Broader context

Photovoltaic solar energy offers humankind a useful instrument to build a globally prosperous, sustainable, and environmentally friendly society. Its recent success as an economically viable source of electricity is founded on a simple optoelectronic device, the crystalline silicon solar cell. The evolution of this device – relatively slow in the past – has accelerated in recent years, posing now new challenges and opening exciting opportunities. This review is both comprehensive and up to date, describing prior, current and emerging technologies for high-efficiency silicon solar cells. It will help the reader understand how crystalline silicon solar cells work, how they are made, and which factors limit their performance. It then describes several approaches to overcome such limitations, and how these approaches are being transferred from research laboratories to the industry. Specific attention is given to two device designs, the interdigitated back contact cell and the silicon heterojunction cell, pointing out their salient features, critical in enabling very high power conversion efficiencies. Despite its proven maturity, silicon solar cell technology continues receiving an influx of important new ideas that promise simpler fabrication and higher performance. A prime example is its combination with other semiconductor materials to build tandem devices for ultra-high efficiencies.

The year 2014 witnessed the breaking of the historic 25.0% power conversion efficiency record for crystalline silicon solar cells, which was set by the University of New South Wales (UNSW), Australia, in 1999.<sup>1,2</sup> Almost simultaneously, Panasonic, Japan,<sup>3</sup> and SunPower, USA,<sup>4</sup> reported independently certified efficiencies of 25.6% and 25.0%, respectively, both using industrially-sized silicon wafers (see Fig. 1 and Table 1). In parallel, the increased production volumes and associated maturity of the technology have brought the cost of photovoltaic modules down to 0.62 US\$/W<sub>p</sub> (average price in 2014 according to the International Technology Roadmap for Photovoltaics).<sup>5</sup> Solar photovoltaic electricity has already reached grid parity in many countries

and locations. While costs associated with cell processing typically account for less than 20% of the total module cost and only about 10% at the system level,<sup>5</sup> increasing the power conversion efficiency of the solar cell offers a direct pathway to further reducing the levelized cost of electricity (LCOE).<sup>6–8</sup> This review retraces recent advances in silicon solar cell technology towards that goal. The reader may be interested in consulting complementary reviews by Saga<sup>9</sup> and Glunz.<sup>10</sup> A detailed life cycle assessment including a discussion of indicators such as primary energy demand, energy payback time and greenhouse gas emissions can be found in ref. 11.

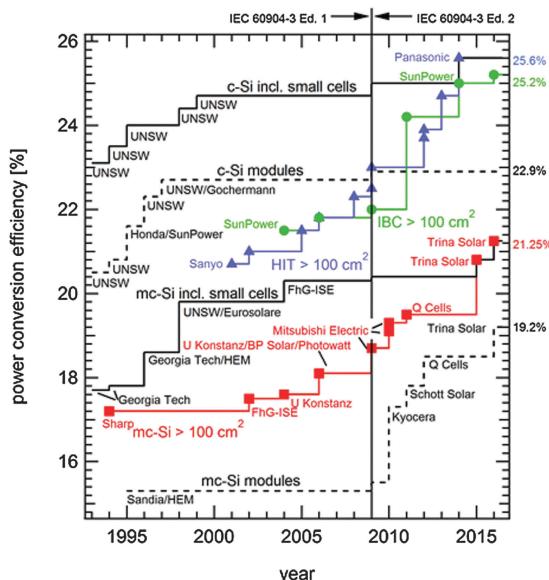
Compared to other photovoltaic technologies, silicon solar cells have the advantage of using a photoactive absorber material that is stable, non-toxic, abundant and well understood. Silicon has an energy band gap of 1.12 eV, corresponding to a light absorption cut-off wavelength of about 1160 nm. This band gap is well matched to the solar spectrum, very close to the optimum value for solar-to-electric energy conversion using a single semiconductor optical absorber. Taking only radiative recombination

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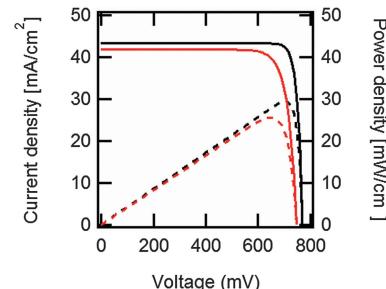




**Fig. 1** Evolution of the energy conversion efficiencies of silicon photovoltaics according to year of entry in tables of ref. 12. Note the steep efficiency improvement of cells with an area larger than  $100\text{ cm}^2$ . The step increase in efficiency in 2009 is due to the redefinition of the standard solar spectrum and affects all technologies.

into account (the so-called detailed balance),<sup>13</sup> the theoretical conversion efficiency limit for a semi-infinitely thick silicon solar cell is 33.5% at 25 °C.<sup>14</sup>

Silicon has an indirect energy band gap, *i.e.* the valence band maximum is not at the same position in momentum space as the conduction band minimum. This has two major consequences. First, it makes radiative recombination fairly inefficient, which implies that, for defect-free material, the photogenerated electrons and holes can exhibit very long lifetimes. In fact, rather than its radiative counterpart, the dominant intrinsic recombination mechanism in silicon is Auger recombination, in which an electron recombines with a hole by transferring their energy difference to a third charge carrier, either a second free electron or hole. This energy is subsequently lost as heat. Consequently, based on an empirical parameterization of experimentally



**Fig. 2** Output current density (continuous black line) and output power density (dashed black line) vs. voltage under one-sun illumination for the ideal, Auger-limited, crystalline silicon solar cell with silicon absorber thickness of 110 μm, open-circuit voltage of 761 mV, short-circuit current density of  $43.3\text{ mA cm}^{-2}$ , fill factor of 89.3%, and power conversion efficiency of 29.4%.<sup>16</sup> In red are the corresponding curves for the current world-record silicon solar cell from Panasonic, with an open-circuit voltage of 740 mV, a short-circuit current density of  $41.8\text{ mA cm}^{-2}$ , a fill factor of 82.7% and a power conversion efficiency of 25.6%.<sup>207</sup> These approximate curves were generated using eqn (7) with ideality factors  $n = 0.675$  for the ideal cell, and  $n = 1$ , plus a series resistance of  $0.61\Omega\text{ cm}^2$ , for the world-record cell.

measured radiative and Auger recombination rates,<sup>15</sup> the limiting intrinsic efficiency for silicon solar cells has been calculated to be 29.4% – significantly lower than the detailed balance limit (for an optimum thickness of 110 μm and considering Lambertian light trapping,<sup>16</sup> Fig. 2 and Table 1).<sup>17</sup> Secondly, because of its indirect band gap, silicon also has a relatively low light absorption coefficient, particularly near its band gap (for a comparison of absorption coefficients of several photovoltaic materials, see, *e.g.*, ref. 18). Despite this, with simple wafer surface texturing, combined with the use of well-designed anti-reflection coatings and rear surface mirrors, efficient light absorption, including the infrared part of the solar spectrum, is possible even with relatively thin wafers ( $\sim 100\text{--}150\text{ }\mu\text{m}$ ).<sup>17</sup> In practice, carrier recombination in silicon can be affected, or even dominated, by the presence of crystallographic defects or foreign impurities. In recent years, thanks to improved silicon ingot growth processes, defect engineering and contamination control during solar cell fabrication, the bulk electronic quality of crystalline silicon wafers has improved to such a point that

**Table 1** Performance parameters of independently certified silicon solar cells discussed in this article. Measurement geometry is specified in the area column: total area (ta) of device including frame, aperture area (ap) defined by a mask that is smaller than the total cell but contains all essential components including finger grid and busbar within the masked area, and designated illuminated area (da) defined by a mask that is smaller than the total area and major cell components lie outside the masked area

Device	Area [cm <sup>2</sup> ]	V <sub>oc</sub> [mV]	J <sub>sc</sub> [mA cm <sup>-2</sup> ]	FF [%]	Eff. [%]	Certification
Ideal, 110 μm		761	43.3	89.3	29.4	Modeled <sup>17</sup>
Panasonic IBC HIT	143.7 (da)	740	41.8	82.7	25.6	AIST (2/14) <sup>3</sup>
SunPower IBC	153.5 (ta)	737	41.3	82.7	25.2	Fraunhofer ISE (10/15) <sup>12</sup>
Kaneka SHJ	151.9 (ap)	738	40.8	83.5	25.1	Fraunhofer ISE (9/15) <sup>370</sup>
Fraunhofer ISE TOPCon	4.0 (da)	718	42.1	83.2	25.1	Fraunhofer ISE (8/15) <sup>290,371</sup>
UNSW PERL (p-type)	4.0 (da)	706	42.7	82.8	25.0	Sandia (3/99) <sup>1,12</sup>
Panasonic HIT	101.8 (ta)	750	39.5	83.2	24.7	AIST (12/12) <sup>218</sup>
EPFL MoO <sub>x</sub> SHJ	3.9 (ap)	725	38.6	80.4	22.5	Fraunhofer ISE (2015) <sup>310</sup>
imec PERT (n-type)	238.9 (ta)	695	40.2	80.5	22.5	Fraunhofer ISE (2015) <sup>160,174</sup>
Trina solar mono-Si PERC (p-type)	243.7	680	40.5	80.3	22.1	Fraunhofer ISE (2015) <sup>12,315</sup>
Trina solar multi-Si PERC (p-type)	242.7 (ap)	667	39.8	80.0	21.3	Fraunhofer ISE (11/15) <sup>12,372</sup>



further device advances now rely on innovative interface passivation and carrier-selective contact structures.

The main purpose of interface passivation is to reduce recombination of photogenerated carriers at the silicon surface.<sup>19–21</sup> This can be done by chemical passivation – usually by hydrogen – of harmful surface defects,<sup>22–25</sup> which are predominantly broken silicon–silicon bonds, called dangling bonds, or by modifying the relative concentration of photogenerated electrons and holes near the surface.<sup>26,27</sup> Effective surface passivation is usually achieved by dielectric materials such as silicon oxide,<sup>26,28–32</sup> silicon nitride,<sup>33–36</sup> silicon carbide<sup>37,38</sup> and aluminum oxide.<sup>19,39–41</sup> Alternatively, a (disordered) semiconductor such as intrinsic hydrogenated amorphous silicon<sup>42,43</sup> can be employed. None of these layers allows carrier extraction *per se*, as they are either insulating or insufficiently conductive.

To enable efficient carrier extraction to the two external metal terminals, two carrier-selective contact structures are needed, which ideally exhibit efficient transport of only one type of carrier (*e.g.*, electrons) while hindering the transport (that is, blocking) of the other type of carrier (*e.g.*, holes). Since recombination requires the participation of both types of carriers, hindering the transport of one of them contributes to reducing recombination in the contact structure. Nevertheless, to suppress recombination more effectively, it is usually necessary to insert in the structure an interfacial passivating layer. Hence a highly selective contact is one that simultaneously presents a high conductivity for just one of the two carriers, while minimizing recombination. In designing high-efficiency solar cells, one may choose either to cover most of the wafer surface with a passivating dielectric material and extract photogenerated carriers selectively through local openings in this insulator,<sup>1</sup> or to deposit carrier-selective materials on the full wafer surface using a suitable interface-passivation strategy. In the latter approach, the two simultaneous requirements of surface passivation and preferential conduction are frequently achieved by using a stack of two or more layers, for example intrinsic and doped hydrogenated amorphous silicon, as in silicon heterojunction solar cell technology.<sup>44–46</sup>

An important criterion for this decision relies on the optical properties of the required materials for contact formation. Indeed, layers blanket-deposited on the wafer surfaces (either for interface passivation or selective transport) should also maximize light coupling into the silicon absorber by minimizing reflection and parasitic absorption losses. Developing contact layers that satisfy these electronic and optical requirements simultaneously represents a considerable challenge. This paper gives a brief overview of recent research to solve it.

## 1. Basic operation and performance indicators of the solar cell

To grasp the full challenge of fabricating simple high-efficiency solar cells, it is useful to briefly reflect on their essential performance parameters. For this, we first consider a solar cell in its most fundamental form, consisting of a semiconductor with a

given energy band gap and electron- and hole-selective contact regions that guarantee charge-carrier separation.

When solar radiation strikes the solar cell, photons with energy greater than the band gap of the semiconductor are absorbed, exciting electrons from the valence band into the conduction band, leaving behind an equally large number of holes in the valence band. Consequently, the total electron and hole concentrations ( $n$  and  $p$ ) under illumination deviate from their thermo-chemical equilibrium values in the dark ( $n_0$  and  $p_0$ , with  $n_0 p_0 = n_i^2$ , where  $n_i$  is  $8.3 \times 10^9 \text{ cm}^{-3}$  at  $25^\circ\text{C}$  for silicon).<sup>47</sup> A net electric current eventually results when those negative (electrons) and positive (holes) charge carriers move in opposite directions in the device. In the quasi-neutral regions of the device, the excess carrier densities ( $\Delta n = n - n_0$ , and  $\Delta p = p - p_0$ ) are approximately equal  $\Delta n \approx \Delta p$ . In analogy to equilibrium, in which the carrier populations are described by a single Fermi energy  $E_F$ , the carrier populations in non-equilibrium conditions can be described by means of the electron and hole quasi-Fermi energies  $E_{Fn}$  and  $E_{Fp}$ <sup>48</sup>

$$n = n_0 + \Delta n = N_C \exp\left(\frac{E_{Fn} - E_C}{k_B T}\right), \quad (1)$$

$$p = p_0 + \Delta p = N_V \exp\left(\frac{E_V - E_{Fp}}{k_B T}\right). \quad (2)$$

$E_C$  and  $E_V$  represent the energetic positions of the conduction band minimum and the valence band maximum.  $N_C$  and  $N_V$  are the effective density of states in the conduction and valence band respectively,  $k_B$  is the Boltzmann constant and  $T$  is the absolute temperature of the semiconductor. The difference between the electron and hole quasi-Fermi energies, which is equal to the sum of the electrochemical potential of an electron  $E_{Fn}$  and the electrochemical potential of a hole  $-E_{Fp}$ , determines the maximum voltage  $V$  that the solar cell can provide<sup>48</sup>

$$V \equiv \frac{E_{Fn} - E_{Fp}}{q} = \frac{k_B T}{q} \ln\left(\frac{np}{n_0 p_0}\right). \quad (3)$$

where  $q$  is the elementary charge.

Under steady-state illumination, photogenerated charge carriers either flow to an external circuit as electric current or they recombine inside the device. In open-circuit conditions, the concentration of carriers builds up, so that the photogeneration rate is perfectly counterbalanced by the recombination rate. As indicated by eqn (3), such high carrier concentration produces the maximum voltage that can be measured in a solar cell, the open-circuit voltage  $V_{oc}$ . For electric current to flow, the solar cell needs to be connected to an external circuit by means of two low-resistance selective contacts – one for the electrons and another for the holes. The current is highest at short circuit (zero voltage), when the concentration of carriers inside the device and, therefore, their recombination rate are relatively low. Note, however, that neither the concentration of carriers nor the difference between the quasi-Fermi energies is zero, even if the terminal voltage is. In a good solar cell, the short-circuit current density  $J_{sc}$  is only slightly lower than the number of photons absorbed in the semiconductor per unit time and area,



multiplied by the elementary charge, which can be called the photogenerated current density  $J_{\text{ph}}$ . The ratio between  $J_{\text{sc}}$  and  $J_{\text{ph}}$  is an indication of the “collection efficiency,” that is, of the ratio of electrons out to photons in. This quantum collection efficiency is usually measured as a function of the wavelength, or energy, of the incident photons. For silicon, with its band gap of 1.12 eV, the highest obtainable  $J_{\text{ph}}$  value for a 110 μm-thick wafer is 43.3 mA cm<sup>-2</sup> under standard test conditions (air mass 1.5 global spectrum, 1000 W m<sup>-2</sup>, 25 °C) (Table 1).

For power generation, the solar cell needs to deliver current and voltage simultaneously, and the total output current density can be written as  $J_{\text{out}} = J_{\text{ph}} + J_{\text{eq}} - J_{\text{rec}}$ , where we have defined the photogenerated current density  $J_{\text{ph}}$  as the net cumulative generation in excess of the equilibrium thermal generation, represented by  $J_{\text{eq}}$ . The recombination current density  $J_{\text{rec}}$  represents all generated carriers that are lost and not collected per unit time and area. Such recombination stems from the higher concentration of electrons and holes required to deliver voltage, compared to short circuit, as shown by eqn (3). Of all loss mechanisms, the most fundamental is radiative band-to-band recombination, which is the inverse process of absorption and is unavoidable. Actually, efficient external luminescence due to radiative recombination is a signature of high-efficiency solar cells,<sup>49,50</sup> as it indicates that very few carriers are lost to recombination *via* defects. Radiative recombination is proportional to the concentrations of the two “reactant species,” that is, to the  $pn$  product of the concentrations of holes and electrons.<sup>48</sup> The constant of proportionality is called the band-to-band recombination coefficient, which for silicon takes a value of  $B = 4.73 \times 10^{-15}$  cm<sup>3</sup> s<sup>-1</sup> at room temperature.<sup>51</sup> Although, as mentioned above, radiative recombination is not dominant in silicon, it is the most fundamental recombination process in any type of photovoltaic absorber and focusing on it helps to elucidate the basic operation principles of solar cells. Using eqn (1) and (2), we can express the total band-to-band recombination current density occurring in a silicon wafer of thickness  $W$  as

$$J_{\text{rec}} = q \cdot W \cdot B \cdot pn = q \cdot W \cdot B \cdot n_i^2 \exp\left(\frac{E_{Fn} - E_{Fp}}{k_B T}\right). \quad (4)$$

In equilibrium, eqn (4) simplifies to

$$J_{\text{eq}} = q \cdot W \cdot B \cdot p_0 n_0 = q \cdot W \cdot B \cdot n_i^2. \quad (5)$$

The output current density of the solar cell can then be written as

$$J_{\text{out}} = J_{\text{ph}} - q \cdot W \cdot B \cdot n_i^2 \left[ \exp\left(\frac{E_{Fn} - E_{Fp}}{k_B T}\right) - 1 \right]. \quad (6)$$

Eqn (6) reflects the relationship between the output current and the sum of the electrochemical potentials of electrons and holes, which is the origin of the output voltage, and, at the same time, is directly related to the  $pn$  product (see eqn (3)) and therefore to recombination. Individually, the gradients of those two electrochemical potentials are the driving forces for the motion of electrons and holes, respectively (see also ref. 48, p. 111). As mentioned above, there is a non-zero difference between the quasi-Fermi energies even in short-circuit conditions,

and this makes  $J_{\text{sc}} \leq J_{\text{ph}}$ . Normally what is measured is the voltage at the cell terminals, which may be smaller than  $(E_{Fn} - E_{Fp})/q$ . Hence, the solar cell characteristic equation is typically written as

$$J_{\text{out}} = J_{\text{sc}} - J_0 \left[ \exp\left(\frac{qV}{nk_B T}\right) - 1 \right], \quad (7)$$

where, in the case of band-to-band recombination, the exponential prefactor  $J_0$  is given by eqn (5), often referred to as dark saturation current density, and the so called “ideality factor” is  $n = 1$ . Physically it represents the generation–recombination current per unit area that takes place in thermal equilibrium, hence the subscript 0. The exponential dependence of the current density on voltage stems directly from the fact that the concentrations of electrons and holes are governed by Fermi–Dirac statistics. This can usually be approximated by Boltzmann statistics, that is, by an exponential dependence on the sum of the electrochemical potentials of an electron and a hole, which eventually translates into a voltage. This explains why so many different types of solar cells display qualitatively very similar – that is, exponential – voltage–current characteristics, independent of the absorber materials and carrier extraction schemes.<sup>52</sup>

Although the above derivation was made for the band-to-band radiative mechanism, other contributing processes to  $J_0$  in silicon are Auger and defect-assisted recombination, which are also proportional to the  $pn$  product. Indeed, real devices are usually dominated by non-radiative recombination. The Auger recombination mechanism is peculiar, because it involves three carriers, even though its end result is to annihilate one free electron and one free hole. Auger recombination is in principle proportional to the  $pn$  product multiplied by the concentration of the majority carriers,  $p$  or  $n$ , but in practice it deviates slightly from an ideal  $p^2n$  (or  $n^2p$ ) dependence due to Coulombic interaction between carriers.<sup>15,53</sup> Defect-assisted, or Shockley–Read–Hall,<sup>54,55</sup> recombination is a two-particle process that can have a complex dependence on the carrier concentrations themselves and on the properties of the defects. Including these additional recombination losses into the solar cell equation requires adapting the  $J_0$  prefactor and the ideality factor  $n$ , which can become either smaller or greater than one.<sup>56</sup> Usually,  $J_0$  and  $n$  are determined experimentally,<sup>57</sup> and their values may reflect a combination of several mechanisms. Low values of  $J_0$ , implying low recombination, and low values of  $n$  are desired for high-efficiency solar cells (see Fig. 2 caption).

Maximum power generation occurs when there is an optimal trade-off between carriers exiting the device, which demands a low concentration of carriers to reduce recombination, and voltage production, which demands a high concentration of carriers. This optimum defines the so-called maximum power point, with associated  $J_{\text{mpp}}$  and  $V_{\text{mpp}}$  values. The fill factor FF is defined by the ratio  $(J_{\text{mpp}} \cdot V_{\text{mpp}})/(J_{\text{sc}} \cdot V_{\text{oc}})$ , and it indicates what fraction of the separate highest current  $J_{\text{sc}}$  and voltage  $V_{\text{oc}}$  can be delivered simultaneously by the solar cell. The maximum value theoretically possible for the fill factor of a silicon solar cell is 89.3%, when considering only intrinsic recombination processes, namely Auger and radiative recombination (Fig. 2).



In practice it can be negatively affected by other internal recombination losses and external shunts. The latter present a path for a leakage current to flow directly between the two terminals of the device. The fill factor is further lowered by resistive losses, due to the flow of current through materials with finite conductivity or cross-sectional area, or across interfaces between different materials (for example, the contact resistance between metals and semiconductors). These effects are usually represented in a simplified manner by lumped series and shunt resistance parameters,  $R_s$  and  $R_{sh}$ , respectively, which can be incorporated into an expanded form of eqn (7). Resistive losses are usually more severe than shunts, and they can be exacerbated by poor cell design.<sup>58</sup> Accurate diagnosis of the  $R_s$  parameter, for which various methods exist,<sup>59</sup> is essential in high-efficiency solar cell development.<sup>60</sup>

The delicate balance between the parameters described above determines the power conversion efficiency,  $\eta = V_{oc}J_{sc}\cdot FF$ , which is typically measured with a solar radiation simulator under standard test conditions for terrestrial applications (air mass 1.5 global spectrum,  $1000\text{ W m}^{-2}$ ,  $25^\circ\text{C}$ ).<sup>61</sup>

## 2. The classic silicon solar cell

### 2.1. Solar cell structure and performance modelling

As will be described in subsequent sections, there are several different ways in which electron- and hole-selective contacts can be implemented on a silicon wafer. Classically, they have been formed by introducing a high concentration of dopants near the two surfaces of the wafer. Fig. 3 shows the schematic structure of such a solar cell, based on a p-type crystalline silicon wafer, a front phosphorus diffusion, and a back aluminum-doped region. For the classic dopant-diffused homojunction silicon solar cell, the choice of p-type material stems from both historical and technological reasons. The first applications of silicon solar cells in the 1950s were to power satellites, where p-type cells featured improved space-radiation hardness, compared to their n-type counterparts.<sup>62,63</sup> Historically, this  $n^+pp^+$  solar cell structure has been referred to as BSF (back surface field), even though

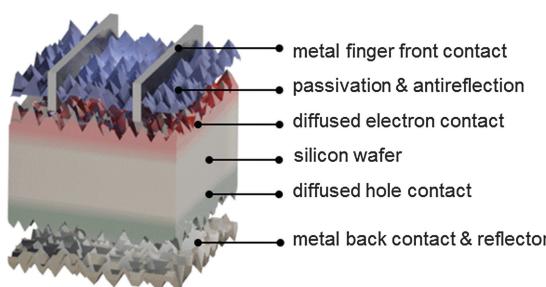


Fig. 3 Schematic of the components of a classic dopant-diffused silicon homojunction solar cell. Electrons and holes generated in the textured p-type silicon wafer are extracted via phosphorus-doped (front, red) and aluminum-doped (back, green) regions. The front surface is passivated with hydrogenated amorphous silicon nitride, which acts simultaneously as antireflection coating. Aluminum is employed as the back contact and serves as a dopant source during firing.

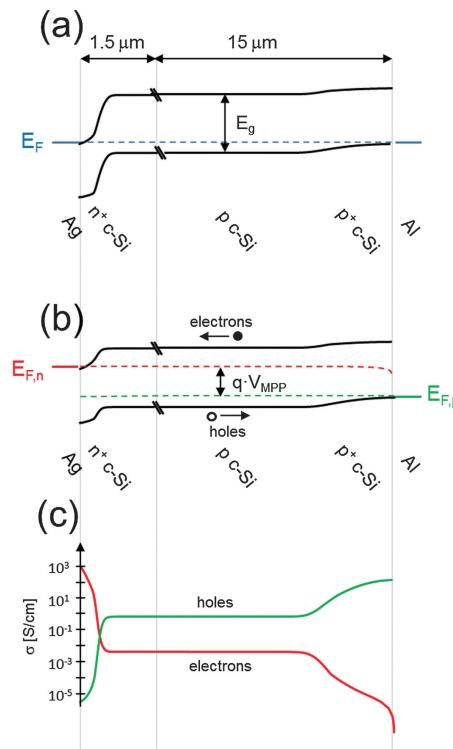


Fig. 4 Energy band diagrams of a classic  $n^+pp^+$  silicon solar cell (a) in equilibrium and (b) at the maximum power point. Representative values were used to model the curves with the program PC1D<sup>66</sup> (p-type wafer doped with  $1 \times 10^{16}\text{ cm}^{-3}$  boron atoms, front  $n^+$  phosphorus diffusion with a surface concentration of  $1 \times 10^{20}\text{ cm}^{-3}$  and depth of  $0.36\text{ }\mu\text{m}$ , and back  $p^+$  aluminum-doped region with a surface concentration of  $1 \times 10^{19}\text{ cm}^{-3}$  and a depth of  $5\text{ }\mu\text{m}$ ). (c) The electron and hole conductivities at the maximum power point, indicating that the  $n^+$  and  $p^+$  regions preferentially transport electrons or holes, respectively.

the equilibrium electric field cannot physically exert a net force on charge carriers.<sup>64,65</sup>

The most widespread industrial fabrication method for wafer-based silicon solar cells will be described below. The solar cell performance parameters that can be obtained in practice deviate from their “ideal” values. It is important to identify the most important limitations of the classic silicon solar cell structure, in order to understand the device designs and technology improvements that have already been, or are in the process of being, adopted by the photovoltaic industry. Fig. 4 and 5 present modelling results of the classic  $n^+pp^+$  structure with the program PC1D,<sup>66</sup> using parameters that are representative of many industrial silicon solar cells: a p-type wafer with a dopant density of  $1 \times 10^{16}\text{ cm}^{-3}$ , thickness of  $150\text{ }\mu\text{m}$ , and minority-carrier lifetime of  $100\text{ }\mu\text{s}$ ;  $n^+$  front phosphorus diffusion with a surface concentration of  $1 \times 10^{20}\text{ cm}^{-3}$ , depth of  $0.36\text{ }\mu\text{m}$ , sheet resistance of  $100\text{ }\Omega\text{ }□^{-1}$ , and front surface recombination velocity of  $10^4\text{ cm s}^{-1}$ ;  $p^+$  aluminum-doped region with a surface concentration of  $1 \times 10^{19}\text{ cm}^{-3}$ , depth of  $5\text{ }\mu\text{m}$ , sheet resistance of  $40\text{ }\Omega\text{ }□^{-1}$ , and rear surface recombination velocity of  $10^7\text{ cm s}^{-1}$ .

Fig. 4a shows the energy band diagram in equilibrium for such a silicon solar cell. The bending of the bands in the



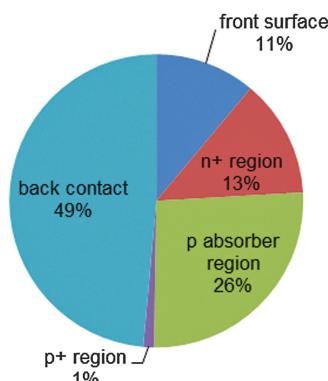


Fig. 5 Analysis of recombination losses of the exemplary  $n^+pp^+$  silicon solar cell described in Fig. 4. At the maximum power point, the main recombination loss occurs at the rear metal/semiconductor interface, while the p-type absorber region contributes 26% and the front  $n^+$  phosphorus diffusion (including its surface) contributes 24%.

vicinity of both diffused regions indicates (i) that the concentrations of electrons and holes vary strongly with position (which can be described as a gradient of their chemical potentials), and (ii) that an electric field (evidenced by the gradient of the bands) is present. These two forces, the gradients of the chemical and electrical potentials, are identical in magnitude and opposite in direction, meaning that there is no net force acting on the carriers and no net movement, as indicated by the constant Fermi energy  $E_F$ . The energy band diagram in Fig. 4b shows that, at the maximum power point, the Fermi energy splits into two quasi-Fermi energies, as a consequence of the excess concentration of carriers generated by the one-sun illumination. Although indistinguishable in the graph, a very small gradient of the quasi-Fermi energies drives electrons to the left and holes to the right. The reason for such directional flow of the two charge carriers can be seen in Fig. 4c, which shows that the electron conductivity is orders of magnitude higher than the hole conductivity on the left (the  $n^+$  region), and the hole conductivity much higher than the electron conductivity on the right (in the  $p^+$  region). The predicted conversion efficiency of this solar cell is 21.1% ( $V_{oc} = 643$  mV,  $J_{sc} = 39.3$  mA cm $^{-2}$ , FF = 83.6%), neglecting any series or shunt resistance effects. A loss analysis at the point of maximum output power ( $V_{mpp} = 565$  mV,  $J_{mpp} = 37.4$  mA cm $^{-2}$ ), is shown in Fig. 5. Although hypothetical, this example is representative of real devices, and it indicates that output power is limited by recombination at the rear metal contact and in the absorber region, with the front phosphorus diffusion, and its surface also causing significant losses.

## 2.2. Typical fabrication process

In the photovoltaic industry today, most solar cells are fabricated from boron-doped p-type crystalline silicon wafers (Fig. 3), with typical sizes of  $125 \times 125$  mm $^2$  for monocrystalline silicon (pseudosquare) and  $156 \times 156$  mm $^2$  for multicrystalline silicon (square), and a resistivity of about  $1\Omega\text{ cm}$ . Monocrystalline silicon wafers are wire-cut from silicon ingots, grown using the Czochralski process, whereas multicrystalline wafers are cut from cast silicon blocks. Wire-cutting traditionally uses slurries,<sup>67</sup>

but in recent years diamond-coated wires have increasingly been used for this purpose, enabling cutting speeds six to eight times faster, and are expected to become the dominant wafering technology.<sup>68,69</sup> The thickness of the cut wafers is typically 180  $\mu\text{m}$ , with a trend towards thinner wafers during the last 15 years.<sup>5,70-73</sup> The kerf loss is typically on the order of 100  $\mu\text{m}$ , representing an important cost factor.

Silicon solar cell manufacturing typically starts with chemical etching and surface texturing of the wafers.<sup>74</sup> Usually, texturing is achieved by immersion of the wafers in a wet chemical bath, yielding identically textured surfaces at the front and back surfaces. The same step also removes several  $\mu\text{m}$  of damaged material resulting from the wire sawing. Potassium hydroxide (KOH) etching of (100)-oriented monocrystalline silicon wafers is anisotropic and results in randomly sized square pyramids with (111) faces,<sup>75</sup> which reflect and refract the incident light at oblique angles, resulting in excellent antireflection and light-trapping properties.<sup>76</sup> Texturing of multicrystalline silicon, which has grains of many different orientations, requires isotropic wet etching, usually based on acidic solutions.<sup>77-80</sup> The reflectance of multicrystalline wafers after acidic texturing is higher than that of monocrystalline silicon after alkaline texturing. However, after deposition of an antireflection coating and encapsulation under glass in the module, the total photo-generation in a multicrystalline cell can reach 99% of that in a monocrystalline cell.<sup>81</sup> For multicrystalline wafers, various types of submicron texture have been proposed to further improve reflectance.<sup>82,83</sup> Very good results have also been reported using plasma texturing.<sup>31</sup>

After surface texturing (particularly after alkaline etching), the wafers need to be cleaned. Several strategies that usually include at least two steps are possible. First, a chemically oxidizing agent, e.g., an acidic peroxide solution, forms an oxide that “encapsulates” potentially harmful impurities present on the surface. Following rinsing in de-ionized water, the oxide is stripped off in a reducing chemical, usually hydrofluoric acid, which yields relatively inert (111) surfaces with hydrogen termination.<sup>84</sup> The wafers are now ready for dopant diffusion, usually phosphorus, for the typical p-type silicon wafer, or boron, if an n-type wafer is used.

Diffusion is usually performed in high-temperature quartz furnaces by exposing the wafers to a gaseous environment containing the phosphorus atoms, typically nitrogen saturated with phosphorus oxychloride (POCl<sub>3</sub>). A small amount of oxygen is also introduced in the furnace so that a phosphorus–silica glass is grown on the wafer surfaces. It is from this glass that the actual diffusion of the dopant atoms into the silicon wafer takes place. Typical diffusion temperatures range from 760 to 850 °C for phosphorus, and slightly higher for boron. As the doping process is not selective, a diffused region is also formed on the rear and at the edges of the wafer and needs to be subsequently etched off. Typically, the sheet resistance of the resulting  $n^+$ -type layer is in the 50–100  $\Omega\text{ cm}^{-2}$  range. Following diffusion, the phosphorus–silica glass is etched in hydrofluoric acid; at this point it is possible to also etch a very small amount of silicon to fine-tune the sheet resistance.



The primary purpose of forming a diffused region is charge separation. The n<sup>+</sup>-type layer at the front surface functions as an electron-selective contact, or electron transport region, by making the concentration of electrons much higher than that of holes, that is, by creating a large asymmetry between the conductivities for electrons and holes (see Fig. 4c). It would seem desirable that the concentration of phosphorus be as high as possible (the maximum electrically active concentration in silicon is about  $3 \times 10^{20} \text{ cm}^{-3}$ ). However, such a high carrier concentration triggers detrimental electronic effects,<sup>85–87</sup> including band gap narrowing and three-particle Auger recombination, which draws holes into the n<sup>+</sup> region and thus reduces the selectivity of the contact, that is, its ability to “block” holes. Excess phosphorus can form precipitates, which may cause additional recombination. Auger, and possibly Shockley–Read–Hall, recombination not only limits the achievable voltage, but also reduces the blue response of the solar cell.<sup>86</sup> A second function of the n<sup>+</sup> layer is to connect the wafer absorber region to a metal electrode. To achieve a sufficiently low contact resistance between the metal and the semiconductor, a high concentration of phosphorus (typically in the  $1 \times 10^{20} \text{ cm}^{-3}$  range) is required to promote quantum-mechanical tunneling across a thin potential barrier that arises as a consequence of the different work functions (electrochemical potentials) of the two materials.<sup>88</sup> The prevalent approach in industry is to implement a phosphorus diffusion with a high surface concentration to achieve a low contact resistivity,<sup>89</sup> while being very shallow to reduce absorption of ultraviolet and blue light and thus maintain a reasonable blue response; typically, the junction depth is between 0.2 and 0.3 μm below the surface. Such diffusion is susceptible to surface recombination losses, and a passivating insulator is usually deposited to suppress such losses.<sup>34</sup> Since the metal contact is restricted to about 5% of the front surface, the diffused region must also provide lateral transport of the collected electrons towards the metal fingers that form the front electrode. The trade-off between the competing factors of carrier separation, bulk and surface recombination and lateral current transport makes the optimization of the front dopant diffusion quite complex, as discussed below in greater detail.

Phosphorus diffusion offers the additional advantage of impurity gettering. Briefly, gettering is the process where transition metals like iron, nickel, chromium, etc.<sup>90–92</sup> diffuse from the bulk of the wafer towards the phosphorus diffusion.<sup>93,94</sup> Once they are in the highly doped n<sup>+</sup> surface region, these impurities are no longer harmful to device operation.<sup>95</sup> This means that relatively impure, and thus cheaper, wafers can be used, making the complete cell process more cost effective. Phosphorus gettering has undoubtedly enabled the development of multicrystalline silicon solar cells.

Wafers are subsequently covered by an antireflection coating with a high transparency across the visible and infrared regions of the spectrum.<sup>96,97</sup> The refractive index of the coating should be the geometric mean of the refractive indices  $n$  of glass ( $n \approx 1.5$ ) and silicon ( $n \approx 4$  in the visible), while its optical thickness dictates the wavelength at which minimum reflection occurs, which for terrestrial application is preferentially set

around 600 nm.<sup>98,99</sup> Hydrogenated amorphous silicon nitride (thickness  $\approx 75$  nm,  $n \approx 2$  in the visible), often just called silicon nitride, deposited by plasma-enhanced chemical vapor deposition at intermediate temperatures (about 400 °C) has been very successful for this purpose.<sup>100</sup> Like the phosphorus diffusion, this layer has multiple functions. In addition to its antireflective properties, silicon nitride provides very efficient passivation of the phosphorus-doped surface.<sup>34</sup> Combined with a moderately doped n<sup>+</sup> diffusion (sheet resistance of about  $100 \Omega \square^{-1}$ ), it can result in low recombination current densities of  $100 \text{ FA cm}^{-2}$  or less.<sup>19</sup> Such excellent passivation is due mainly to hydrogen termination of silicon dangling bonds at the surface.<sup>35</sup> In addition, silicon nitride layers contain a high positive fixed charge density ( $\sim 10^{12}$  elementary charges per  $\text{cm}^2$ ),<sup>101,102</sup> which further increases the concentration of electrons and decreases that of holes at the surface, resulting in a reduced statistical probability of recombination, according to the Shockley–Read–Hall model. Hydrogenated silicon nitride has an added beneficial effect for multicrystalline silicon wafers, as the hydrogen contained in these films is released into the silicon wafer during the so-called contact firing step at the end of the cell process.<sup>77,103</sup> The beneficial effect of hydrogenation on defective silicon was already established in 1980.<sup>104</sup> Firing of the front metal contact through the silicon nitride layers has proven to passivate defects in multicrystalline silicon wafers very effectively, and it complements the prior POCl<sub>3</sub> gettering step.<sup>105,106</sup> In the modelling presented in Fig. 5 a minority-carrier lifetime of 100 μs was assumed, but much longer carrier lifetimes have been achieved, thanks to the combined effects of gettering, hydrogenation, and improved ingot growth technologies.

The front side is finalized by screen printing over the antireflection coating an array of silver finger gridlines (width 50–100 μm) usually connected by several busbars and, on top of the busbars, copper-tin stripes (width 1–2 mm). The screen printing paste contains a binder material (glass frit) that dissolves the metal powder, reacts with the silicon nitride and wets the silicon surface during high-temperature firing. During cooling, silver particles precipitate and adhere to the surface of the silicon wafer.<sup>107–110</sup> It is critical to minimize shading, by reducing the width of the grid lines, in order to maximize the short-circuit current, but there is a trade-off between shading and resistive losses that needs to be optimized. Minimization of the metal/semiconductor contact fraction is critical to achieve a high voltage (see Fig. 5), but the contact fraction needs to be balanced against an increased contact resistance loss.

During the same firing-through step, the back contact is also formed. Usually a screen-printed aluminum paste is applied over the full back surface of the wafer.<sup>107,111–113</sup> During firing, the aluminum forms a eutectic melt with silicon, consuming a similar amount (about 5–20 μm) of silicon. This fully melts and compensates (over-dopes with aluminum) the parasitic n-type region formed at the rear during phosphorus diffusion. During cooldown, a heavily aluminum-doped p-type epitaxial silicon layer forms near the rear surface of the wafer. In addition, this p-type region acts as a hole-selective contact to the p-type silicon absorber. Similar to what was observed above about the



$n^+$  region, it would be desirable to implement a very high concentration of aluminum dopant atoms (hence of holes), but the solubility of aluminum in silicon is limited to about  $1 \times 10^{19} \text{ cm}^{-3}$ . The selectivity of this contact region in terms of blocking electrons is limited by heavy-doping effects such as band gap narrowing<sup>114,115</sup> and Auger recombination,<sup>116</sup> whereas impurity and carrier-carrier scattering, which limit the minority-carrier mobility, are beneficial in this instance. The eutectic mix that remains on the wafer makes it impossible to apply dielectric coatings to passivate the wafer surface, unless it is etched off. This can lead to high recombination losses, as shown in Fig. 5. To keep minority electrons from reaching the rear metal/silicon interface, a thick  $p^+$  layer is used, so that the total conductance (conductivity divided by distance) for the electrons is low. Optimized aluminum-doped regions can reach a recombination current parameter  $J_0$  of about  $500 \text{ fA cm}^{-2}$ ,<sup>117</sup> but a value of  $1000 \text{ fA cm}^{-2}$  is more typical. The latter can be expressed in terms of an effective surface recombination velocity of about  $1000 \text{ cm s}^{-1}$  (note that, for a given aluminum-doped region, the surface recombination velocity scales inversely with the dopant density of the wafer, in low injection). The aluminum also acts as a back reflector, albeit a poor one<sup>118,119</sup> (that is made even worse by the alloying process), reflecting back into the silicon absorber a fraction of the infrared light that has not been fully absorbed during the previous passage through the silicon wafer.<sup>120</sup> Silver-paste strips are usually printed on the rear to enable soldering to the copper interconnects, which “string” the front grid of one cell to the back contact of the neighboring cell in a module. Finally, the parasitic phosphorus diffusion present at the edges is removed by laser scribing around the perimeter of the wafer.

Next, each solar cell is individually measured and sorted according to efficiency and current. The latter is of extreme importance, as cells are connected in series to form strings, which requires that each individual cell contribute an identical current. The module is finished by encapsulating the solar cell strings between a front glass plate and a polyethylene terephthalate (PET) or tedlar/PET/polyamide (TPA) back sheet by means of a lamination process that includes melting of an ethylene vinyl acetate (EVA) sheet.

Industrial silicon solar cells fabricated with the process scheme described here, or variations of it, typically deliver efficiencies of up to 19.5% for monocrystalline and up to 17.8% for multicrystalline substrates.<sup>121</sup> Advances in module technologies, including the use of antireflection coatings on the outer glass, result in cell-to-module power ratios close to 100%.<sup>5</sup> Nevertheless, the frame, interconnection and other losses cause module efficiencies to be typically 1.5–2% lower than the cell efficiencies.

The great simplicity and robustness of multicrystalline silicon technology explains its current dominance in the photovoltaics market, with a share of about 56%.<sup>122</sup> However, over the past years, the price of silicon has dropped significantly, while its electronic quality has improved.<sup>6</sup> As a consequence, monocrystalline silicon has become increasingly attractive for solar cell fabrication, with a current market share of about 35%. To fully exploit the benefits of such higher quality material, more sophisticated device designs and fabrication processes are needed. To guarantee overall lower \$/Watt values, compared to multicrystalline technology,

such processes should remain cost effective and deliver high efficiency. Several factors explain the drive towards higher efficiency silicon solar cells. High-efficiency solar modules require less mounting hardware and space and result in a lower balance-of-system cost. Such modules also yield higher energy densities, which may be important for applications where space is at a premium. Higher efficiency solar cells also usually perform better at higher ambient temperatures and reduced illumination levels, compared to their lower efficiency counterparts. To further increase the energy yield, high-efficiency modules can be combined with solar tracking systems.<sup>123</sup>

While today's state-of-the-art R&D silicon solar cells can deliver efficiencies above 25%, the performance of industrial cells remains constrained by economic factors. Many of the features enabling high efficiency cause a significant rise in processing or equipment costs. However, identifying and understanding the limitations of the traditional process scheme enables the development of innovative concepts that might lead to higher efficiencies at lower cost. In the following we first discuss briefly how the standard dopant diffusion technology can be “upgraded” towards higher efficiencies. Next, we discuss two archetypal high-efficiency cell architectures, namely interdigitated-back-contact and silicon heterojunction solar cells. Finally, we discuss recent trends combining high voltage and current, as well as simple processing, by using alternative self-passivating and dopant-free contacting schemes.

### 3. Increasing the efficiency of silicon solar cells

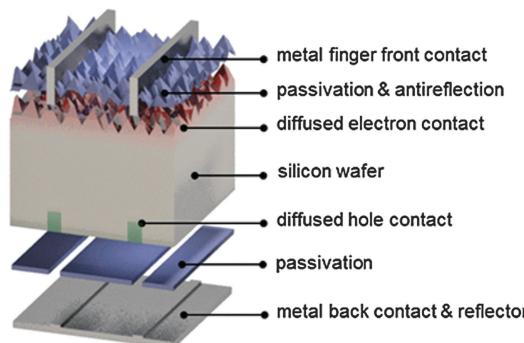
#### 3.1. Selective front diffusions

A good strategy to improve the performance of industrial silicon solar cells is to address step-by-step the individual limitations of the classic technology. A first modification is the decoupling of the requirements of the front diffused region in terms of carrier collection and, on the other hand, high voltage and good contact. As described in Section 2.2., this region is usually very thin, moderately doped and surface passivated, to ensure a high quantum collection efficiency. On the other hand, a high dopant concentration is usually needed to guarantee good contact formation by screen printing. In addition, a deep and highly doped diffusion is desirable to reduce recombination in the fraction of the front surface contacted by the metal grid. Selective diffusion (also called selective-emitter) technology resolves this trade-off by featuring a lowly doped region between the metal fingers, while creating a high doping level just below the fingers. Several approaches have been proposed for the fabrication of such structures, including selective diffusion, ion implantation and laser doping processes.<sup>124–129</sup>

#### 3.2. Localized back contacts and dielectric back surface passivation

As mentioned above, aluminum-doped regions help to control recombination near the rear metal/semiconductor surface, but they are not ideal from the recombination or optical point of view.





**Fig. 6** Schematic of the components of a localized rear contact solar cell with dielectric rear surface passivation. Aluminum doping from the back contact into the silicon wafer (green) is confined to the small openings in the rear passivation layer, minimizing recombination. The dielectric passivation layer simultaneously improves the reflectivity of the aluminum back reflector.

The level of recombination current they can achieve is about  $1000 \text{ fA cm}^{-2}$ , that is, 10 to 50 times larger than a front phosphorus-doped region coated with a passivating dielectric. Hence, they represent a limiting factor to silicon solar cell efficiency.

Restricting the aluminum alloyed  $p^+$  region to a small fraction (about 1–5%) of the rear surface while passivating the rest with an insulating material has significant electronic and optical benefits. In this approach, which is commonly referred to with the acronyms PERC (Passivated Emitter and Rear Cell), PERL (Passivated Emitter, Rear Locally-doped) or PERT (Passivated Emitter, Rear Totally diffused),<sup>1,130</sup> local contact openings (in industry typically as lines) are made in the insulator using, for example, laser ablation (Fig. 6). Subsequently, an aluminum paste is screen printed over the full rear surface and fired, so that local  $p^+$  regions are formed within the openings in the dielectric. This approach is similar to so-called laser-fired contacts, where local openings are made after the final rear metallization.<sup>32,131</sup> In either case, the result is the formation of an almost ideal back surface mirror, since internal reflection inside the silicon device significantly benefits from the presence of a low refractive index material between the metal and the silicon wafer.<sup>132,133</sup> Free-carrier absorption in the classic, uniform  $p^+$  aluminum-doped region is also avoided.

But the greatest benefit from the localized contact approach comes from the superior control of surface recombination achievable with insulating films. Arguably the best known among such films is created by high-temperature oxidation of silicon surfaces to form silicon oxide,<sup>28</sup> which can yield very low interface state densities,<sup>133</sup> combined with a level of charge-assisted passivation.<sup>26</sup> Although resulting in low surface recombination velocities, high-temperature thermal oxidation can deteriorate the bulk carrier lifetime due to dissolution of impurity clusters in the multicrystalline material.<sup>134</sup> Even if intelligent process sequencing to maximize phosphorus gettering can be used to circumvent the problem, a second high-temperature step can add cost and complexity to solar cell fabrication. Because of that, deposited films are generally preferred in

industry to achieve passivation of the rear surface. Hydrogenated amorphous silicon nitride, commonly used at the  $n^+$  front, is unsuitable for rear surface passivation in actual solar cells: even though good surface passivation can be obtained on p-type surfaces,<sup>135</sup> the presence of such a layer at the rear in solar cells causes undesired shunting at the local rear contacts.<sup>136</sup>

The search for a suitable dielectric to passivate p-type silicon surfaces has been increasingly intensive since the early 2000s.<sup>37,137–141</sup> A breakthrough came with the advent of aluminum oxide, which is a negative fixed-charge dielectric,<sup>39,40</sup> essentially avoiding the shunting path caused by silicon nitride in locally contacted solar cells. Such films show a very high negative fixed-charge density (around  $10^{13} \text{ cm}^{-2}$ ),<sup>27</sup> strongly attracting holes to the surface and thus creating a  $p^+$  accumulation layer, which helps to suppress electron recombination at the rear surface. Aluminum oxide layers can be deposited with a variety of techniques, including atomic layer deposition,<sup>39,40</sup> plasma-enhanced chemical vapor deposition,<sup>142,143</sup> atmospheric pressure chemical vapor deposition,<sup>144</sup> and sputtering.<sup>145</sup> As most of the charges are located very close to the silicon surface, these layers can be kept very thin (a few nanometers), although they are usually capped with a thicker silicon nitride<sup>146</sup> or silicon oxide<sup>147</sup> layer to improve internal optical reflection in the device. In case no blanket metallization is applied, the developed cells can be used for bifacial applications.<sup>70,148</sup> Importantly such stacks can be engineered to withstand contact firing.<sup>149–153</sup> To fully exploit the benefit of dielectric-layer integration at the rear of solar cells, it may be desirable to polish the rear side of the silicon wafer.<sup>101,154–156</sup> As aluminum oxide is an excellent passivation layer for p-type surfaces, very successful results have also been reported integrating this dielectric at the front, boron-diffused region of n-type solar cells.<sup>157</sup>

The idea of restricting the contacts to lines or points, while passivating most of the surface with an insulator was applied in 1989 to the rear undiffused side of p-type silicon solar cells in ref. 19 (line contacts, silicon nitride passivation) and in ref. 158 (point contacts, silicon oxide passivation) for small laboratory devices. By adapting and scaling up such concepts, the photovoltaic industry is currently developing similar cell designs.<sup>153</sup> A record industrial partial rear contact (PERC/PERL) solar cell on p-type silicon wafers was recently announced by Trina Solar, China, reaching an independently certified efficiency of 22.13% (see Table 1).<sup>12,315</sup>

### 3.3. Metallization

The screen-printed silver pastes typically employed by industry need to be subjected to a contact firing step. Besides ensuring a low contact resistance between the metal and the diffused n-type region underneath, the conductivity of the printed lines improves during firing, but remains, nevertheless, higher than that of pure metal lines. This can be resolved with metal plating.<sup>159–161</sup> Thanks to the improved line conductivity and the different patterning technique, narrower and taller lines can be fabricated, reducing shading losses. Copper is often the metal of choice, offering attractive cost advantages. Another advantage of this approach is that it circumvents the firing-stability



constraint for dielectric passivation layers. High-performance firing-free devices have been reported that exploit firing-incompatible passivation approaches, such as the use of hydrogenated amorphous silicon as rear surface passivating film,<sup>139</sup> and hybrid devices featuring a homojunction front contact and a heterojunction rear contact.<sup>162,163</sup> Despite these developments, an important breakthrough with direct industrial impact will be the development of a full-area hole-selective passivating rear contact that can withstand the contact firing process.

### 3.4. Wafer crystallinity and conductivity type

In recent years, significant progress has been made in the casting of multicrystalline silicon ingots. Relatively small grain sizes can better accommodate the stress associated with crystallization, thus reducing the density of dislocations inside the grains. This is of great importance, as dislocations are strong recombination sites.<sup>164</sup> Moreover, dislocation-rich regions are relatively unresponsive to gettering and hydrogenation treatments.<sup>165</sup> The use of this material, called high-performance multicrystalline silicon, is becoming pervasive and is partly responsible for the improved performance now achieved with multicrystalline silicon solar cells.<sup>166</sup> Monocrystalline silicon is capable of even higher performance, and further gains may be obtained by changing its conductivity type. As has already been pointed out, p-type wafers have historically dominated over n-type wafers.<sup>62</sup> This choice could also be argued to be beneficial from a performance perspective, as the mobility of the minority carrier in the absorber wafer region (*i.e.*, electrons) is about a factor of three higher than that of holes in n-type wafers. This yields much longer diffusion lengths for wafers with identical carrier lifetimes. However, the comparison between p-type and n-type silicon is frequently done at constant resistivity. If the comparison is instead made at equal dopant concentration (which is more meaningful in terms of achievable device voltage), then the Auger limit to the lifetime is higher for p-type crystalline silicon than for n-type crystalline silicon.<sup>17</sup> In practice, for wafers with comparable dopant and defect concentrations, the carrier lifetime of n-type silicon is usually much higher than that of p-type silicon.<sup>167</sup> One reason for this is that typical carrier lifetime killers in silicon are transition metals,<sup>168,169</sup> which generally have much larger carrier capture cross sections for electrons than for holes.<sup>170</sup> A second reason is that a significant oxygen concentration is usually present in Czochralski-grown silicon, which is known to lead to the formation of a boron–oxygen complex under light exposure or excess carrier injection,<sup>171,172</sup> with a subsequent degradation of the minority-carrier lifetime.<sup>173</sup> In comparison, the minority-carrier lifetime of n-type silicon is not affected by the presence of oxygen, and the Czochralski method can be used to grow high-quality ingots.

Despite these factors, p-type silicon remains the material of choice for the photovoltaic industry. An important reason for this is to be found in the solidification of silicon from its molten state. Boron has a segregation coefficient close to 1, which results in a small variation of its concentration along the silicon ingot and a relatively tight distribution of wafer resistivity. In contrast, phosphorus has a low segregation coefficient that results in a strong variation of wafer resistivity along the ingot

(approximately a factor of 10). Although not insurmountable, it is an obstacle for industrial processes and device designs with tight wafer resistivity specifications.

Yet another reason for the predominance of p-type silicon is the relative simplicity and proven expertise of implementing the thermal diffusion of phosphorus to form the p–n junction on a p-type wafer, compared to the relative novelty and higher temperature of boron diffusion. The traditional  $n^+pp^+$  firing-through process sequence described in Section 2.2. cannot easily be transferred to n-type wafers. The  $p^+nn^+$  device structure corresponding to the latter requires both boron and phosphorus diffusions, since an n-type dopant element (donor) that may be alloyed to silicon does not exist. This issue was recently circumvented in a 22.5% device featuring an  $n^+np^+$  structure, where the  $p^+$  region was located at the rear, and where contact firing was replaced by low-temperature copper-plated metallization.<sup>160,174</sup>

Despite this, the principal advantage of n-type silicon over p-type in terms of resilience to metal contaminants is largely wiped out by the gettering action of the phosphorus diffusion and the aluminum alloying. In this context, the possibility to make high-efficiency diffused-junction solar cells from p-type silicon wafers was recently further underlined by Trina Solar, China, announcing efficiencies of 22.13 and 21.25%, using p-type monocrystalline and multicrystalline wafers, respectively (Table 1). There remains the light-induced degradation caused by boron–oxygen complexes, but a cure for the defect seems to have been found,<sup>175</sup> possibly linked to the introduction of hydrogen into the wafer.<sup>176</sup> The use of alternative p-dopants, such as gallium, may be a strategy to circumvent this degradation issue,<sup>177</sup> provided that homogeneous doping through a full ingot can be established. In either case, the use of high-lifetime wafers with classic device structures such as the so-called aluminum back surface field solar cell would only marginally improve device performance. To better exploit the merits of n-type wafers motivates the introduction of alternative device architectures, of which the two most archetypical are the interdigitated-back-contact solar cell and the heterojunction solar cell.

Finally, as described in Section 2.2, monocrystalline and multicrystalline wafers are obtained from a wire-cutting process, with a typical associated kerf loss of about 100  $\mu\text{m}$  per cut wafer. This explains the quest for “kerf-less” crystalline silicon technologies, including silicon ribbon growth,<sup>178,179</sup> film (re-)crystallization,<sup>180–182</sup> and silicon epitaxial growth,<sup>183–189</sup> possibly combined with lift-off, controlled spalling or other techniques to detach thin silicon absorbers from a thicker substrate<sup>190,191</sup> or growth template.<sup>192,193</sup> Several strategies have been developed to increase light coupling in ultra-thin silicon (<50  $\mu\text{m}$ ) and fabricate solar cells from such material.<sup>194–204</sup> In particular Solexel’s 239.7  $\text{cm}^2$  cell using 35  $\mu\text{m}$ -thick silicon delivered a remarkable power conversion efficiency of 21.2%.<sup>11</sup>

## 4. Archetypal high-efficiency concepts

### 4.1. Interdigitated-back-contact solar cells

Whereas the very first crystalline silicon solar cell, developed at Bell Labs, USA, featured already a back-contact architecture,<sup>205,206</sup>



the modern interdigitated-back-contact (IBC) cell originally envisioned for applications under concentrated illumination has its origins in the late 1970s.<sup>207–209</sup> The first successful commercialization was by SunPower, with a device architecture derived from earlier work at Stanford University.<sup>210</sup> With its most recent technological improvements, SunPower has demonstrated an efficiency of 25.2% under one-sun operation.<sup>12</sup> A SunPower module has achieved a 22.8% conversion efficiency, which is the current world record for a large-area crystalline silicon photovoltaic module (15 739 cm<sup>2</sup> aperture area; a smaller module with a 778 cm<sup>2</sup> designated illumination area by UNSW reached an efficiency of 22.9%, see Fig. 1).<sup>12</sup>

An important factor for this high performance is the fact that IBC cells achieve high short-circuit currents by completely eliminating metal grid shading at the front surface (Fig. 7). In the IBC design, both electron and hole collection occur at the rear side of the device. This permits a high degree of freedom in the optical and electronic design of the front side of the cell, evidenced by a short-circuit current density as high as 41.33 mA cm<sup>-2</sup> for the record IBC cell. Front surface passivation, for example by silicon oxide in combination with silicon nitride as an anti-reflection layer, can be complemented by a lightly diffused n-type layer, which suppresses the concentration of holes near the pyramidal textured surface. Other possibilities for maximizing light coupling into the wafer include the use of black silicon as a broadband antireflection coating,<sup>211–214</sup> and multiscale surface texture.<sup>215</sup> Nevertheless, it is essential that such optical schemes be compatible with high-quality surface passivation.

In a possible fabrication sequence, boron diffusion is applied to part of the back surface to selectively transport holes. In the remaining part of the back surface, phosphorus is locally diffused to selectively collect electrons. Hence the cell structure consists of alternating, or interdigitated, stripes of n-type and p-type doped regions. Optimization of the widths of the stripes is essential for effective carrier collection and depends on the carrier diffusion length and on the recombination properties of the phosphorus- and boron-doped regions. Since electron mobility is approximately three times higher than hole mobility in moderately

doped silicon, some IBC structures favor a one-dimensional flow to holes, by covering a larger fraction of the rear side (for example, around 75%) with a p<sup>+</sup> region. This also reduces the buildup of hole concentration at the front surface, which would exacerbate recombination there. Electrons flow mostly laterally towards the n<sup>+</sup> rear stripes, not only through the n-type wafer, but also through the front n<sup>+</sup> diffusion, when present. Nevertheless, the IBC cell structure needs to be specifically optimized for a given set of recombination and transport properties.

A thin insulating layer is used to passivate the back surface of the wafer.<sup>216</sup> Electrical contact is made by metal stripes through local openings etched into the passivation layer. The metal stripes are aligned to the doped regions but they are slightly narrower, to avoid overlap with neighboring stripes, which would cause a shunt. The openings must be large enough to extract current with minimal contact resistance losses and small enough to minimize recombination losses caused by the direct contact of the metal to the silicon. A high fill factor of 82.7% was achieved for the record IBC cell, despite its large area, with this local contact design. A significant advantage of placing both metal contacts at the rear is that they can be optimized without having to trade off resistance for shading. The metal stripes can, in fact, almost fully cover the rear surface, and thus simultaneously act as a back reflector. The thin dielectric layer between the silicon and the metal stripes helps to minimize parasitic plasmonic absorption of infrared light in the metal layer.<sup>132</sup>

An alternative to minimizing the contact area between the doped silicon and the metal stripes is to incorporate passivating contacts based on doped polysilicon layers,<sup>287</sup> which can relax those requirements. With an open-circuit voltage of 737 mV, the record IBC cell demonstrates remarkable bulk lifetime, surface passivation and contact passivation. However, in terms of open-circuit voltage, silicon heterojunction technology can provide even better performance.

#### 4.2. Silicon heterojunction solar cells

The silicon heterojunction (SHJ) solar cell was pioneered in the early 1990s by Sanyo (acquired in 2010 by Panasonic) and has been commercialized under the HIT trademark (heterojunction with intrinsic thin layer).<sup>44,217</sup> Using this concept, Kaneka, Japan, has recently achieved a cell efficiency of 25.1%.<sup>370</sup> Panasonic's HIT technology now yields commercial module efficiencies approaching 20%.<sup>218</sup> In 2014, Panasonic demonstrated a new world record efficiency of 25.6% by combining their HIT technology with the IBC concept.<sup>3</sup> The approximate current density–voltage characteristics of this record cell are compared to the ideal, Auger-limited, solar cell in Fig. 2. The ideality factor and series resistance values for the simulated IBC HIT cell in Fig. 2 were chosen so as to replicate the experimentally measured fill factor of 82.7%. As can be seen in Fig. 2,  $J_{sc}$  and  $V_{oc}$  of the record cell are lower than the ideal values, but the largest difference with the ideal limit occurs at the maximum power point. Whereas in the intrinsic limit case the low ideality factor of  $n = 0.675$ , typical of Auger recombination in high injection, leads to a very high FF = 89.3%, other recombination mechanisms (probably at the surfaces) at the lower injection conditions of maximum power, or series

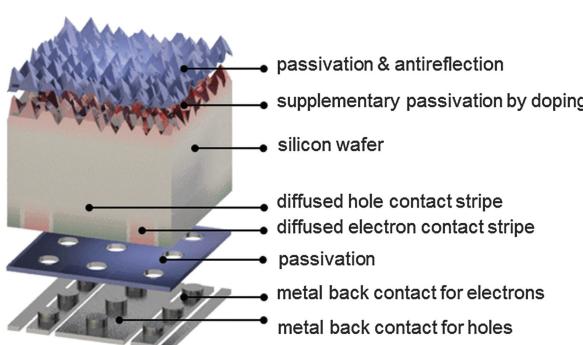


Fig. 7 Schematic of the components of an interdigitated-back-contact cell. Both electrons and holes are extracted through the rear via locally diffused phosphorus and boron stripes that are contacted to individual metal stripes via local openings in the dielectric passivation layer.



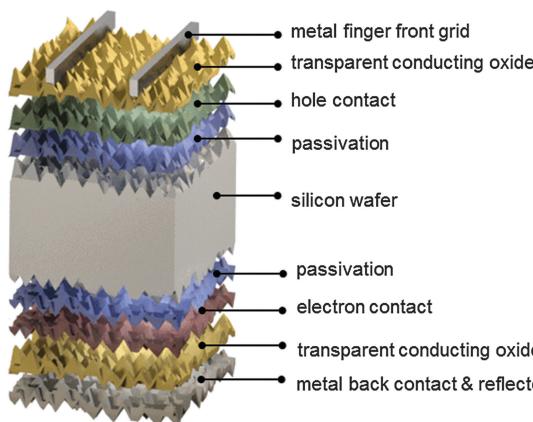
resistance effects, prevail in the HIT cell and place a cap on the FF.<sup>370</sup> In the following we focus on the original two-side contacted silicon heterojunction solar cell.

The silicon heterojunction concept is based on two critical innovations. First, it makes use of a thin hydrogenated amorphous silicon layer to achieve excellent surface passivation.<sup>42,43,45</sup> To ensure such passivation, it is critical that deposition processes be tuned to obtain atomically sharp interfaces between the wafer and buffer layers, devoid of any unintentionally grown epitaxial silicon.<sup>219–222</sup> Second, this thin passivating film is inserted underneath the electron-selective and hole-selective contact layers,<sup>44</sup> yielding virtually recombination-free surfaces, even for the areas contacted by the metal electrodes (Fig. 8). This translates into a very high open-circuit voltage,<sup>223</sup> with values as high as 750 mV, obtained by Panasonic for a two-side-contacted cell with an efficiency of 24.7%.<sup>218</sup> Note that the theoretical, Auger-limited open-circuit voltage for a wafer with similar thickness ( $\sim 110 \mu\text{m}$ ), is 761 mV,<sup>17,224</sup> underlining the remarkable passivation achieved with this technology.

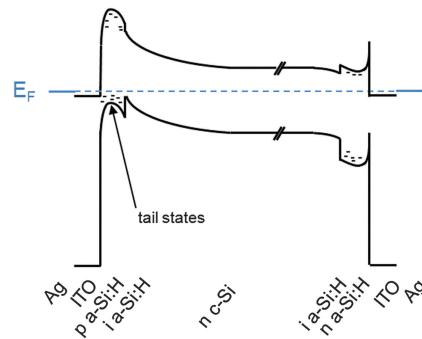
The fabrication process sequence starts with surface texturing and cleaning, followed by passivation of both sides of the silicon wafer with a thin layer of intrinsic hydrogenated amorphous silicon.<sup>46</sup> These films are usually deposited by plasma-enhanced chemical vapor deposition and measure only about 5 nm in thickness.<sup>225–227</sup> These films can be considered the “heart” of the silicon heterojunction solar cell, as they yield very effective passivation, while simultaneously being transparent for charge carrier transport. As a consequence, their electronic<sup>228–231</sup> and microstructural<sup>232,233</sup> properties as well as their deposition processes<sup>234–238</sup> have been extensively studied. Rather than relying on dopant diffused regions of the same material (crystalline silicon) to separate the charge carriers, in silicon heterojunction

technology such separation is achieved by a combination of doping and use of a wider band gap material, producing nearly ideal carrier-selective contacts. To form these, doped amorphous silicon layers with thicknesses of about 10 nm are deposited on top of the intrinsic layer. Boron is used as a dopant to obtain a p-type layer for transporting the holes, and phosphorus is used to obtain an n-type layer for conducting the electrons. Both dopants are incorporated into the films by adding relevant precursor gasses during film deposition, such as trimethylboron and phosphine. Direct deposition of the doped layers on the crystalline silicon surface degrades passivation, as dopant incorporation generates a significant amount of recombination-active defects in amorphous silicon, explaining the need for intrinsic buffer layers in this technology.<sup>239,240</sup> The doped layers may alter the surface passivation when deposited on the intrinsic buffer layers because they can change the carrier concentrations inside the wafer (this is evidenced in Fig. 9 by a bending of the energy bands in equilibrium).<sup>241</sup> Interestingly, the silicon heterojunction process sequence can be easily applied to either n-type or p-type wafers,<sup>242</sup> with n-type wafers delivering slightly higher efficiencies due to the fact that such surfaces are usually easier to passivate than their p-type counterparts, as discussed above. With this technology it is also fairly straightforward to change the polarity of the device.<sup>46,162,243,244</sup> Due to the asymmetric band offsets at the amorphous/crystalline silicon interface, holes usually face a larger barrier than electrons, potentially hindering efficient carrier collection (see Fig. 9).<sup>245,246</sup>

Full-area contacts are formed by sputtering an indium tin oxide transparent front electrode. As the lateral conductivity of the doped amorphous silicon films is relatively poor, lateral current transport to the metal fingers needs to be provided by the transparent conductive oxide film, requiring a relatively low sheet resistivity of about  $50\text{--}100 \Omega \square^{-1}$ , similar to that of a



**Fig. 8** Schematic of the components of a silicon heterojunction cell. The front and rear surfaces of the n-type silicon wafer are passivated by an intrinsic hydrogenated amorphous silicon layer. Contact to holes and electrons is established by subsequently depositing a boron-doped p-type and phosphorus-doped n-type hydrogenated amorphous silicon on the front and rear respectively. Lateral transport of holes at the front to the silver finger grid is achieved employing an indium-oxide-based transparent electrode which simultaneously acts as antireflection coating. A transparent conductive oxide is also employed at the back side to minimize parasitic plasmonic absorption in the silver back reflector.



**Fig. 9** Energy band diagram of a silicon heterojunction solar cell in equilibrium showing the valence band offset at the interface between the n-type crystalline silicon (n c-Si) absorber and the intrinsic hydrogenated amorphous silicon passivation layer (i a-Si:H). Representative values were used for the modelling of the curves with the program PC1D<sup>66</sup> (n-type wafer doped with  $1 \times 10^{15} \text{ cm}^{-3}$  electrons, amorphous silicon with a band gap of 1.8 eV, and electron and hole concentrations of  $1 \times 10^{19} \text{ cm}^{-3}$  for n-type and p-type amorphous silicon respectively; for indium tin oxide (ITO), a band gap of 3.3 eV and an electron concentration of  $1 \times 10^{21} \text{ cm}^{-3}$  were chosen). Layer thicknesses along the horizontal axis are not to scale, for readability. In particular, the depletion region extends about  $1.5 \mu\text{m}$  into the crystalline silicon wafer.

typical diffused region in classic crystalline silicon solar cells. Thanks to its low refractive index of about 2, this layer is also well suited as an antireflection coating (sometimes in conjunction with a second layer of magnesium difluoride to further minimize reflection losses).<sup>60</sup> The transparent conductive oxide is also important to guarantee a sufficiently low contact resistivity, explaining its use at the rear side as well. There, it also helps to reduce parasitic plasmonic absorption of light at the silver back contact, in case this metal is deposited as a blanket layer.<sup>132</sup> The cells are finalized by screen printing a silver finger and busbar grid on the front side; copper-plated metallization is an attractive alternative.<sup>247–249,370</sup>

Compared to the IBC concept, which produces a current density of  $41.8 \text{ mA cm}^{-2}$ , the silicon heterojunction cell from Kaneka, featuring contacts on opposite sides, delivers a slightly lower short-circuit current density of  $40.8 \text{ mA cm}^{-2}$ . These losses are caused not only by grid shading, but also by parasitic absorption in the window layers. Optical losses at the front and back surface of silicon heterojunction cells were analyzed in detail in ref. 227 and 250. At the front side, parasitic absorption in the doped and intrinsic amorphous silicon layers with a relatively narrow band gap of about 1.8 eV represents the main contribution to current losses in the blue and ultraviolet part of the spectrum. In the red and infrared part of the spectrum, current is lost mainly through free-carrier absorption in the front and back indium tin oxide electrodes as well as through parasitic plasmonic absorption in the silver back reflector.

Several approaches to improve the short-circuit current of silicon heterojunction cells have been explored, including the replacement of the doped amorphous silicon layers by wider band gap hydrogenated amorphous silicon oxide<sup>245,251,252</sup> or silicon carbide layers,<sup>253,254</sup> or by replacing the indium tin oxide with higher mobility transparent conductive oxides such as hydrogen-doped indium oxide,<sup>255–263</sup> tungsten-doped indium oxide,<sup>264</sup> cerium-doped hydrogenated indium oxide,<sup>265</sup> and amorphous indium zinc oxide.<sup>266</sup> While such transparent conductive oxides clearly lead to an increase in the current density, the use of hydrogenated amorphous silicon oxide or silicon carbide often results in a reduced fill factor, and neutralizes the gains in short-circuit current. In general, fill factor losses related to transparent conductive oxides are due to a suboptimally matched work function,<sup>267,268</sup> or to increased sheet or contact resistances between the transparent conductive oxide and the doped amorphous silicon layers.<sup>269</sup> Transparent conductive oxides typically exhibit n-type conductivity and consequently readily form an Ohmic contact to n-type hydrogenated amorphous silicon. As p-type transparent conductive oxides suffer from relatively low hole mobilities caused by the large effective hole mass of most oxides,<sup>270</sup> contact to p-type amorphous silicon is also commonly established with n-type transparent conductive oxides.<sup>271</sup> This recombination junction requires a relatively high carrier concentration in the oxide at least near the interface with p-type amorphous silicon to enable tunneling of carriers across the interface and avoid fill factor losses.<sup>259</sup> The deposition process for transparent conductive oxides, such as sputtering, may also lead to undesired performance losses.<sup>272</sup> These combined

factors motivate the engineering of gently deposited, well-tuned transparent conductive oxides, possibly as multi-layer stacks.<sup>273</sup>

An alternative approach has made use of a perforated insulating magnesium difluoride layer between the amorphous silicon and transparent indium oxide back electrode, which improves the infrared response significantly as the reflection is increased due to higher refractive index contrast.<sup>274</sup> Finally, conformal atomic layer deposition of transparent conducting oxides on black silicon has been demonstrated,<sup>275</sup> possibly offering optical advantages. It remains to be seen whether similarly conformal amorphous silicon layers can be produced, yielding efficient devices.

## 5. Emerging concepts and technologies

### 5.1. Passivating contacts

As discussed in the previous sections, passivating the two surfaces of the silicon wafer is key to achieving high performance. Ultimately, such passivation should extend to underneath the metal contacts, but, given that most passivating materials are insulators, simultaneously suppressing surface recombination and conducting electrical current is challenging. Silicon heterojunction technology has achieved this, thanks to its use of a semiconductor, intrinsic hydrogenated amorphous silicon, instead of an insulator as the passivating layer. These contacts are somewhat similar to the so-called SIPOS approach – essentially a mixture of microcrystalline silicon and silicon dioxide – which demonstrated  $V_{oc}$  values of 720 mV in the mid-1980s.<sup>276</sup> The latest IBC cells from SunPower also incorporate an undisclosed passivating contact, yielding open-circuit voltages of up to 737 mV. In this section we describe other possibilities that are based on the use of passivating interlayers thin enough to permit quantum-mechanical tunneling.

The idea of using an ultra-thin layer of silicon oxide between metal and semiconductor was exploited in early metal insulator semiconductor (MIS) solar cells<sup>277,278</sup> and subsequently applied to devices that had an n-p junction (MINP).<sup>279</sup> The use of an ultra-thin film of aluminium oxide deposited by atomic layer deposition onto a phosphorus-diffused region has recently been found to increase the open-circuit voltage by 15 mV, at the expense of a tolerable increase in contact resistance.<sup>280,281</sup> Another recent development is an enhanced MIS approach, in which the chemical passivation afforded by a thermal silicon oxide tunnel layer is enhanced by hydrogen originating from a hydrogenated amorphous silicon layer that is carefully alloyed with aluminum.<sup>282</sup> This enhanced MIS contact has been applied to the back side of  $p^{+}nn^{+}$  solar cells, which achieved a 21% efficiency.<sup>283</sup>

Even more effective is to place a  $\sim 1.2 \text{ nm}$ -thick silicon oxide layer underneath a  $\sim 30 \text{ nm}$ -thick doped polycrystalline (or mixed amorphous/crystalline) silicon film to form what in bipolar transistor technology has been called a polysilicon contact. The thin interlayer can be formed by low-temperature thermal oxidation, immersion in a chemical bath, or by ozone treatment.



Selective tunnelling of one type of carrier through the oxide film is required for effective current transport, explaining the need for accurate control of the oxide thickness. The silicon layer is usually deposited by plasma-enhanced chemical vapor deposition, either directly as polycrystalline silicon or as hydrogenated amorphous silicon. Frequently a dopant (phosphorus or boron) is incorporated *in situ*,<sup>284</sup> alternatively, it can be subsequently introduced by ion implantation,<sup>285</sup> thermal diffusion from a gaseous source<sup>286</sup> or from a doped oxide.<sup>287</sup> In all cases, the dopant is activated at a temperature in the range of 800–900 °C, which partially crystallises the initial amorphous silicon layer. Lastly, a hydrogenation treatment, either from a plasma or from annealing in forming gas (*i.e.* a mixture of nitrogen and hydrogen), is used to further reduce interface recombination. The high temperatures used to form polysilicon contacts makes them, in principle, compatible with the firing-through of a screen-printed front metal grid,<sup>288</sup> although it is still unclear if such a process may be applied to the thin polysilicon layer itself. The performance achieved by phosphorus-doped polysilicon contacts is similar to that achieved by the silicon heterojunction technology in terms of recombination current density, which can be as low as  $J_{oc} \approx 1\text{--}10 \text{ fA cm}^{-2}$ , together with contact resistivities approximately one order of magnitude lower than the silicon heterojunction technology,  $\rho_c \approx 20 \text{ m}\Omega \text{ cm}^2$ .<sup>282–284</sup> The application of a tunneling oxide plus an n<sup>+</sup> silicon film coated with silver as a full-area rear contact has led to a 25.1% efficient solar cell, using a textured front side, but planar rear side.<sup>289</sup> Nevertheless, contacts based on p<sup>+</sup> polysilicon seem to be harder to optimize, possibly related to excessively large valence band offsets with the silicon wafer, and their selectivity parameters are not yet as good as those of n<sup>+</sup> contacts.<sup>290</sup> The 25.1% device mentioned above was made on an n-type silicon wafer that also incorporated a selective boron diffusion on the front surface (heavier under the metal fingers). Similar devices that combine a thermal boron diffusion with a rear n<sup>+</sup> polysilicon/silicon oxide contact have been reported recently, albeit with lower efficiencies.<sup>8</sup>

## 5.2. Dopant-free electron and hole contacts

All contacting concepts discussed so far employ extrinsic doping as a means to move the Fermi level of the contact region close to the valence or conduction band of the absorber to achieve hole or electron selectivity, respectively. Doping has a number of serious drawbacks. In diffused homojunction cells, heavy doping, which is required to keep the contact resistance to the metal fingers low and consequently to reach high fill factor, leads to Auger recombination, which negatively affects both open-circuit voltage and short-circuit current, in particular the blue response. In silicon heterojunction cells, doping of the amorphous silicon layers creates recombination-active defects that negatively affect passivation, rendering the use of an intrinsic amorphous silicon buffer layer mandatory.<sup>240</sup> Again this negatively affects the blue response and, consequently, the short-circuit current, as the band gap of amorphous silicon is only 1.8 eV.<sup>250</sup> These shortcomings motivate the search for dopant-free contact concepts compatible with silicon.

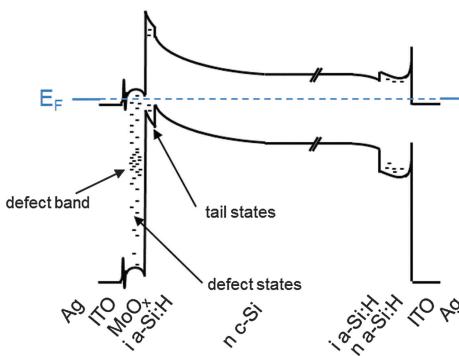
A glimpse outside silicon photovoltaics proves that doping is not a necessary ingredient for solar cell construction.<sup>291</sup> Cadmium telluride (CdTe) thin-film solar cells use a thin, undoped, naturally n-type cadmium sulfide layer with a low carrier concentration,<sup>292</sup> deposited typically by chemical bath deposition, as an electron-selective contact. They also use a naturally p-type zinc telluride layer to facilitate hole extraction out of the cadmium telluride absorber layer to the molybdenum metal back contact. A similar strategy is used also for copper indium gallium selenide (CIGS) and copper zinc tin selenide (CZTS) solar cells. As early as 1977, cadmium sulfide was tested as an electron-selective contact to p-type silicon, but efficiencies remained below 10%.<sup>293</sup>

Dye-sensitized solar cells, in their earliest implementations, used titanium dioxide (TiO<sub>2</sub>) to extract electrons and the redox potential of a liquid iodide/triiodide electrolyte to extract the holes from a photoexcited dye absorber.<sup>294</sup> Titanium dioxide is still a popular electron contact and is also commonly employed for lead halide perovskites<sup>295</sup> and even III-V absorbers.<sup>296</sup> A heterojunction solar cell employing a p-type silicon absorber with a titanium dioxide electron contact was reported in ref. 297, but suffered from a low open-circuit voltage of 520 mV and, consequently, low efficiency. The application of TiO<sub>2</sub> to n-type silicon wafers, motivated by evidence of reasonably good surface passivation,<sup>298,299</sup> has been more successful. Recently, a 19.8% efficient n-type silicon solar cell with a front boron diffusion and a rear full-area TiO<sub>2</sub> passivating contact has been reported.<sup>300</sup> Adding a tunneling silicon oxide layer to the contact structure further reduced recombination, and led to a 20.5% conversion efficiency.<sup>301</sup>

To extract holes, lead halide perovskite solar cells typically employ a p-type polymer such as 2,2',7,7'-tetrakis(*N,N*-di-*p*-methoxyphenylamine)-9,9'-spirobi-fluorene (spiro-OMeTAD). P-type polymers including spiro-OMeTAD or poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) have also been employed as hole front contacts for n-type crystalline silicon, and have recently reached an efficiency of 13.8% (see supplementary information in ref. 302 for a compilation of polymer/silicon hybrid cell performance data preceding the cells reported in ref. 303). Nevertheless, their air and ultraviolet stability remains a major concern.<sup>304</sup> As an alternative to polymer contact layers, the organic photovoltaic community introduced transition metal oxides as hole-selective contacts. In particular the adoption of substoichiometric molybdenum trioxide (MoO<sub>x</sub>,  $x < 3$ ) led to significant improvements in device performance and stability.<sup>305,306</sup>

The use of substoichiometric molybdenum trioxide (MoO<sub>x</sub>) as a hole contact for n-type crystalline silicon was first introduced in ref. 302. With its very high work function of up to 6.6 eV, exceeding that of elemental metals, MoO<sub>x</sub> can act as an efficient hole contact without the use of doping. While the first MoO<sub>x</sub>-silicon heterojunction cell reached an efficiency of only 14.3%, it already outperformed the best polymer/silicon hybrid cells at that time. Subsequently, an efficiency of 16.4%<sup>307</sup> followed by 16.7%<sup>308</sup> was achieved for a solar cell made by depositing MoO<sub>x</sub> directly onto an n-type silicon wafer.





**Fig. 10** Energy band diagram of a  $\text{MoO}_x$ -silicon heterojunction solar cell in equilibrium. Comparison with Fig. 9 reveals that n-type  $\text{MoO}_x$  has an effect similar to that of p-type amorphous silicon on band bending in the crystalline silicon absorber due to its high work function. Representative values were used for the modelling of the curves with the program PC1D<sup>66</sup> (n-type crystalline silicon wafer doped with  $1 \times 10^{15} \text{ cm}^{-3}$  electrons, amorphous silicon with a band gap of 1.8 eV and electron concentration of  $1 \times 10^{19} \text{ cm}^{-3}$  for the n-type amorphous silicon; for  $\text{MoO}_x$  and ITO, a band gap of 3.3 eV and an electron concentration of  $1 \times 10^{16}$  and  $1 \times 10^{21} \text{ cm}^{-3}$  were assumed). Layer thicknesses along the horizontal axis are not to scale for readability. In particular, the depletion region extends about 1.5  $\mu\text{m}$  into the crystalline silicon wafer.

A significant boost in efficiency was achieved by combining the  $\text{MoO}_x$  hole contact with an intrinsic hydrogenated amorphous silicon passivation layer.<sup>309</sup> The cell structure is identical to the silicon heterojunction cell discussed in Section 4.2., but replaces the narrow band gap p-type amorphous silicon layer with the wide band gap  $\text{MoO}_x$  (3.3 eV, see Fig. 10), resulting in a substantial current gain of  $1.9 \text{ mA cm}^{-2}$ , thanks to an improved capture of the blue and ultraviolet region of the spectrum, and a respectable efficiency of 18.8%. Importantly, the open-circuit voltage of this cell was as high as for a co-processed silicon heterojunction reference cell with the standard amorphous silicon layer, demonstrating that  $\text{MoO}_x$  deposition did not deteriorate the surface passivation. However, due to a low fill factor of only 67.2%, the cell efficiency did not exceed the 20% benchmark.

The fill factor issue was finally solved in ref. 310, where the annealing temperature after screen printing of the silver finger grid was reduced from 200 to 130 °C. Low-temperature annealing avoids the formation of an interfacial layer between  $\text{MoO}_x$  and the indium oxide transparent electrode, which is believed to be responsible for the low fill factor previously observed. A remarkable fill factor of 80.4% and an independently certified efficiency of 22.5% were finally obtained by replacing the screen-printed finger grid with a copper-plated finger grid, which does not require annealing at 200 °C.<sup>310</sup>

The use of  $\text{MoO}_x$  as an excellent Ohmic contact to p-type silicon even without a passivation layer was proposed in ref. 311. Contact resistivities as low as  $0.2 \text{ m}\Omega \text{ cm}^2$  and recombination current densities of  $200 \text{ fA cm}^{-2}$  were demonstrated. Consequently, an interesting application of  $\text{MoO}_x$  is as a hole contact at the back of p-type silicon solar cells, where it can replace local p<sup>+</sup> regions formed by aluminum alloying or boron diffusion. A proof of concept device with an efficiency of 20.4% has

been demonstrated.<sup>312</sup> A device employing a PEDOT:PSS full area hole contact at the back of a p-type (n-type) silicon solar cell reached an efficiency of 20.6% (18.3%).<sup>313,314</sup> Implementing PEDOT:PSS at the flat back avoids the challenges associated with spin coating on a textured surface and resolves the issue with ultraviolet stability.

## 6. Summary and outlook

### 6.1 Summary of silicon solar cells

The rapid progress during the last ten years in the field of silicon photovoltaics has consolidated early laboratory results into large-area, industrially made devices (see Fig. 1). While the fabrication of the 25% efficient, 4  $\text{cm}^2$  PERL cell in 1999 cell required several photolithography steps, the photovoltaic industry has adapted the key ingredients of that cell design to large volume production, and Trina Solar has recently reported an independently certified efficiency of 22.13%.<sup>12,315</sup> In the meantime, several conceptually very different technologies have managed to reach or cross the 25.0% efficiency barrier (see Table 1). These include Panasonic's 25.6% efficient cell combining the HIT with the IBC approach, SunPower's 25.2% IBC cell, Kaneka's 25.1% silicon heterojunction cell, which tops the 24.7% HIT cell record set by Panasonic in 2012, and Fraunhofer's 25.1% cell featuring a tunneling oxide passivated contact (TOPCon). It is remarkable that with the exception of the 4  $\text{cm}^2$  TOPCon cell, all these cells were certified for areas exceeding 100  $\text{cm}^2$ .

From Fig. 1, a similar scenario can be observed for modules. Indeed, while the best module efficiency achieved to date (22.9%, by UNSW) was certified as early as 1996 for a minimodule area of 778  $\text{cm}^2$ , SunPower has demonstrated an independently certified full-sized 15 739  $\text{cm}^2$  module with an efficiency of 22.8%.<sup>12</sup> Although this review has not described module fabrication technologies, the trends shown in Fig. 1 indicate that it is just a question of time until progress in solar cell performance translates into higher module efficiencies. This applies both to best-of-a-kind modules and to those produced at large scale.<sup>316</sup>

Two ingredients are necessary at the cell level to achieve high efficiency: an excellent interface passivation scheme and efficient carrier-selective contacts. While classic crystalline silicon solar cells use doping to achieve the latter, several dopant-free concepts have emerged. Molybdenum oxide has been proved to function as a highly efficient hole contact for both n-type and p-type silicon.<sup>302,307–310</sup> Such dopant-free contact concepts show great promise for silicon solar cells as a potential route to minimize Auger recombination in the carrier-selective regions. Fully dopant-free silicon solar cells are under development at several research laboratories.<sup>317,318</sup> The dopant-free device with the highest reported efficiency, close to 20%,<sup>319</sup> uses a molybdenum oxide film as a hole-collecting layer and a stack of lithium fluoride and aluminum as the electron-collecting contact. Underneath both contacts, intrinsic hydrogenated amorphous silicon films are inserted for interface passivation.



It is known, not only from the photovoltaic industry, but also from the semiconductor and battery industries, that it may easily take 10 or 20 years to bring new materials and concepts to the market. In principle, a new concept must offer advantages, not only in terms of the properties of its constituent materials, but also in view of their integration into the device, achievable device performance, manufacturability and yield, operational stability, reliability, and cost. The \$/W ratio is still a commonly used metric to quantify the cost *vs.* output power trade-off of different photovoltaic technologies. In recent years, it has become clear that a more relevant metric is the leveled cost of electricity (LCOE), as photovoltaics are competing against other technologies to provide energy in an economic manner. The LCOE, given in units of \$/kW h, takes into account not only the cost to build, but also to operate, a system over its lifetime, divided by the total energy output over that lifetime. It is important to realize that a higher efficiency at the cell level impacts the LCOE positively, with a large leverage, while reducing the cost per cell in a module affects the LCOE only marginally, as the sum of fixed costs associated with the glass, back sheet, junction box and balance of system cost, *etc.* dominate.<sup>320</sup> Consequently, there is an opportunity for new concepts to be economically viable even at higher cost.

## 6.2 Outlook beyond single-junction solar cells

Ultimately, the efficiency of silicon photovoltaics will be limited by Auger recombination (once all contributions to parasitic light absorption, defect-induced recombination and resistive losses are eliminated) inherent to the operation of silicon absorbers in a single-junction architecture under one-sun illumination. Over the past decades, several advanced concepts have been proposed to overcome the single-junction limit of silicon solar cells. These ideas are often referred to as “third-generation” photovoltaics,<sup>321</sup> ultimately aiming to approach the thermodynamic limit of 93%.<sup>322</sup> Of the different proposed methods, a few may also hold some promise to enhance the efficiency of single-junction silicon solar cells,<sup>323</sup> such as spectral downshifting,<sup>324</sup> and up- and down-conversion.<sup>325–328</sup> Yet, arguably the most straightforward strategy to significantly boost efficiency is the tandem architecture, where silicon offers a nearly ideal band gap value to act as the bottom cell in a two-subcell configuration with a top cell with an ideal band gap of 1.7–1.8 eV. In a two-terminal tandem device, the total number of incident photons is ideally split equally between the two subcells, so that the number of electron–hole pairs generated in each subcell is the same, resulting in a “matched” photogenerated current density (see Fig. 11).

The current density in a tandem is, therefore, half that of a silicon solar cell. The voltage of the two-terminal tandem device is the sum of the voltages of the individual subcells. Given that the material placed on top of the silicon has a wider band gap, it can be expected to produce a higher voltage. Hence the voltage of the tandem cell can be expected to be more than two times higher than the voltage of the single silicon cell, thus resulting in a greater output power. To what extent the voltage, and hence the efficiency, increases depends on technological factors such as interface passivation and contact strategies.

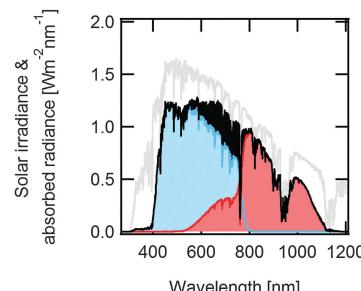


Fig. 11 Solar spectral irradiance (air mass 1.5 global spectrum) and contributions absorbed by the top (blue) and bottom cell (red) of a two-terminal perovskite/silicon tandem solar cell.<sup>361</sup> The total absorbed radiance includes the black area.

From a pure performance perspective, the most attractive tandem uses a III–V semiconductor solar cell with the appropriate band gap, such as *e.g.* indium gallium nitride (InGaN) or indium gallium phosphide (InGaP), as the top cell in combination with a silicon bottom cell.<sup>329–333</sup> In a four-terminal configuration, efficiencies as high as 29.8% were recently demonstrated for a mechanically stacked III–V/silicon tandem.<sup>12</sup> Despite this high efficiency, monolithic two-terminal tandems represent arguably the most elegant tandem design but pose formidable challenges in terms of hetero-epitaxial material growth.<sup>334–338</sup> III–V/silicon tandem solar cells fabricated *via* growth of III–V layer stacks on epitaxial substrates combined with lift-off and layer transfer techniques have been demonstrated, but remain difficult to scale to large volume production.<sup>339–343</sup> However, a method for the growth of III–V layers on non-epitaxial substrates has recently been introduced that could change this situation.<sup>344,345</sup>

A recent analysis revealed that established thin-film technologies based on hydrogenated amorphous silicon or the family of copper indium gallium selenide (CIGS) and copper zinc tin selenide (CZTS) compounds cannot offer a wide band gap top cell with sufficient efficiency to improve or even maintain the efficiency of a > 25.0% efficient bottom cell.<sup>346</sup> If the silicon cell is dominated by Auger recombination, a halving of the number of photogenerated electrons and holes also implies that its open-circuit voltage gets reduced by 12 mV, compared to full one-sun illumination (18 mV or more if dominated by extrinsic recombination).

A suitable top cell for high-efficiency crystalline silicon bottom cells may be offered by organic–inorganic perovskites.<sup>347–349</sup> This material class has only recently been considered for photovoltaic applications, and has achieved a fast progress in device efficiency ever since.<sup>350–355</sup> The best single-junction devices use lead-halide-based perovskites as the optical absorber, and have reached efficiencies as high as 21%.<sup>356</sup> The band gap of the perovskite absorbers for these single-junction record devices is around 1.57 eV, which is lower than the ideal band gap of 1.7–1.8 eV of a top cell for a silicon-based tandem. Blending lead-iodide-based perovskites with their lead bromide counterparts can open the band gap to the ideal value of 1.7–1.8 eV.<sup>357,358</sup> Careful engineering of mixed-cation lead mixed-halide perovskites may resolve the photo-stability issues of wider band gap



perovskite absorbers.<sup>359</sup> Despite this, using the well-established 1.57 eV band gap lead-iodide-based perovskite can also already be a meaningful approach to significantly boost the efficiency of silicon solar cells; modelling predicts efficiencies of around 30%, largely independent of the precise device design.<sup>360</sup> In principle, a four-terminal device offers higher flexibility in device fabrication, as current matching does not need to be respected. However, two-terminal perovskite/silicon tandem solar cells are the most attractive combination of these technologies. The use of a silicon heterojunction solar cell as the bottom cell is particularly attractive.<sup>361,362</sup> This demands a perovskite top-cell fabrication process below 200 °C to avoid damage to the bottom cell. With this scheme, monolithic tandem efficiencies of 21% were recently obtained.<sup>359</sup> Due to the relatively low refractive index of perovskites,<sup>363</sup> the perovskite top cell could act as a “photovoltaic-active” antireflection coating for the bottom silicon solar cell.<sup>360</sup> A third possible approach to combine such different technologies is based on spectral splitting technology, with a demonstrated efficiency of 28%.<sup>364</sup>

The main challenge for tandem architectures is parasitic light absorption,<sup>365</sup> for two reasons. Firstly, because of the additional contact (and passivation) layers, additional parasitic absorption is difficult to avoid. Secondly, because the current is cut approximately to half, the overall power conversion efficiency is more strongly affected by optical losses. For example, a 1 mA cm<sup>-2</sup> loss in current density due to parasitic absorption in a single-junction crystalline silicon solar cell with 40 mA cm<sup>-2</sup> reduces the efficiency by 2.5%, while the same current density loss reduces the efficiency of a two-terminal tandem cell with 20 mA cm<sup>-2</sup> by 5%. These arguments hold in particular for perovskite top cells in a tandem architecture; a suitable hole contact layer for perovskite absorbers that overcomes these challenges has yet to be found; the search is ongoing for layers with broadband transparency that are deposited with a process that does not detrimentally affect the underlying layers.<sup>366–369</sup> On the other hand, the lower current density of a tandem solar cell should in principle allow for reducing Ohmic losses and indirectly allow for improving the current density, as more resistive contact and passivation layers can be integrated that may offer higher transparency. In addition, the higher voltage in the tandem configuration results in an increased tolerance with respect to slight voltage losses. Nevertheless, perovskite/silicon tandem solar cells that rival single-junction silicon cells have yet to be developed.

This review has focused on recent progress at the solar cell level in the fast-moving field of silicon photovoltaics. Many exciting developments occurring at the module and system levels could not be addressed here, even though they are equally important to ensure the economic competitiveness of solar electricity.

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