Accelerate JAX on Intel GPUs via PJRT

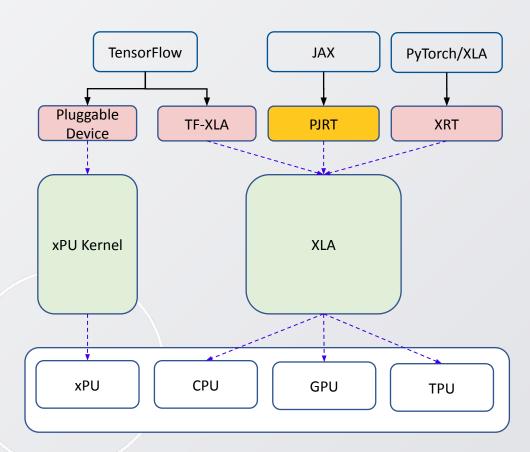
Xiao Yu, Google Yiqiang Li, Intel





#### **Problem**

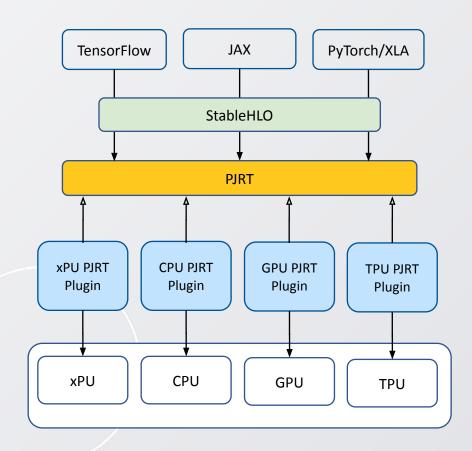
- Fragmented stack for different ML frameworks
- No way to add new hardware support in JAX
- TensorFlow has its own way for adding new hardware support
  - Cannot leverage compiler technologies





#### **PJRT**

- Unified pluggable device API --- PJRT
- A PJRT Plugin contains:
  - Hardware-specific compiler, which takes StableHLO as standard input IR.
  - Hardware runtime
- Decouple ML Framework and device PJRT plugin
  - Plugin are discovered and loaded as dynamic library





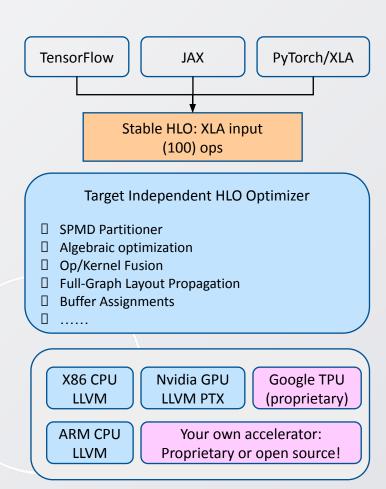
### PJRT: high level overview

- Scope: "Compile and Execute a StableHLO program"
- A PJRT Plugin will implement following APIs:
  - Compile: StableHLO -> PjrtLoadedExecutable
    - Trigger HW specific compiler to compile StableHLO into a HW executable
  - **H2D transfer:** host buffer, PjrtDevice -> PjrtBuffer
    - Prepare input by transferring data from host to HW
  - **Execute:** PjrtLoadedExecutable, PjrtDevice, PjrtBuffer -> PjrtBuffer
    - Execute the program on HW
  - D2H transfer: PjrtBuffer -> host buffer
    - Transfer output back to host



#### **OpenXLA**

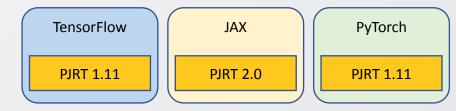
- It is challenging to build a new device compiler and runtime from scratch
- OpenXLA: Open, state-of-the-art ML compiler, using the best of XLA & MLIR
- Reusable target independent optimizer

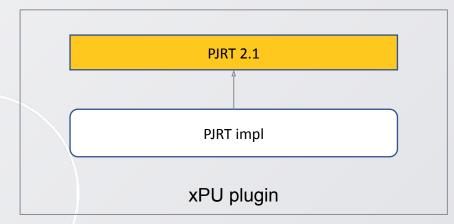




#### Versioning

- ML Frameworks and PJRT Plugins can be released separately
  - ML Frameworks and PJRT Plugins may use different version of PJRT.
- Proposal:
  - The program works as long as the framework and the plugin have the same Major version.

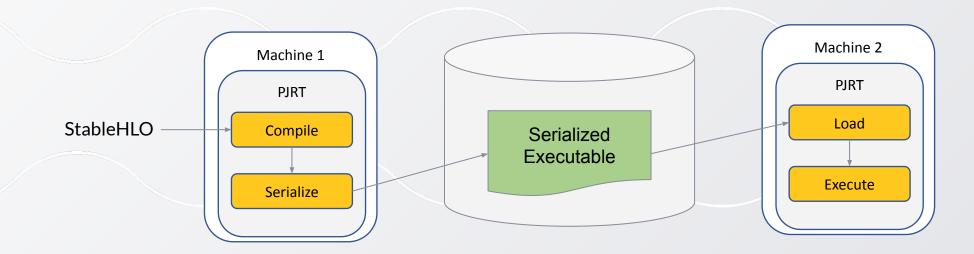






### **Ahead of Time Compilation**

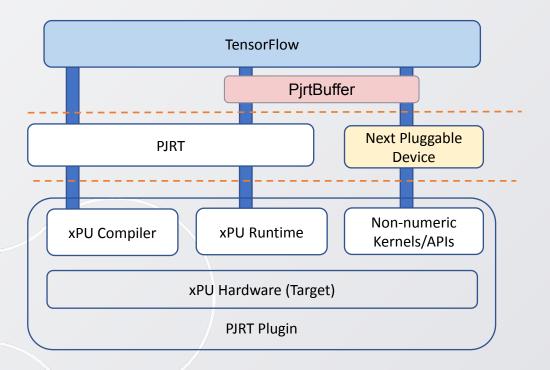
- Compile and execute StableHLO program on different machines
- Supported by Jax (done) and TensorFlow (WIP)
- PJRT Plugin is responsible for defining versioning and compatibility of serialized executable





#### **Custom Kernel support**

- Custom Kernels are critical to support
  - Operation that cannot be represented in StableHLO.
  - Hand-written kernel
- Use PjrtBuffer as the concurrency to enable efficient (O Copy) buffer sharing between PJRT and custom kernels
  - Implemented in TensorFlow as NextPluggableDevice API





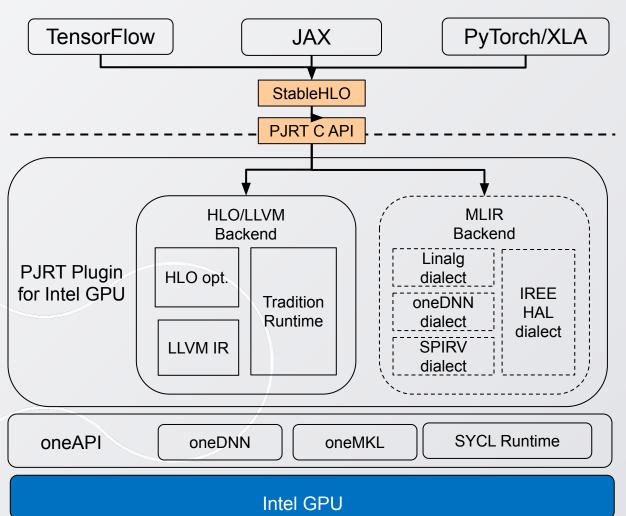
#### **PJRT - Future**

- Memory Space Support
  - Example use case: Nvidia Grace Hopper Superchip
- Sparsity Support
  - Enable ML compiler to optimize sparse computation
- MPMD Support
  - Enable more advanced Pipelining Parallelism



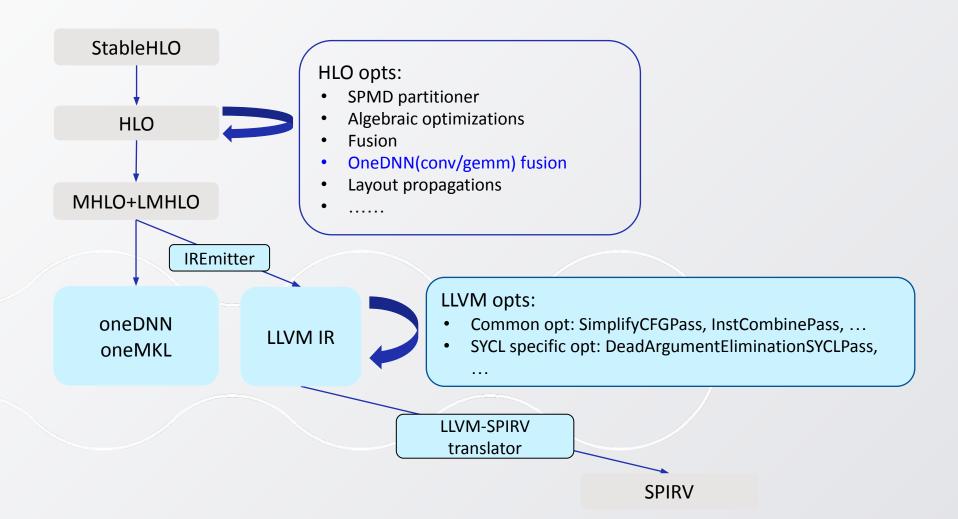
### PJRT Plugin for Intel GPU

- Intel GPU plugin integrates via PJRT API using oneAPI, and works on two code-gen techniques in parallel:
  - HLO/LLVM IR, release, runs JAX models
  - MLIR/IREE, experimenting, runs simple cases
- Release to support JAX (<u>link</u>)





#### PJRT Plugin for Intel GPU





### PJRT Plugin for Intel GPU --- Library Opt

- oneDNN
  - Conv/GEMM
  - Supported fusion pattern
    - Conv + [bias + add + activation]
    - [alpha \*] GEMM (A, B) + [beta \* C]
  - Graph API integration is coming soon to have more fusion capabilities
- oneMKL: Cholesky, FFT, TriangularSolve

```
StableHLO:

module @jit_lax_conv_example {
   func.func public @main(%arg0: tensor<2x1x9x9xf32>, %arg1: tensor<1x1x4x4xf32>) ->
   (tensor<2x1x6x6xf32>) {
        %0 = stablehlo.convolution(%arg0, %arg1) : (tensor<2x1x9x9xf32>,
        tensor<1x1x4x4xf32>) -> tensor<2x1x6x6xf32>
        %1 = call @relu(%0) : (tensor<2x1x6x6xf32>) -> tensor<2x1x6x6xf32>
        return %1 : tensor<2x1x6x6xf32>
      }
   func.func private @relu(%arg0: tensor<2x1x6x6xf32>) -> tensor<2x1x6x6xf32> {
        %0 = stablehlo.constant dense<0.000000e+00> : tensor<f32>
        %1 = stablehlo.broadcast_in_dim %0, dims = [] : (tensor<f32>) ->
   tensor<2x1x6x6xf32>
        %2 = stablehlo.maximum %arg0, %1 : tensor<2x1x6x6xf32>
        return %2 : tensor<2x1x6x6xf32>
    }
}
```

```
Optimized HLO:
ENTRY main.10 {
    constant_3 = f32[1]{0} constant({0})
    Arg_1.2 = f32[1,1,4,4]{3,2,1,0} parameter(1)
    Arg_0.1 = f32[2,1,9,9]{3,2,1,0} parameter(0)
    onednn-conv-bias-activation.1 = (f32[2,1,6,6]{3,2,1,0}, u8[0]{0})
custom-call(Arg_0.1, Arg_1.2, constant_3), backend_config="{\"activation_mode\":\"2\"}"
-> conv+relu fusion
    ROOT get-tuple-element = f32[2,1,6,6]{3,2,1,0}
get-tuple-element(onednn-conv-bias-activation.1), index=0
}
```



#### PJRT Plugin for Intel GPU --- LLVM IR

# Python code: @jax.jit def func\_jit(a): a = jnp.abs(jnp.sqrt(x)) return a

```
module @jit_func {
   func.func public @main(%arg0:
   tensor<1024xf32> {jax.arg_info = "x", ...}) {
        %0 = stablehlo.sqrt %arg0 :
   tensor<1024xf32> loc(#loc2)
        %1 = stablehlo.abs %0 : tensor<1024xf32>
   loc(#loc3)
        return %1 : tensor<1024xf32> loc(#loc)
      } loc(#loc)
} loc(#loc)
```



```
### Missed_computation (param_0.1: f32[1024]) -> f32[1024] {
    %param_0.1 = f32[1024]{0} parameter(0)
    %sqrt.0 = f32[1024]{0} sqrt(f32[1024]{0} %param_0.1),
    metadata={op_type="Sqrt" ...}
    ROOT %abs.0 = f32[1024]{0} abs(f32[1024]{0} %sqrt.0),
    metadata={op_type="Abs" ...}
}
ENTRY %func.8 (arg0.1: f32[1024])->f32[1024] {
    %arg0.1 = f32[1024]{0} parameter(0), ...
    ROOT %fusion = f32[1024]{0} fusion(f32[1024]{0} %arg0.1),
    kind=kLoop, calls=%fused_computation,
}
```

#### Lmhlo module:

```
module attributes {hlo.unique_id = 0 : i32, mhlo.unique_id = 0 : i64} {
 func @func(%arg0: memref<4096xi8> {lmhlo.params = 0 : index}, %arg1:
memref<4096xi8> {lmhlo.output index = dense<> : tensor<0xi64>})
attributes {result_xla_shape = "f32[1024]{0}"} {
   %c0 = arith.constant 0 : index
   %0 = memref.view %arg0[%c0][] : memref<4096xi8> to memref<1024xf32>
   %c0 0 = arith.constant 0 : index
   %1 = memref.view %arg1[%c0 0][] : memref<4096xi8> to
memref<1024xf32>
   "lmhlo.fusion"() ({
     %2 = bufferization.to tensor %0 : memref<1024xf32>
     %3 = "mhlo.sqrt"(%2) : (tensor<1024xf32>) -> tensor<1024xf32>
     %4 = "mhlo.abs"(%3) : (tensor<1024xf32>) -> tensor<1024xf32>
     memref.tensor_store %4, %1 : memref<1024xf32>
     "lmhlo.terminator"(): () -> ()
   }) : () -> ()
    "lmhlo.terminator"(): () -> ()
```

#### PJRT Plugin for Intel GPU --- LLVM IR

#### Difference with NVVM:

- Target data layout and triple
- Address space
- SPIRV builtin function
  - get\_global\_id,...
  - Subgroup shuffle, barrier
  - Math function: sqrt, expm

Address Space	NVPTX SPIR-V		
	Memory Space	Memory Space	
0	Generic	Private	
1	Global	Global	
2	*Internal Use	Constant	
3	Shared	Workgroup	
4	Constant Generic		
5	Local		

```
LLVM IR:
target datalayout = "e-p:64:64:64-i1:8:8-i8:8:8-xxxxx"
target triple = "spir64-unknown-unknown"
define spir func void @fusion(i8 addrspace(1)* noalias nocapture
readonly align 16 dereferenceable(4096) %alloc0, i8 addrspace(1)*
noalias nocapture writeonly align 128 dereferenceable(4096)
%alloc1) local unnamed addr !intel reqd sub group size !1 {
entry:
  %0 = call i64 @ Z12get group idj(i32 0)
 %block id = trunc i64 %0 to i32
 %1 = call i64 @ Z12get local idj(i32 0)
  %thread id x = trunc i64 \%1 to i32
  %2 = shl nuw nsw i32 %block id, 10
  %linear index = add nuw nsw i32 %2, %thread id x
  %3 = bitcast i8 addrspace(1)* %alloc0 to float addrspace(1)*
  %4 = zext i32 %linear index to i64
  %5 = getelementptr inbounds float, float addrspace(1)* %3, i64 %4
  %6 = load float, float addrspace(1)* %5, align 4, !invariant.load
!2
 %7 = call float @ Z4sqrtf(float %6)
 %8 = call float @llvm.fabs.f32(float %7)
 %9 = bitcast i8 addrspace(1)* %alloc1 to float addrspace(1)*
 %10 = getelementptr inbounds float, float addrspace(1)* %9, i64
  store float %8, float addrspace(1)* %10, align 4
  ret void
declare spir func float @ Z4sqrtf(float) local unnamed addr #0
```



Latency (s)

#### Flax/JAX Stable Diffusion

https://huggingface.co/CompVis/stable-diffusion-v1-4#jaxflax No code change is required for Intel GPU

```
import jax, sys, time
import numpy as np
from flax.jax utils import replicate
from flax.training.common utils import shard
from diffusers import FlaxStableDiffusionPipeline
scheduler, scheduler state =
FlaxDPMSolverMultistepScheduler.from pretrained("CompVis/stable-diffusion-v1-4",
subfolder="scheduler")
pipeline, params = FlaxStableDiffusionPipeline.from pretrained("CompVis/stable-diffusion-v1-4",
scheduler=scheduler, revision="bf16", dtype=jax.numpy.bfloat16)
params["scheduler"] = scheduler state
prompt = "a photo of an astronaut riding a horse on mars"
prng seed = jax.random.PRNGKey(0)
prompt = jax.device count() * [prompt]
prompt_ids = pipeline.prepare_inputs(prompt)
params = replicate(params)
prng_seed = jax.random.split(prng_seed, jax.device_count())
prompt ids = shard(prompt ids)
def elapsed_time(nb_pass=10, num_inference_steps=20):
  # warmup
 images = pipeline(prompt_ids, params, prng_seed, num_inference_steps, jit=True).images
  start = time.time()
  for in range(nb pass):
    _ = pipeline(prompt_ids, params, prng_seed, num_inference_steps, jit=True).images
  end = time.time()
  return (end - start) / nb pass
print("Latency per image is: {:.3f}s".format(elapsed time(nb pass=5, num inference steps=20)))
```

\$ export LD\_LIBRARY\_PATH="python-path/jaxlib/:\$LD\_LIBRARY\_PATH" \$ export PJRT\_NAMES\_AND\_LIBRARY\_PATHS="xpu:/path/libitex\_xla\_extension.so" \$ numactl -N 0 -m 0 python jax\_stable.py

Latency per image is: 0.79s on Intel® Data Center Max GPU 1550

**Diffusion Steps** 

**Precision** 

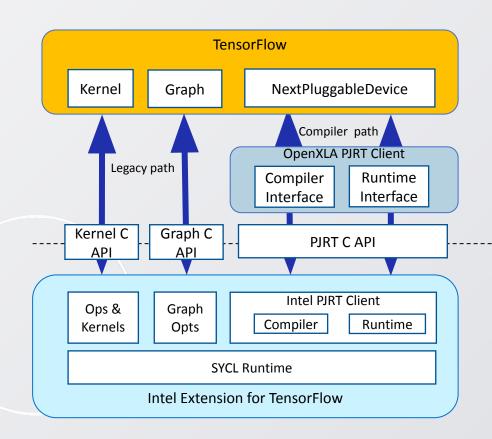
Model

stable-diffusion-v 1-4	BF16	20	0.79	
		BF16	50	1.84
<b>③</b> 10.112.109.52.8005	x +			v - o x
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### NextPluggableDevice

- TensorFlow supports mixed execution mode
  - Run single TF model with both traditional and OpenXLA runtime
- Problems for TensorFlow plugins
  - PluggableDevice is StreamExecutor based, while OpenXLA is PJRT based
  - "NO" interoperation between them
- NextPluggableDevice solves this issue by extending PluggableDevice to use unified PJRT runtime for both





#### **Summary**

- PJRT simplifies ML Hardware and Framework integration with unified API to support all frameworks (TensorFlow, JAX, PyTorch via PyTorch-XLA)
- Intel GPU plugin integrated with JAX via PJRT API using oneAPI and LLVM/ SPIR-V and demonstrates good performance on Intel® Data Center Max GPU

## Questions