CMPE-630 Digital IC Design
Laboratory Exercise 7

Autolayout Design Techniques (HDL-Layout)

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Andrew Fountain
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By submitting this report, you attest that you neither have given nor have received any assistance (including writing, collecting data, plotting figures, tables or graphs, or using previous student reports as a reference), and you further acknowledge that giving or receiving such assistance will result in a failing grade for this course.

Your Signature: _____

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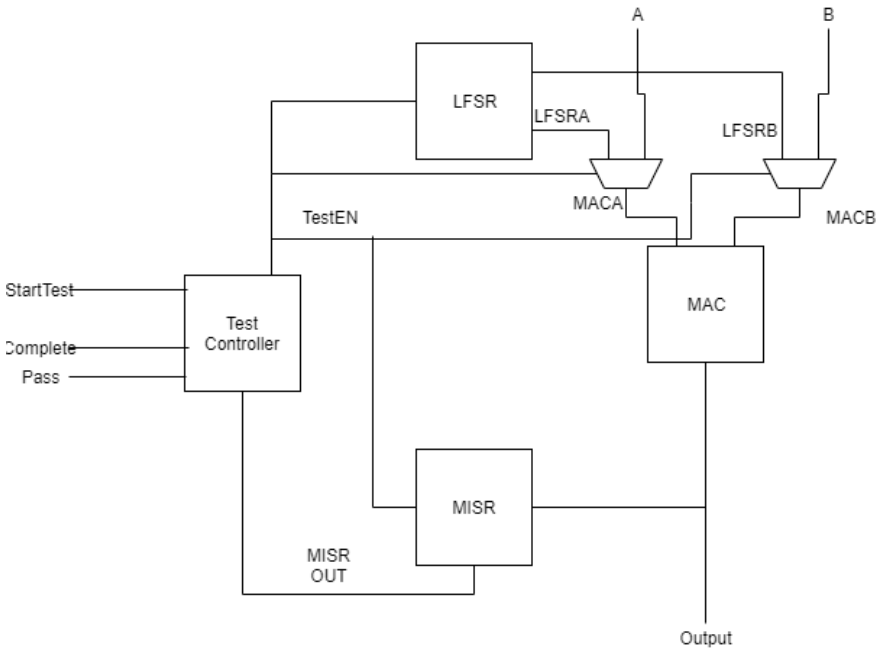


Figure 1: **Figure 1:** High Level Block Diagram of the MAC with BIST.

1 Abstract

Integrated Circuit Design is a costly and complex endeavor. Fortunately, automatic tools speed up the process and allow designs that are not possible to create manually. This exercise implemented a 1-Bit ALU and a 16-Bit ALU using autolayout. The autolayout tools generated very reasonable circuits. The 1-Bit ALU has an input frequency of 380.92MHz and a throughput frequency of 553.4MHz, while the 16-bit ALU has an input frequency of 461.02MHz and a throughput frequency of 110.2MHz. The area used by the ALUs was also reasonable with the 1-bit ALU taking up $647.89\mu m^2$ and the 16-bit ALU occupying $9792.5\mu m^2$.

2 Design Methodology and Theory

A cornerstone of IC design is the ability to create large, complex designs from smaller more manageable parts. The project outlined in this exercise calls for the design, testing and layout of a multiply and accumulate (MAC) unit, which takes two 16-bit inputs, multiplies them together, adds them to the value stored in a register, and then stores that output back into the register. The final component should contain a built in self test (BIST) that verifies the functionality of the MAC.

The MAC is composed of a carry-save multiplier, ripple carry full-adder, and parallel register. The BIST is implemented through the use of an LFSR for the inputs, an MISR for the output, and a test controller which controls the timing and sets the test passed and test complete outputs. A full diagram of the MAC with BIST can be seen below in *Figure 1.*

3 Results and Analysis

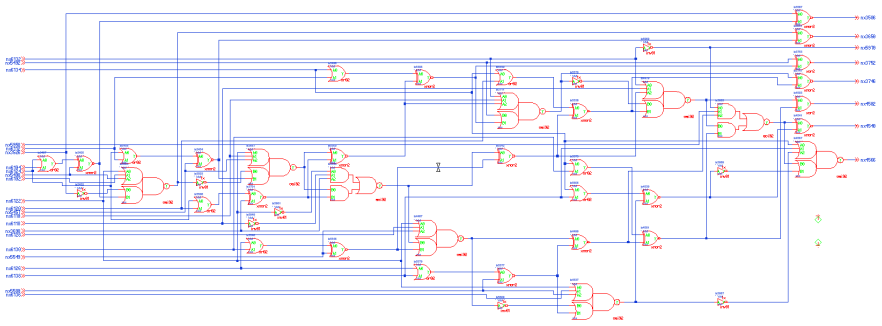


Figure 2: Full Schematic Page 7

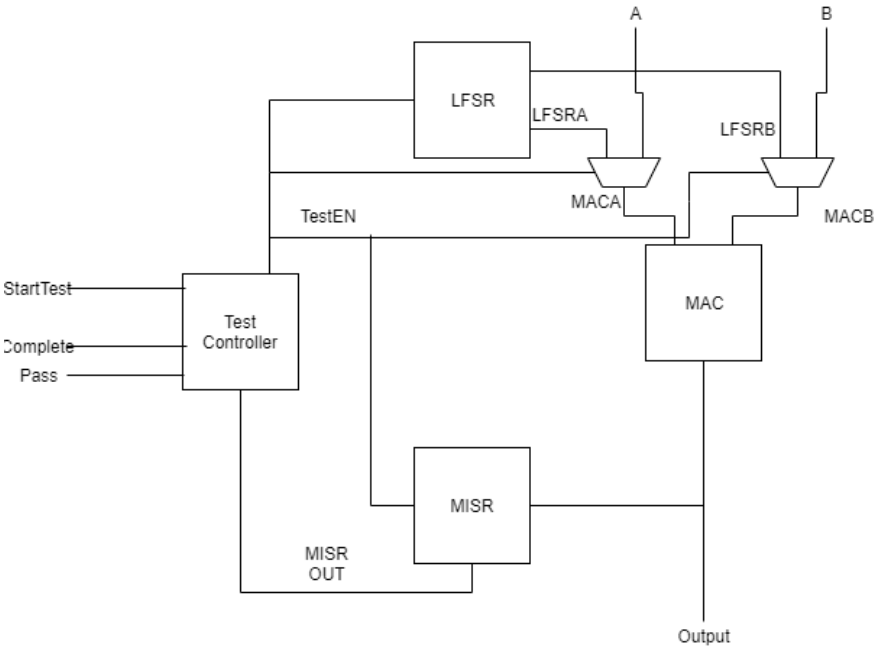


Figure 3: Full Project Block

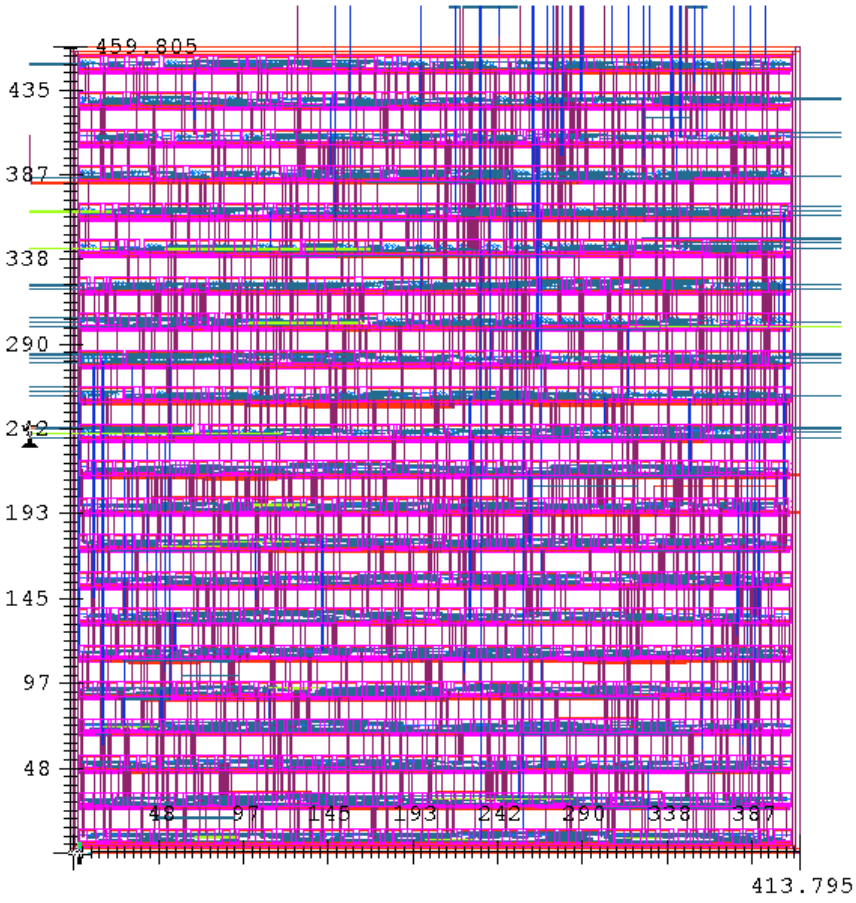
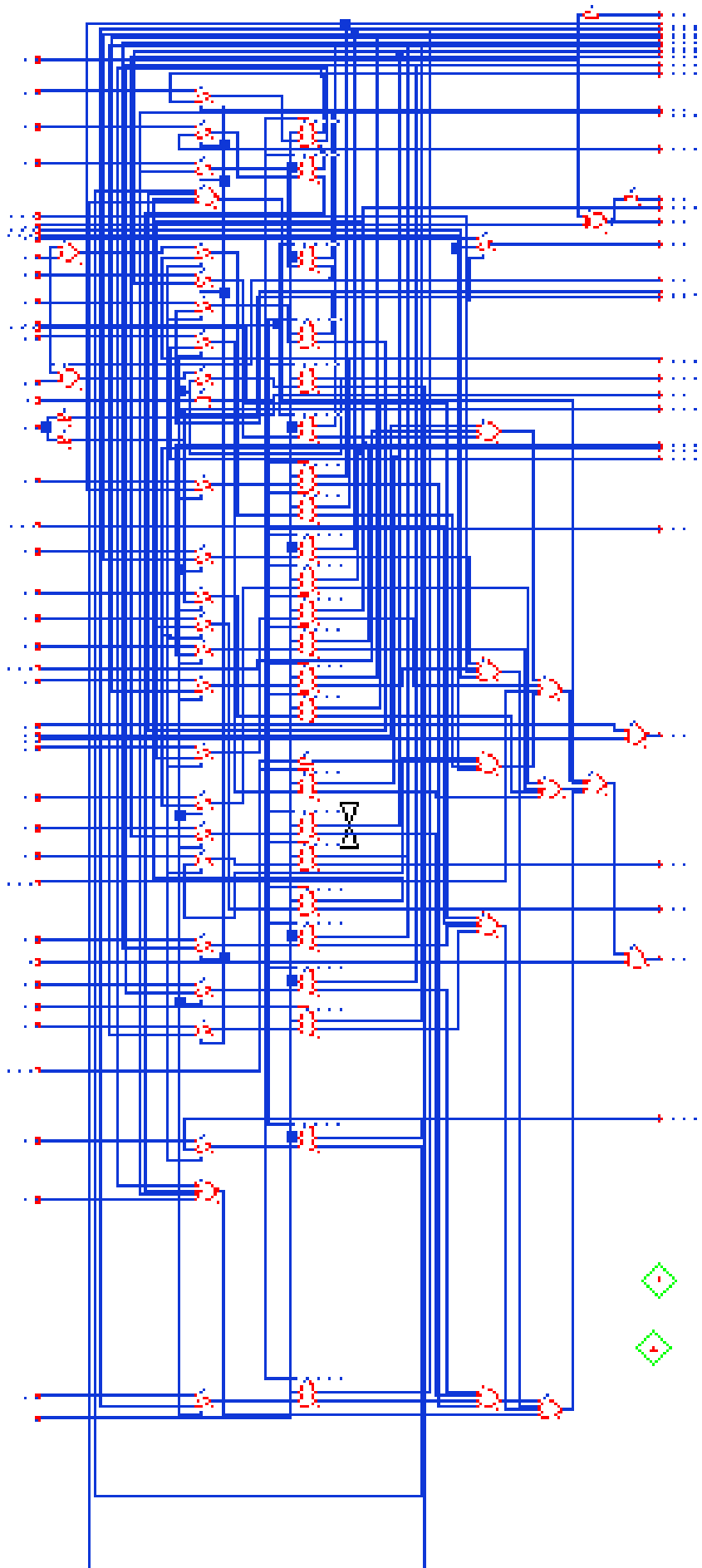
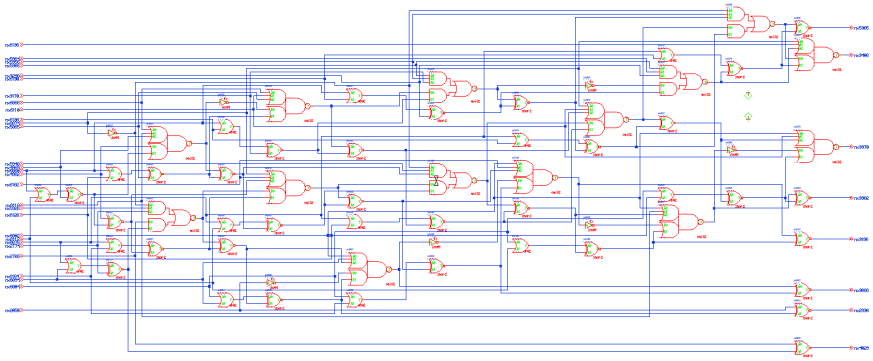


Figure 4: Full Layout





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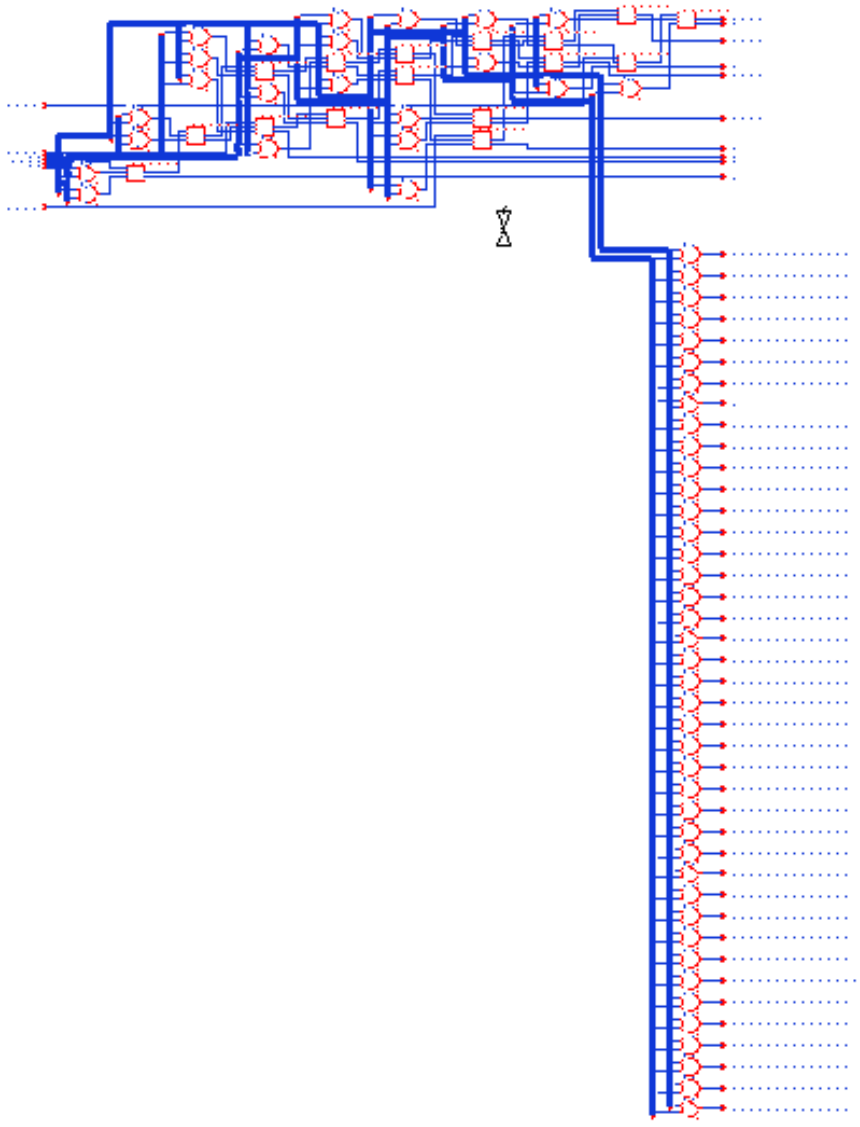

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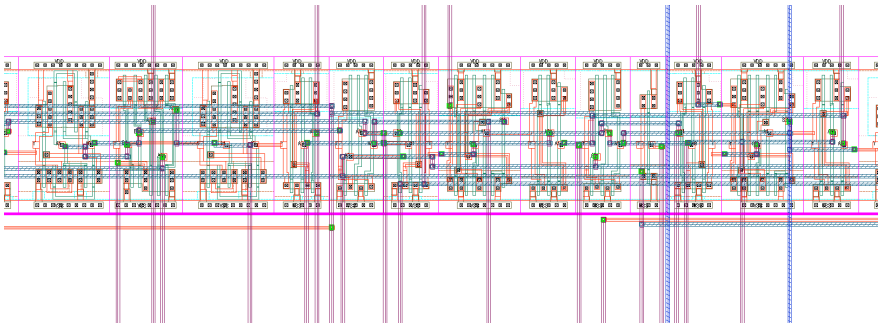
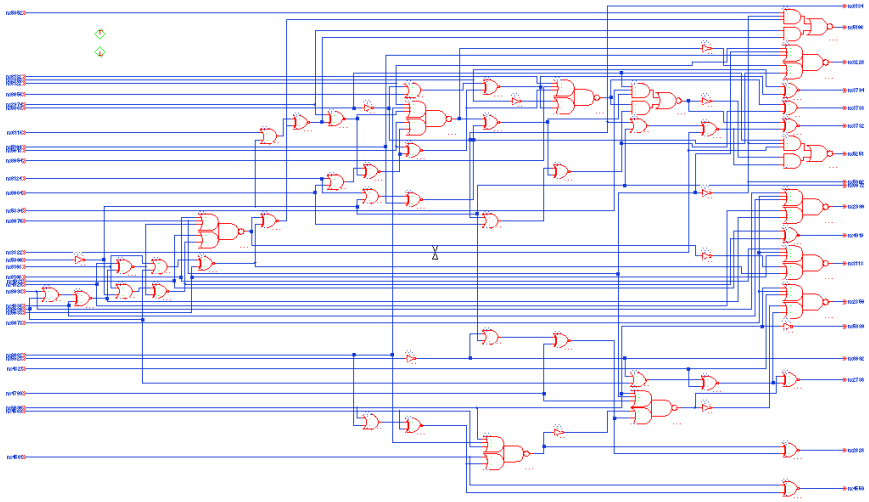


Figure 8: Full Layout Close Up View

Figure 9: BIST Test Bench



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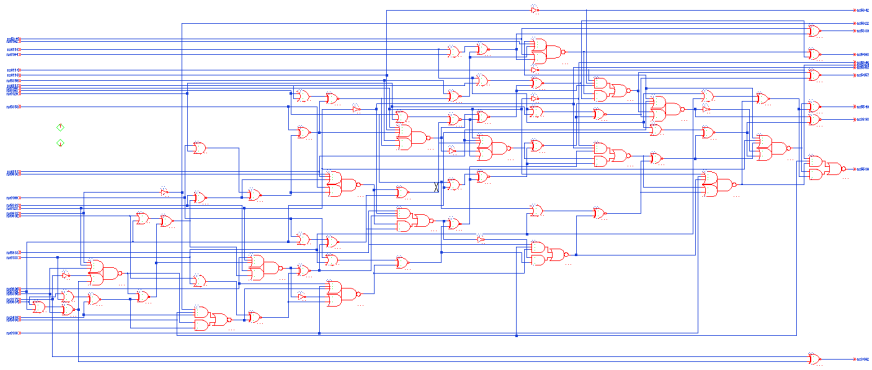

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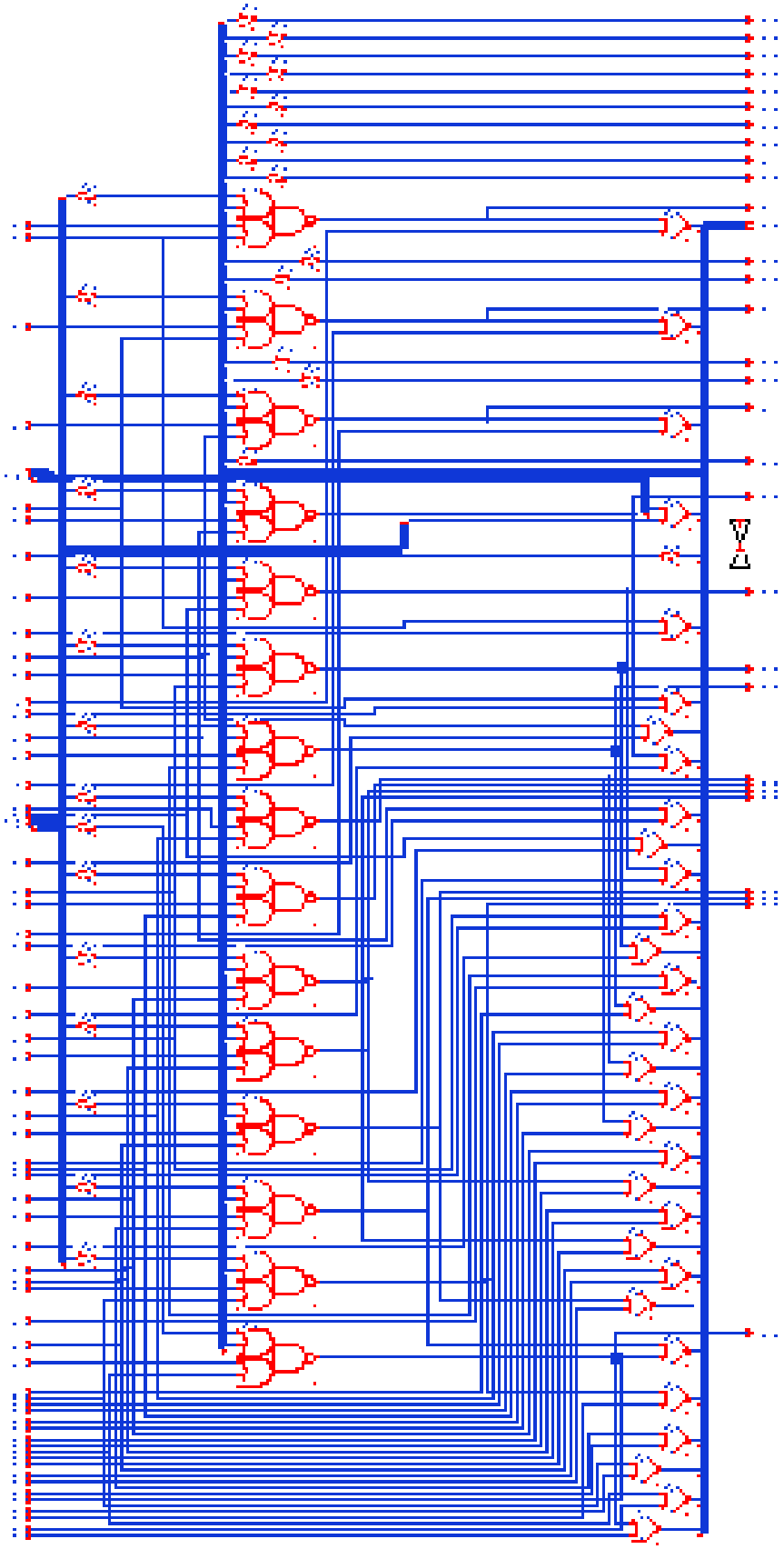
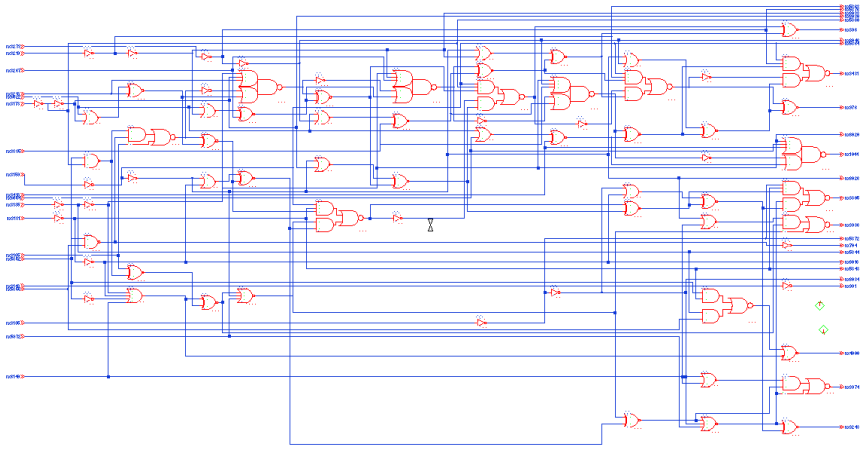


Figure 12: nBitAdder Schematic Page 1



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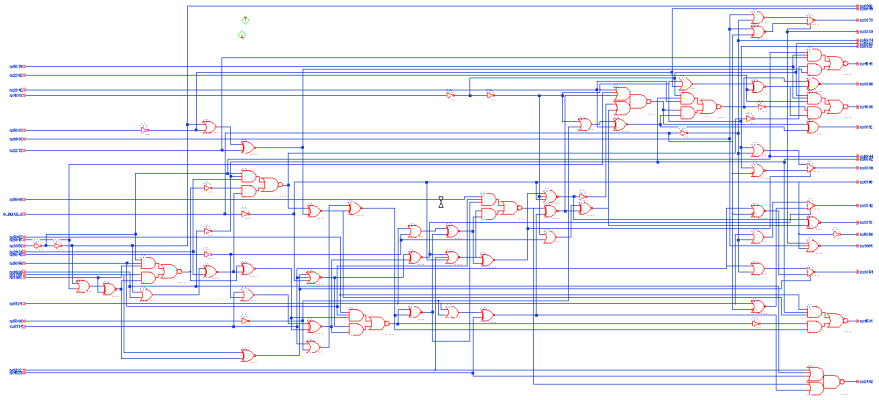

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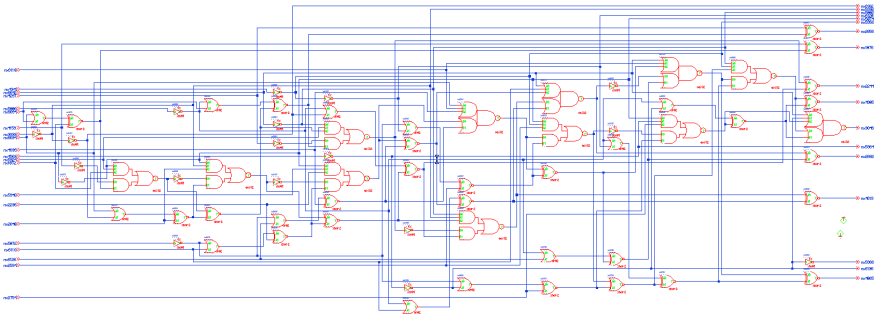

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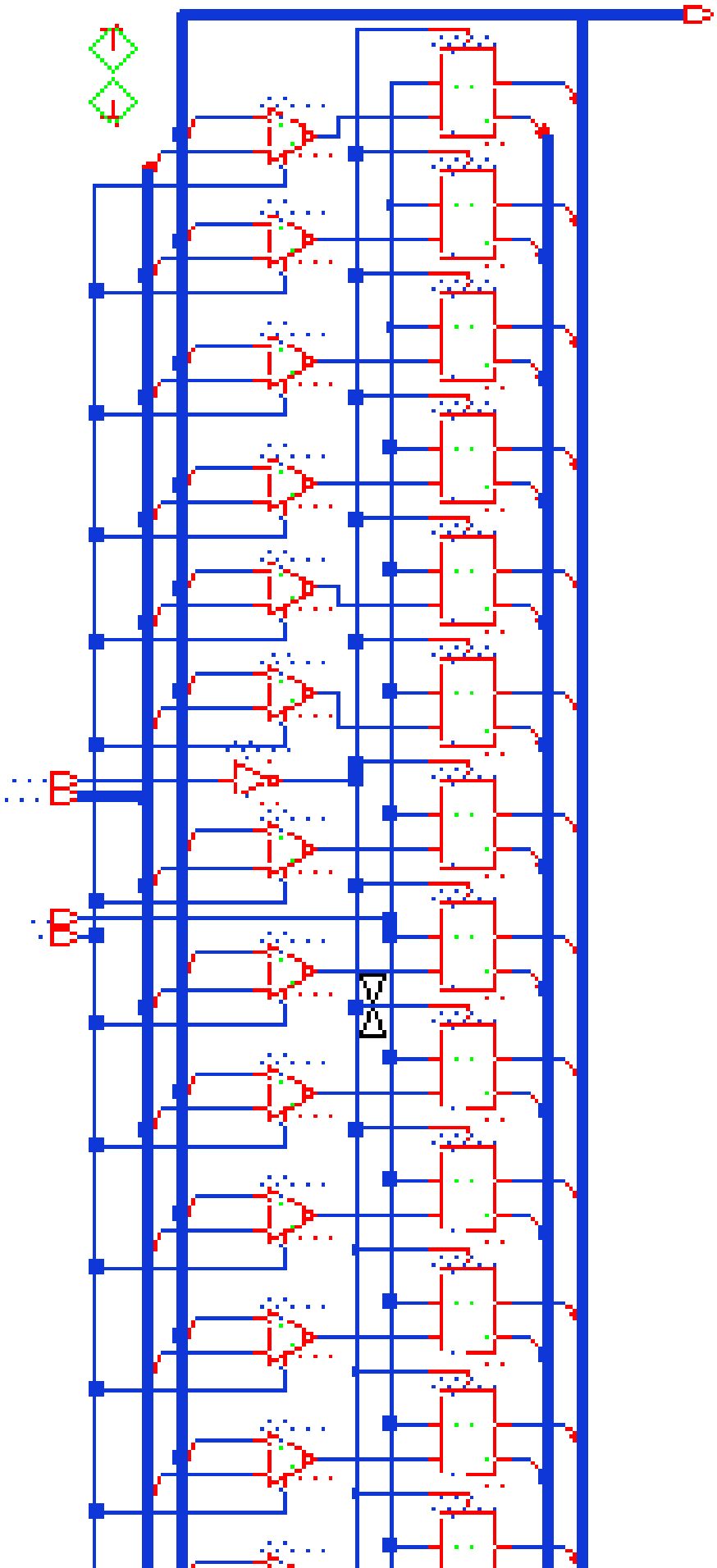
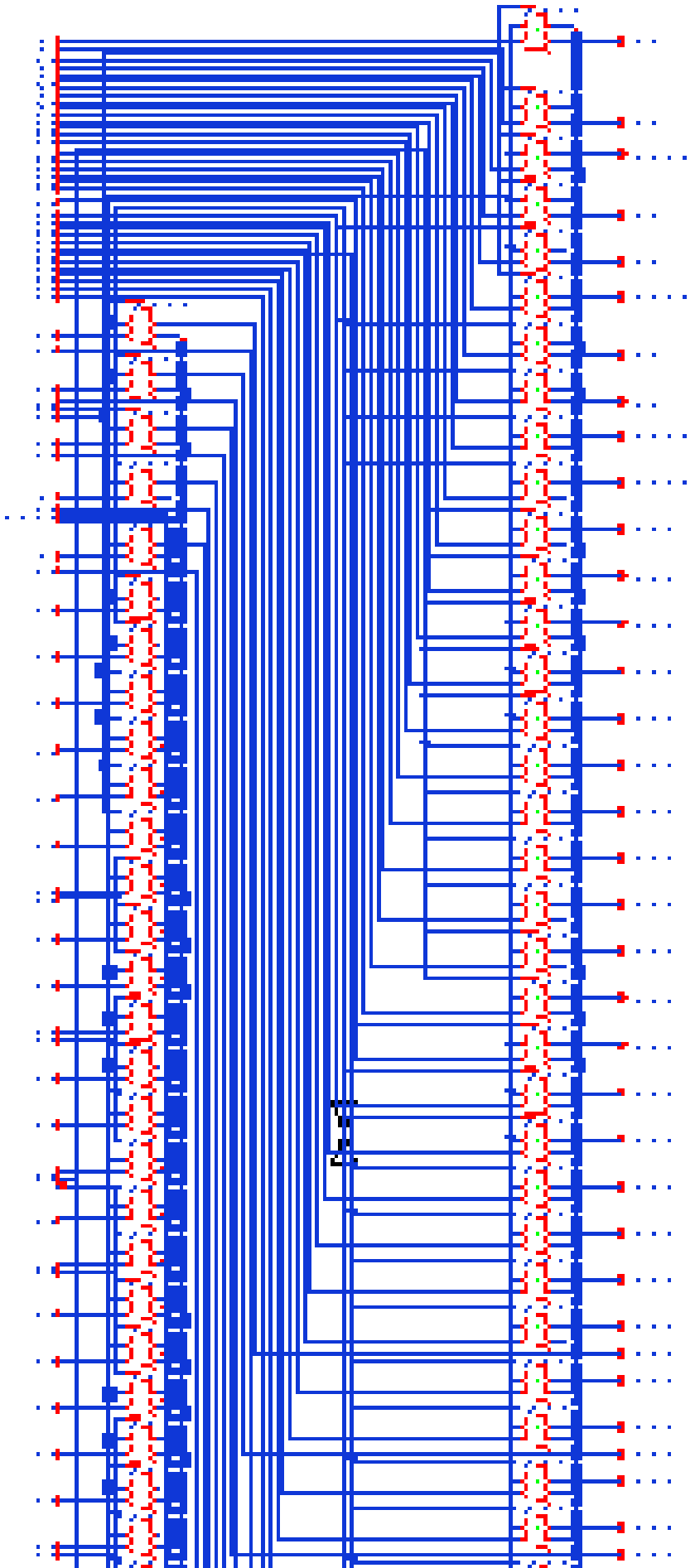
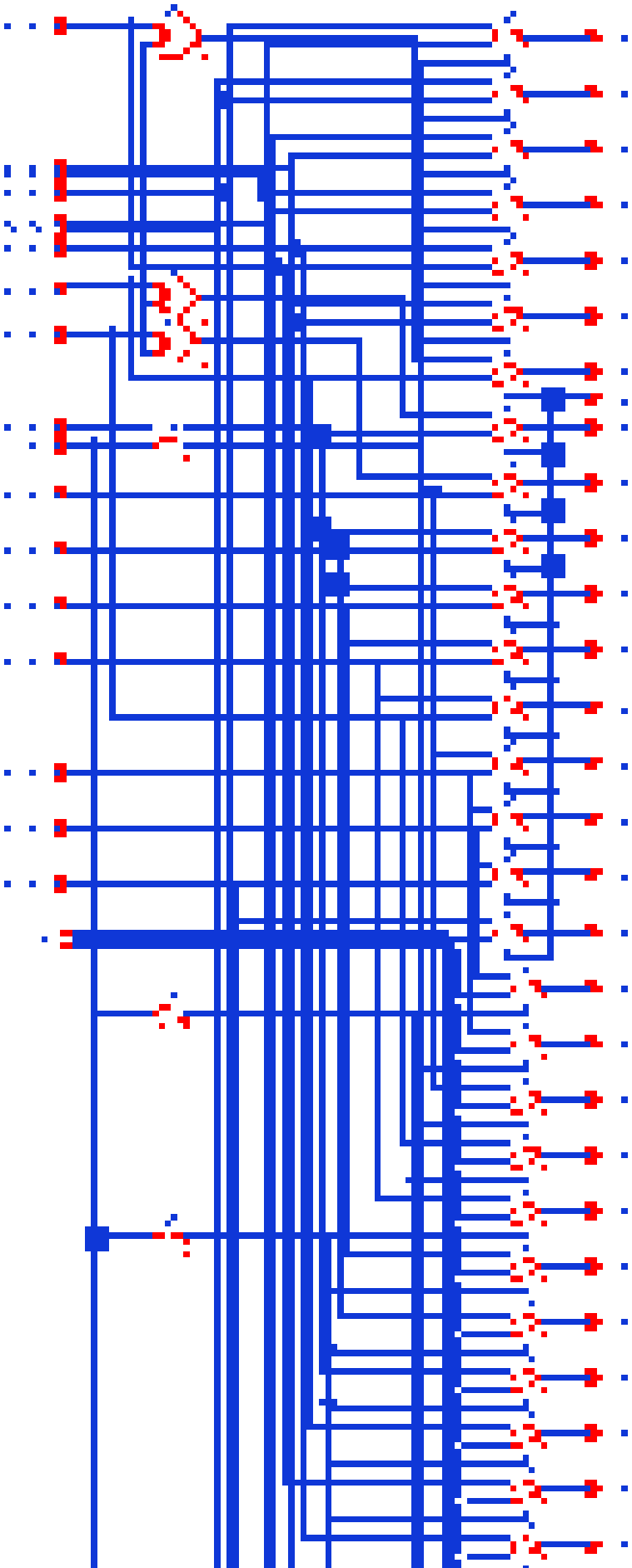






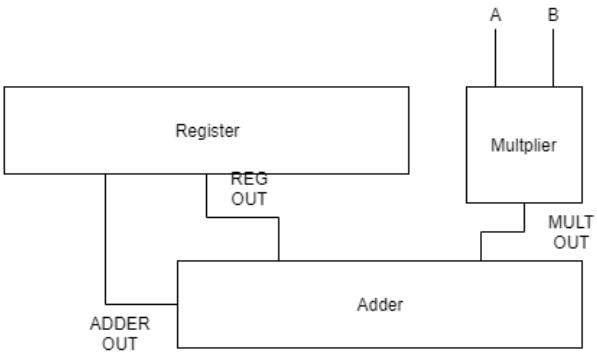
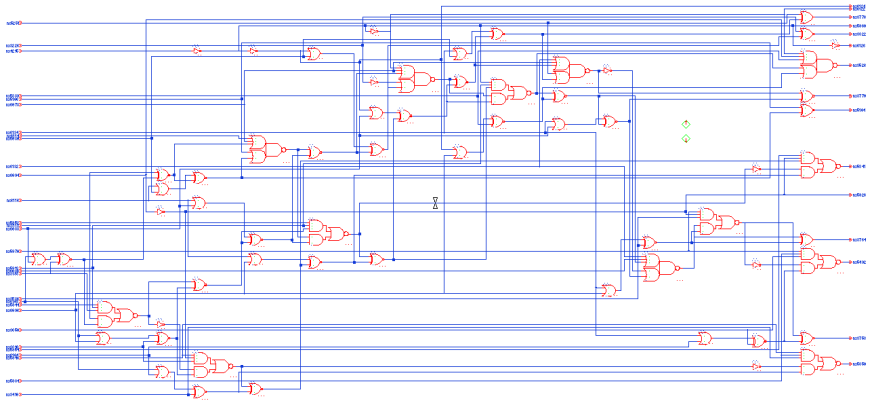


Figure 19: MAC block



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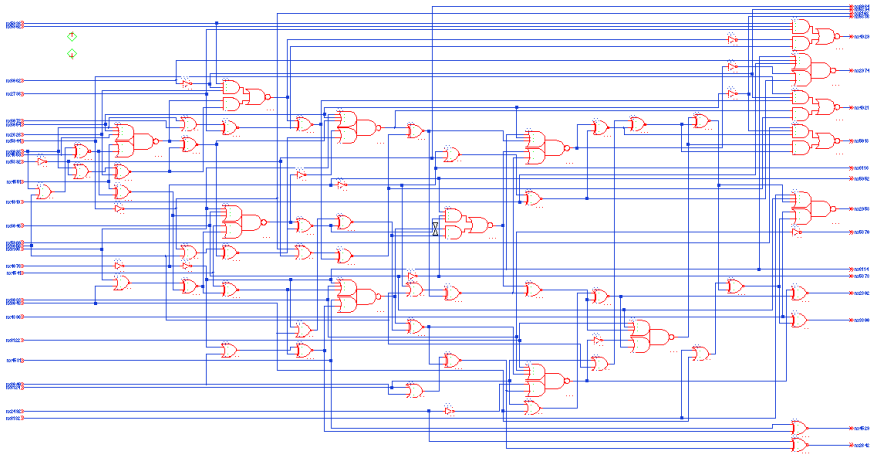

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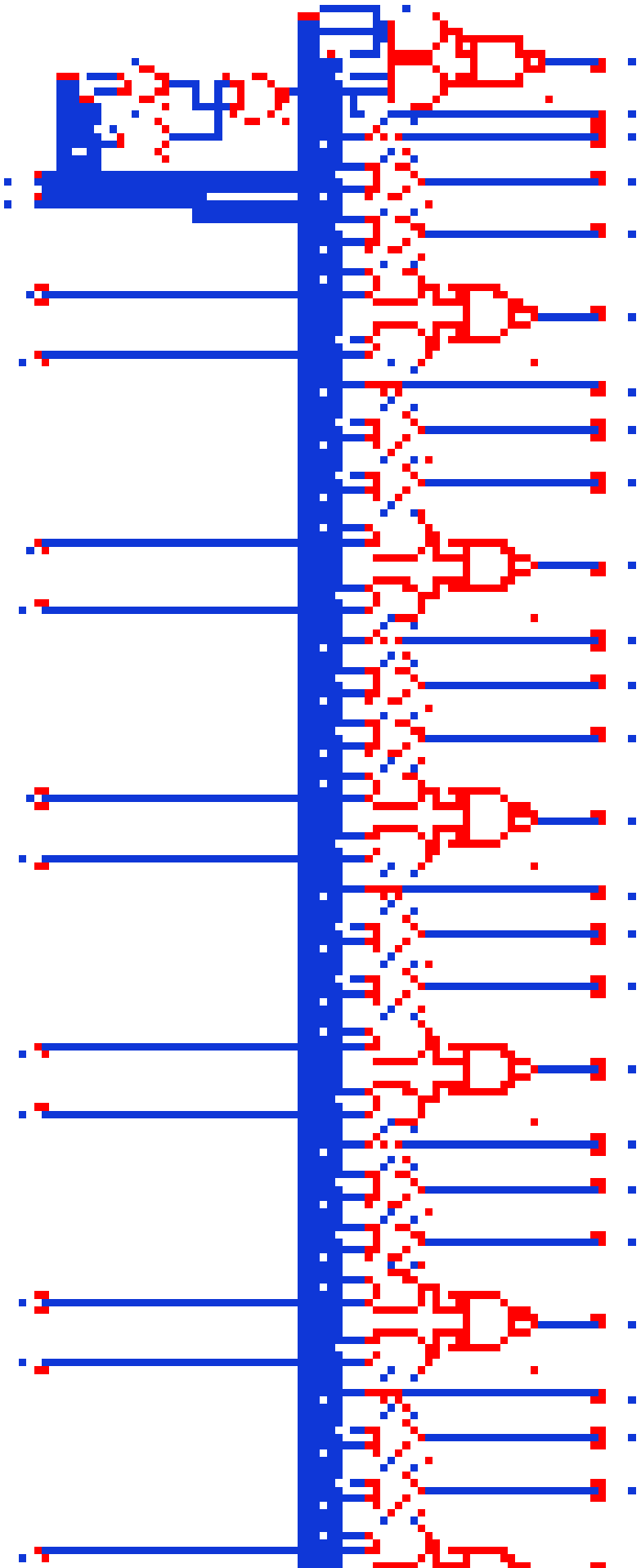

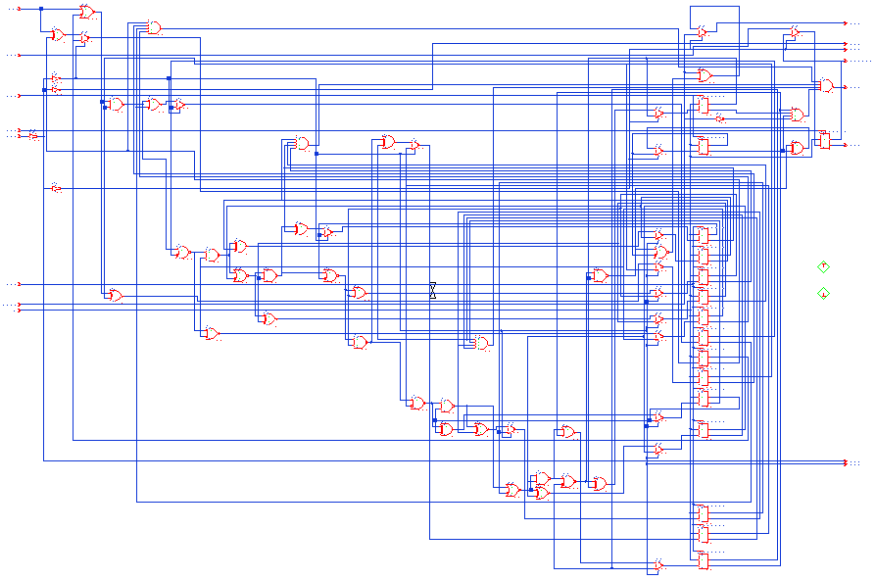

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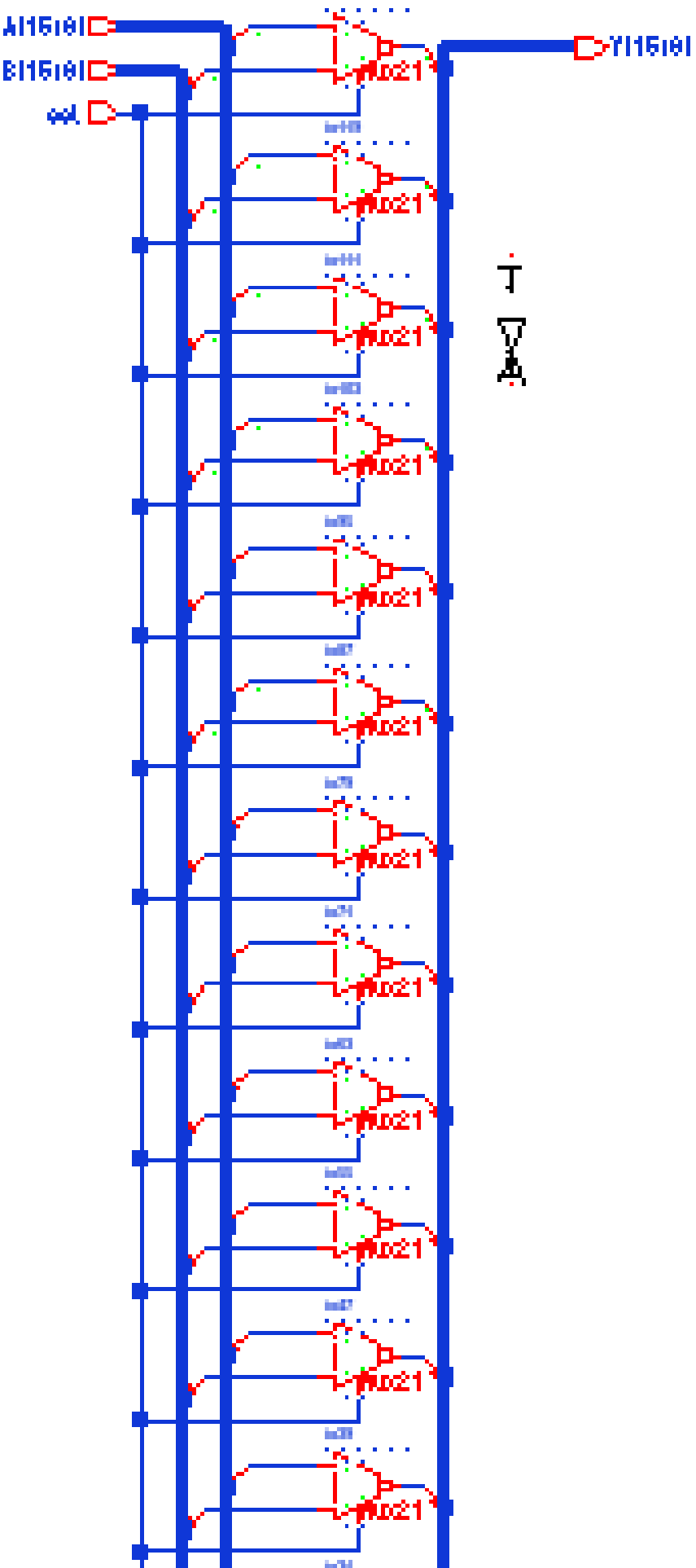

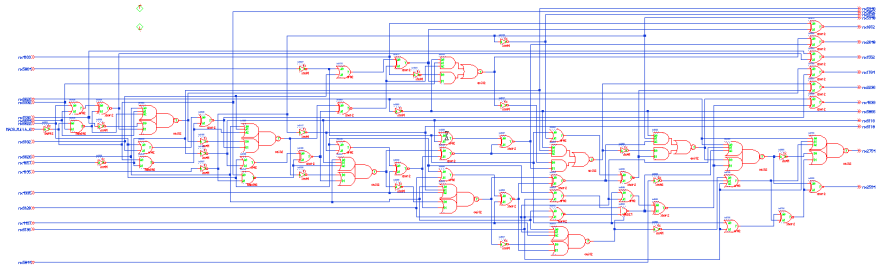

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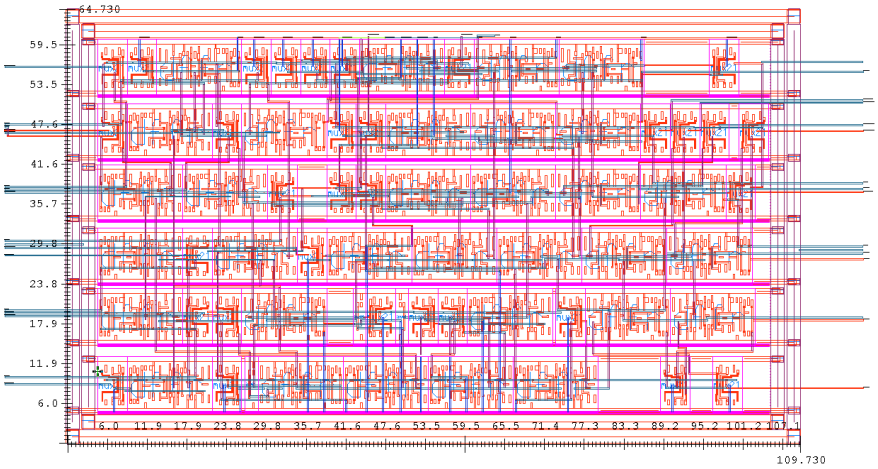
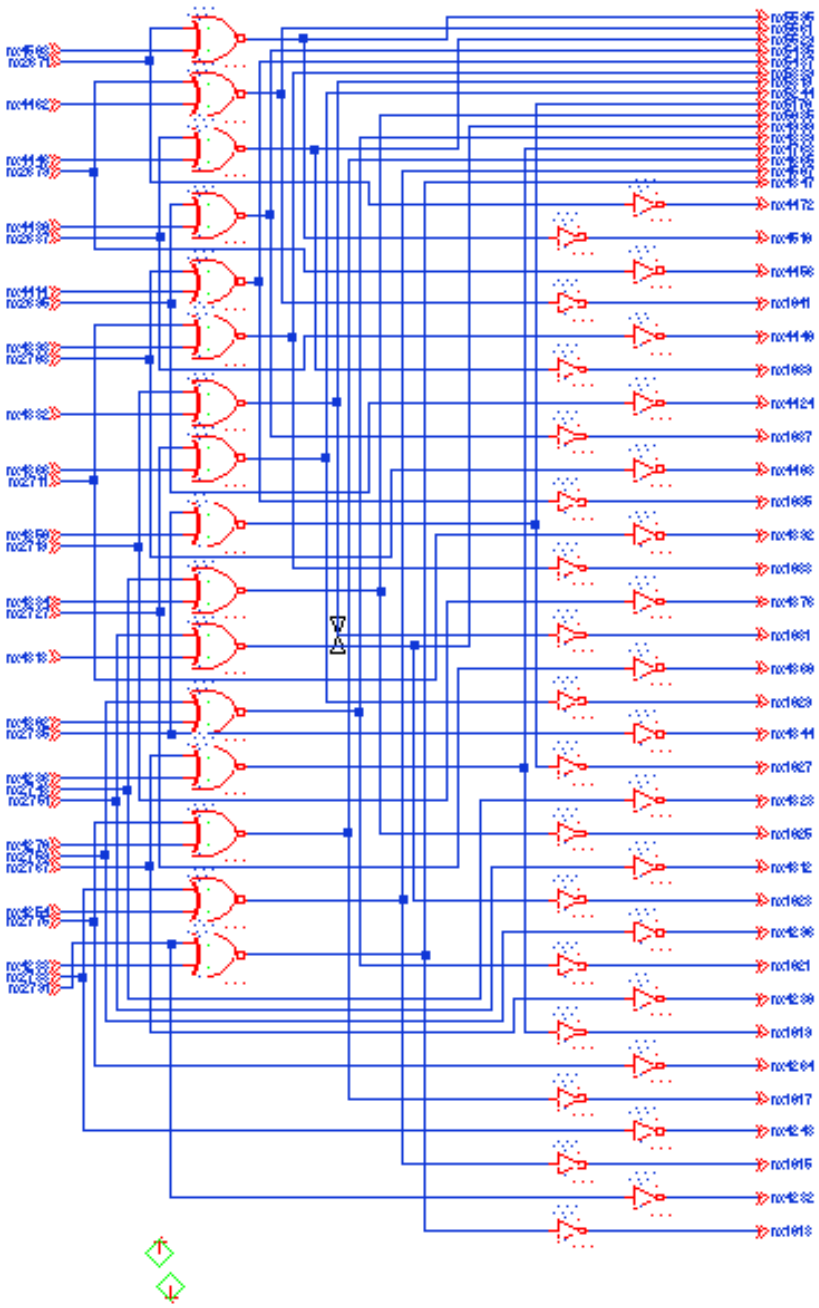


Figure 26: nBitRegister 32 Bit Layout



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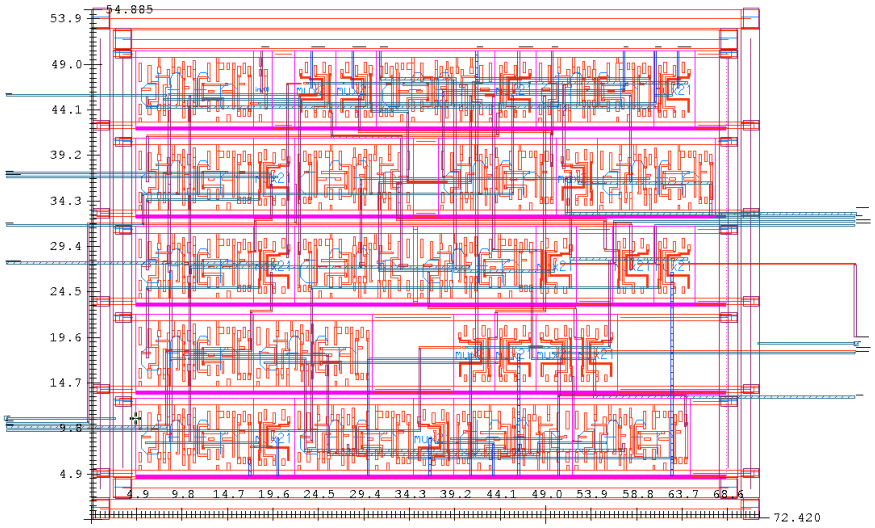
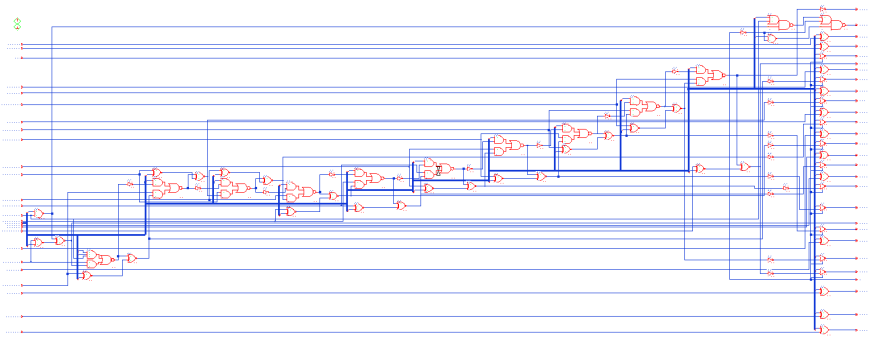


Figure 28: nBitRegister 16 Bit Layout



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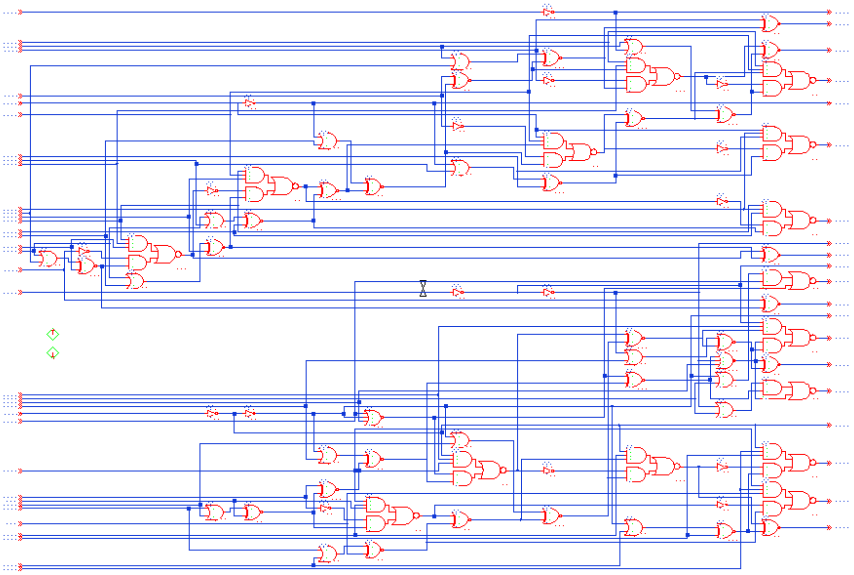

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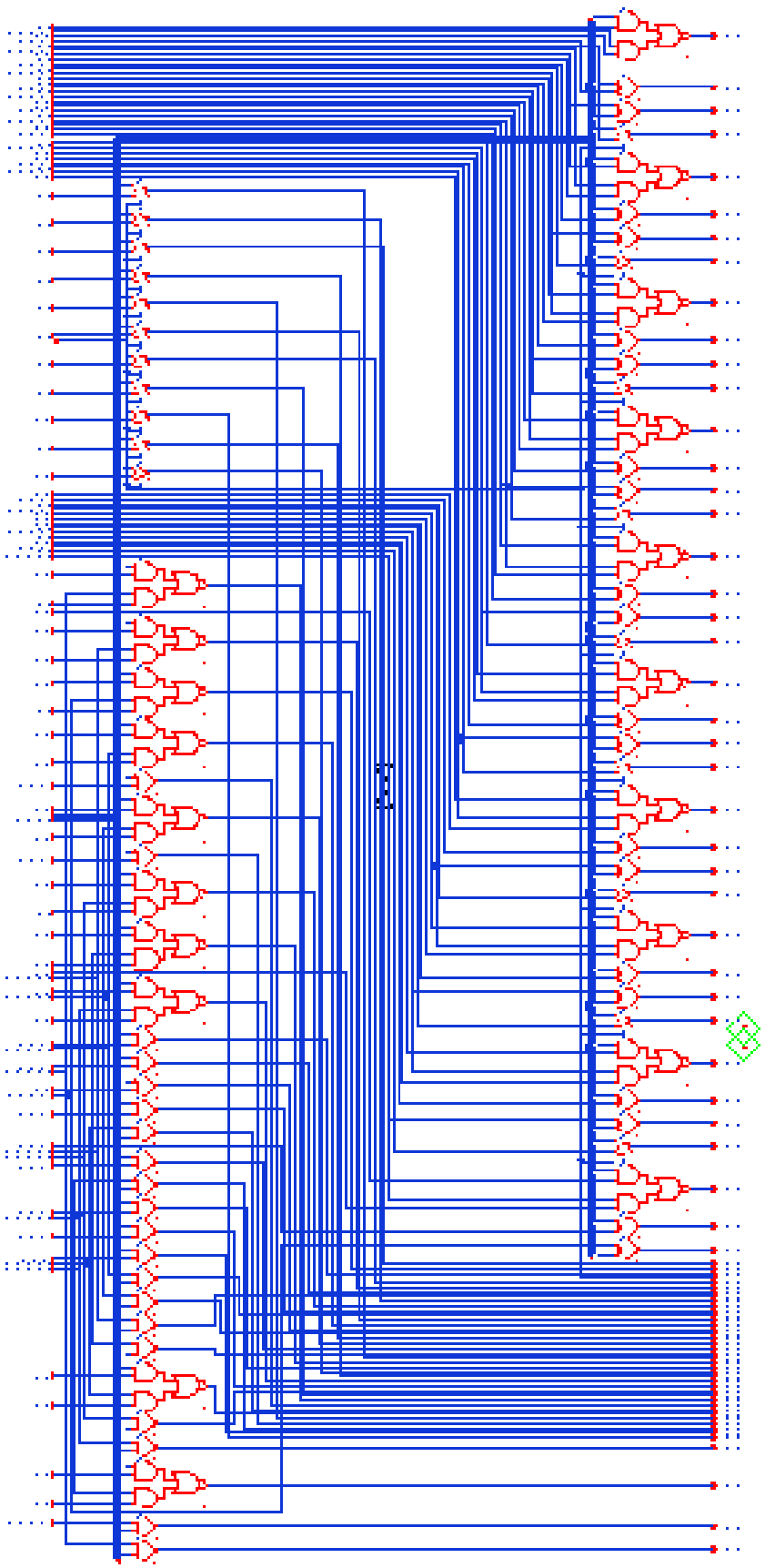

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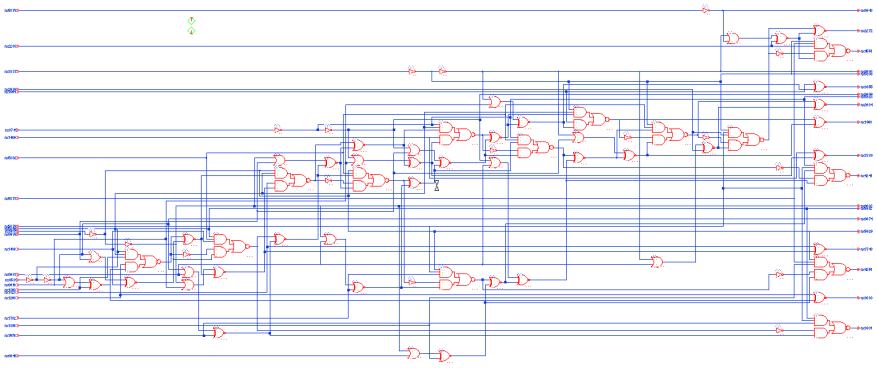

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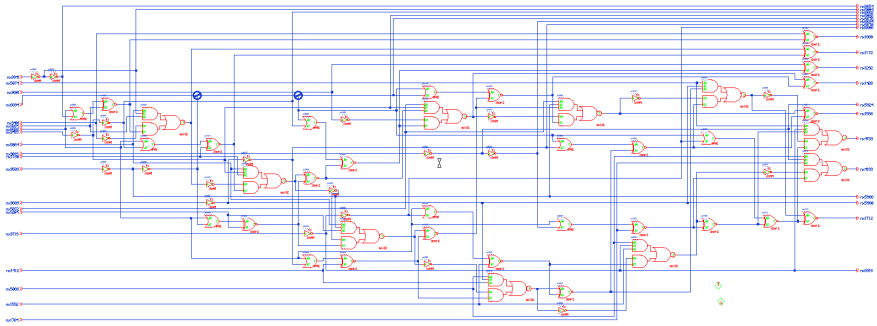

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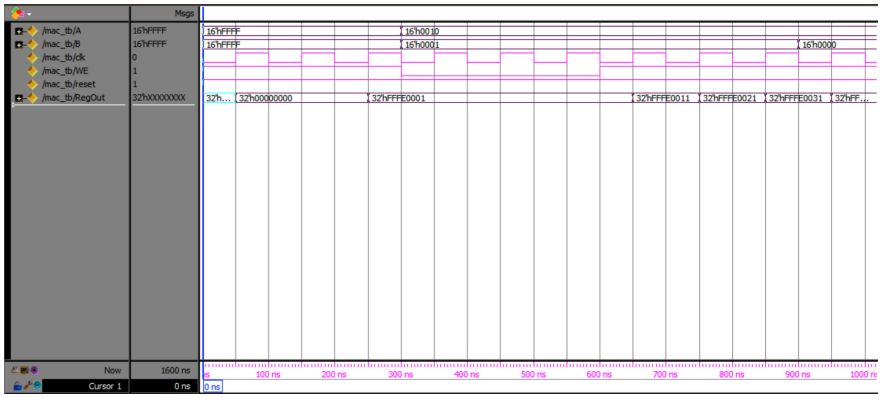
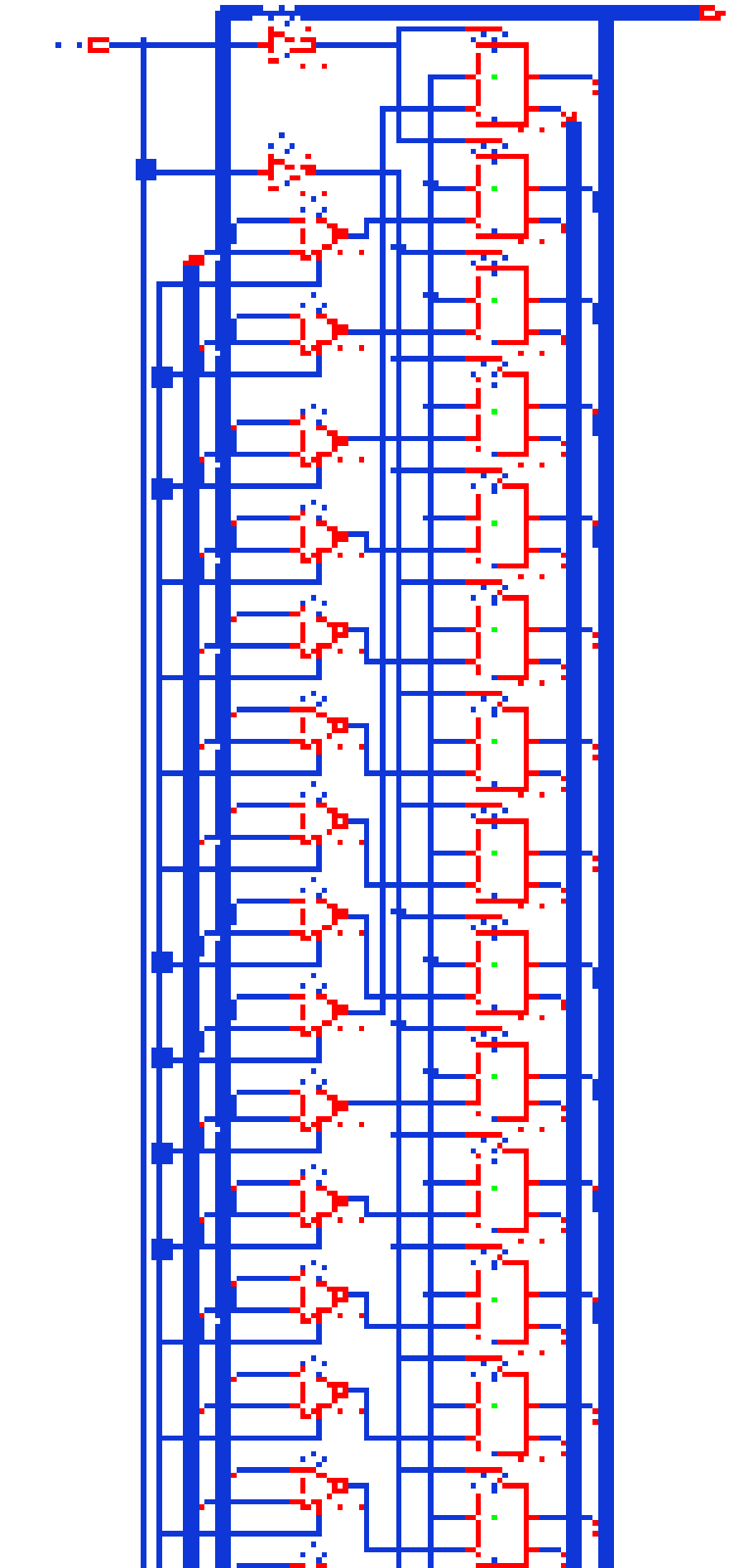
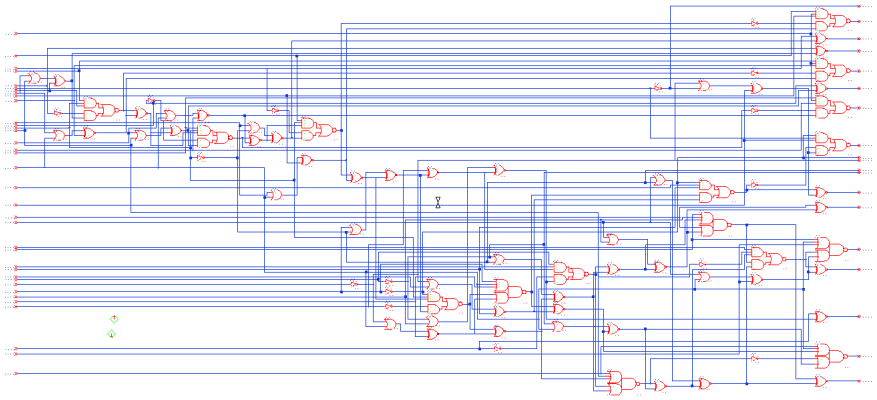


Figure 34: MAC 16bit Test Bench





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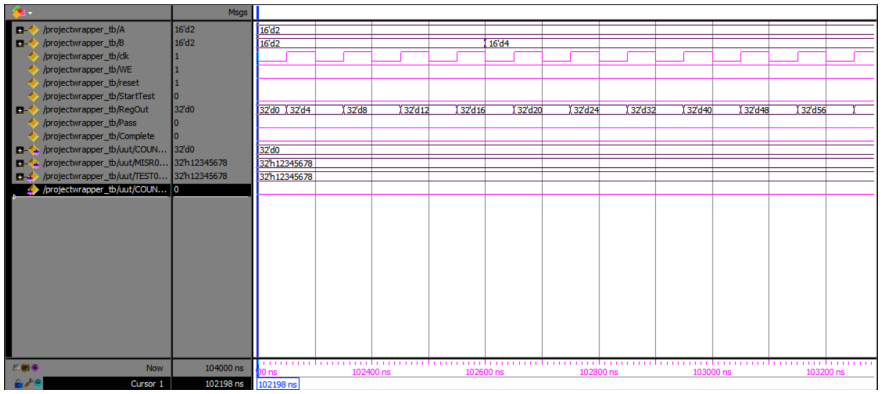
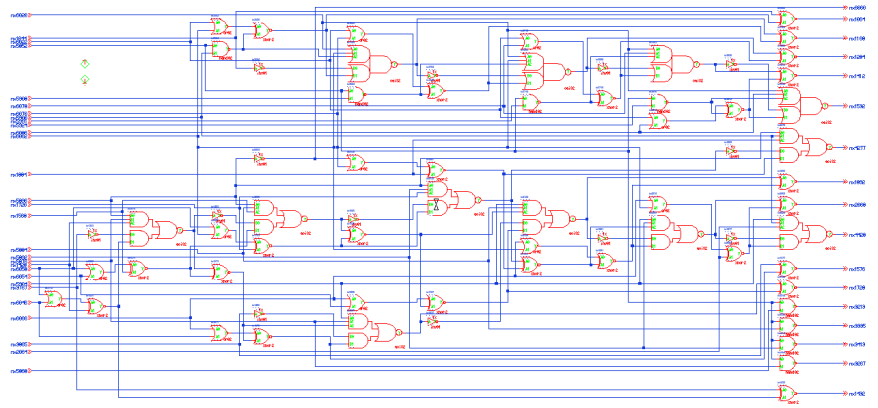


Figure 37: MAC Test Bench



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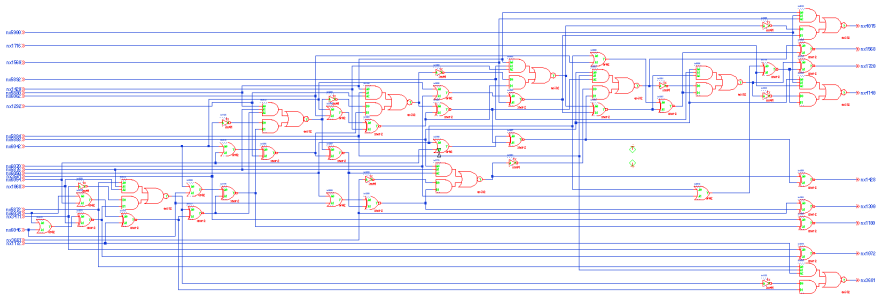

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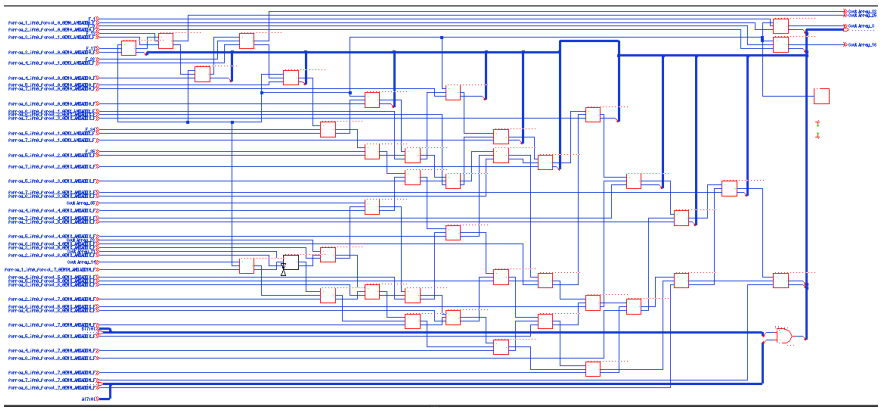
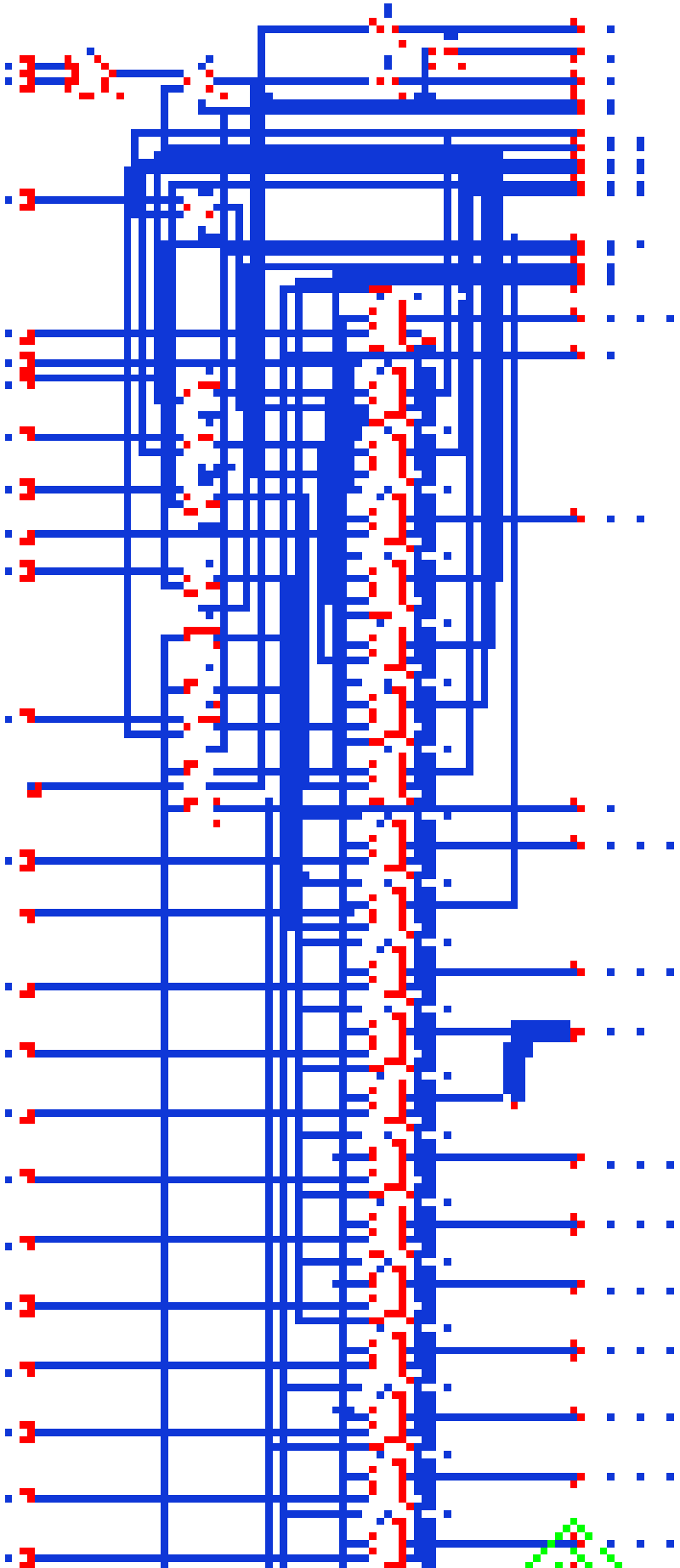
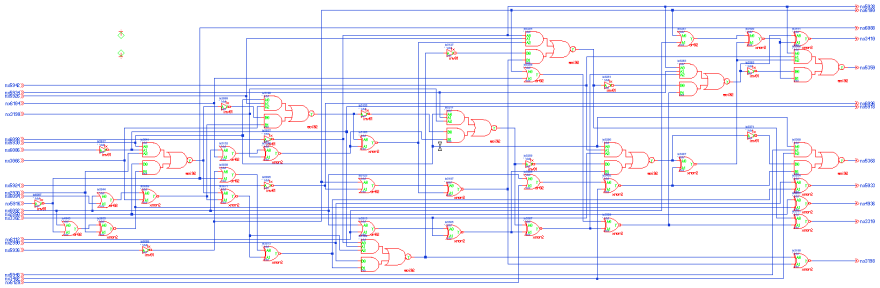


Figure 40: Multiplier Schematic Page 1





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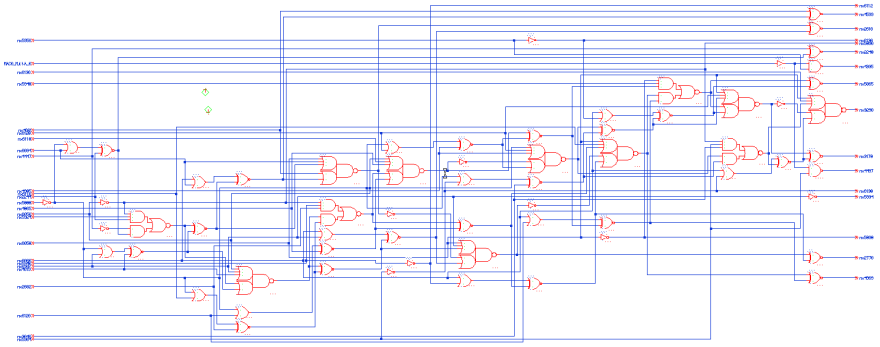

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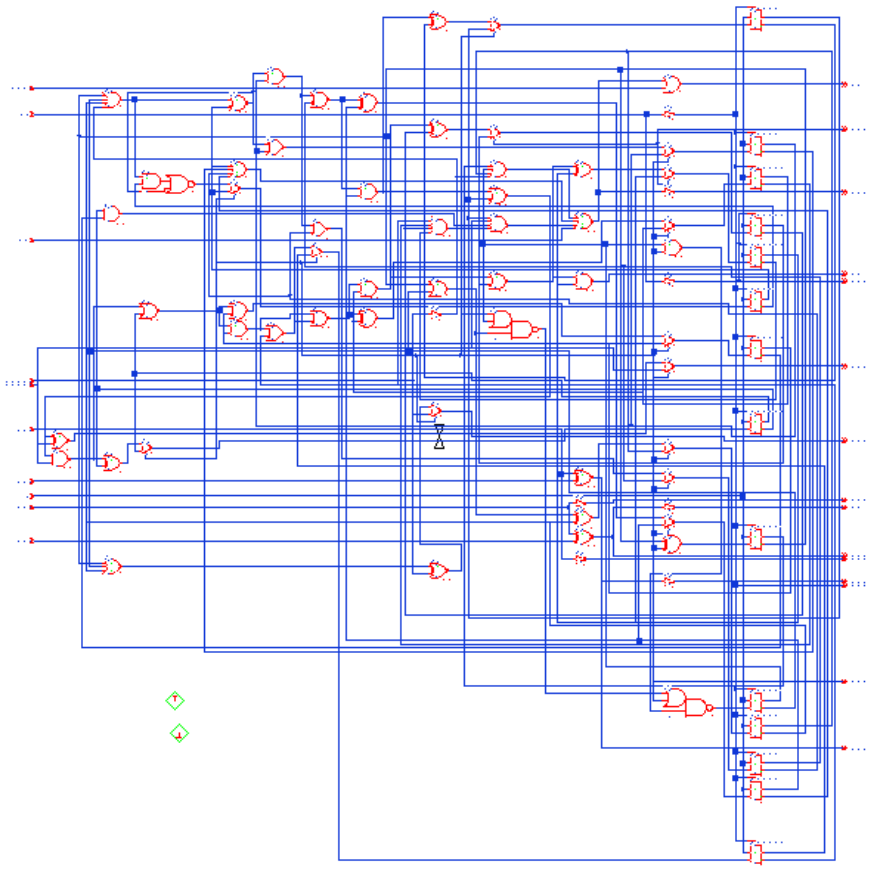

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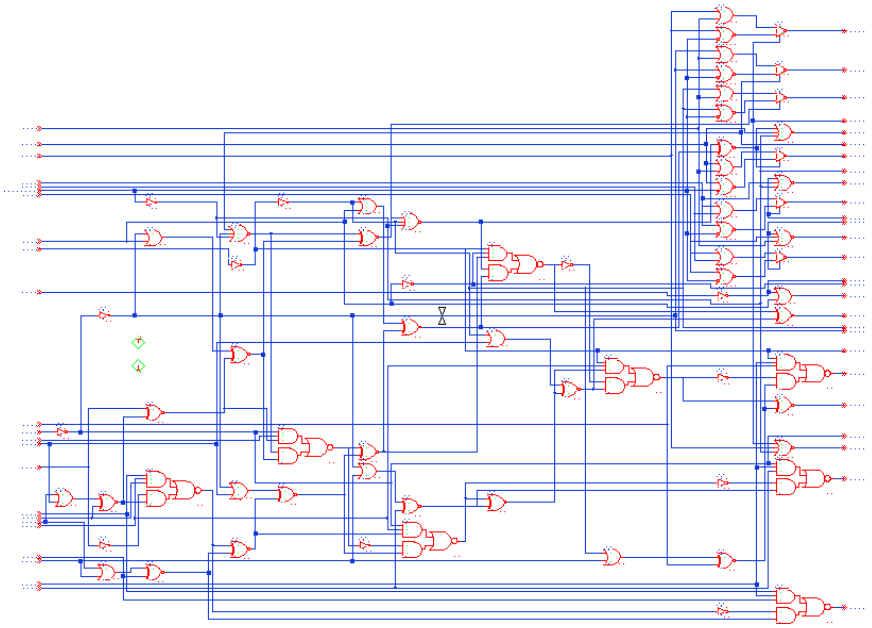

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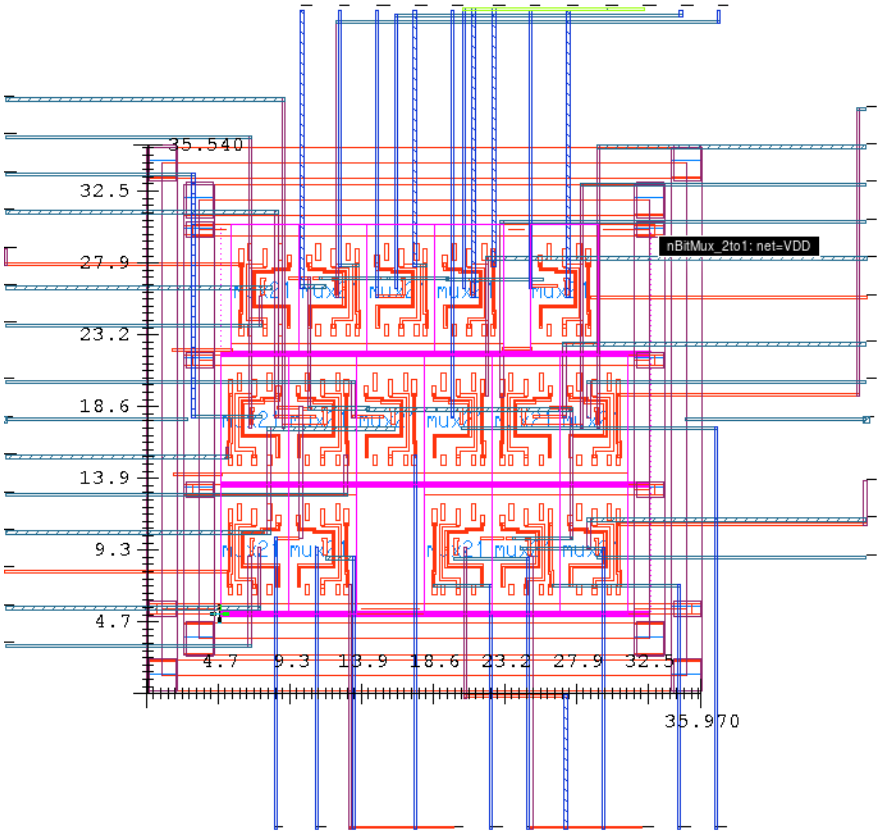

Figure 46: nBitMux 2to1 Layout

3.1 Layout

3.2 Timing

3.3 Power

4 Conclusion

5 Appendix

5.1 VHDL

5.2 Leonardo Scripts

5.3 SPICE

6 References

Key, Brandon A. *CMPE 260 Laboratory Exercise 3 Arithmetic Logic Unit.* CMPE 260 Laboratory Exercise 3 Arithmetic Logic Unit.

// TODO add BIST from DSD II