CMPE-630 Digital IC Design
Laboratory Exercise 2

Design of CMOS Logic Gates

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Contents

1 Abstract

In this exercise, an NMOS transistor and a CMOS inverter were designed in Pyxis, and then simulated using Eldo. The voltage characteristics of the NMOS transistor were analyzed based upon the simulation. The linear and saturation regions of the NMOS were observed. The inverter had multiple simulations to collected voltage and timing properties of the inverter. Temperature was varied from $25\,\mathrm{deg}\,C$ to $125\,\mathrm{deg}\,C$. The max voltage of the inverter was varied between 1.2V and 1.08V. A load capacitor of 120fF was added to the output of the inverter. It was found that the inverter had an input frequency of 10kHz with no load capacitor and an input frequency of 302Hz with the load capacitor. It was found that temperature and voltage have a much smaller impact on frequency response than capacitance.

2 Design Methodology and Theory

A NMOS schematic was designed in Pyxis. The voltage characteristics were the question of the NMOS transistor. A CMOS inverter was created using an NMOS pull-down and a PMOS pull-up transistor. The voltage and timing properties of the inverter were the subject of Eldo simulation.

2.1 NMOS

The NMOS schematic was created by using a standard NMOS and setting the width to 0.26μm and the length to 0.13μm. The length was chosen as a reasonable length that could be easily created. The width was set to be twice the length, which generally creates a favorable NMOS transistor. The resulting schematic can be seen in Figure 2.

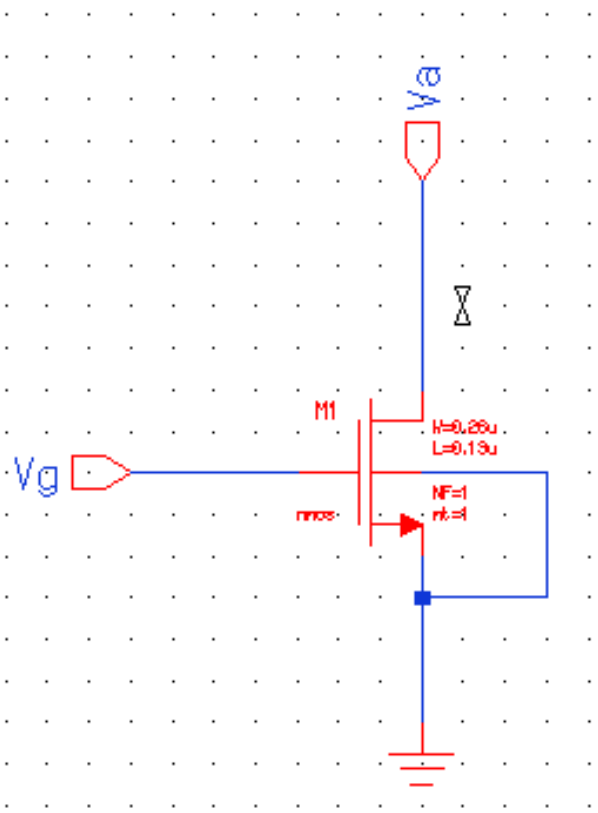

Figure 1: NMOS Transistor Schematic

The transistor should have a linear region where current from drain to source increases more-or-less linearly with voltage applied to the gate. Once the channel of the transistor cannot grow anymore, the transistor becomes saturated and the current plateaus and will not increase while the gate voltage increases.

2.2 Inverter

A PMOS and an NMOS can be combined to create an inverter. A PMOS can pull the output high and an NMOS can pull the output low. The schematic in Figure 2 illustrates the wiring for an inverter.

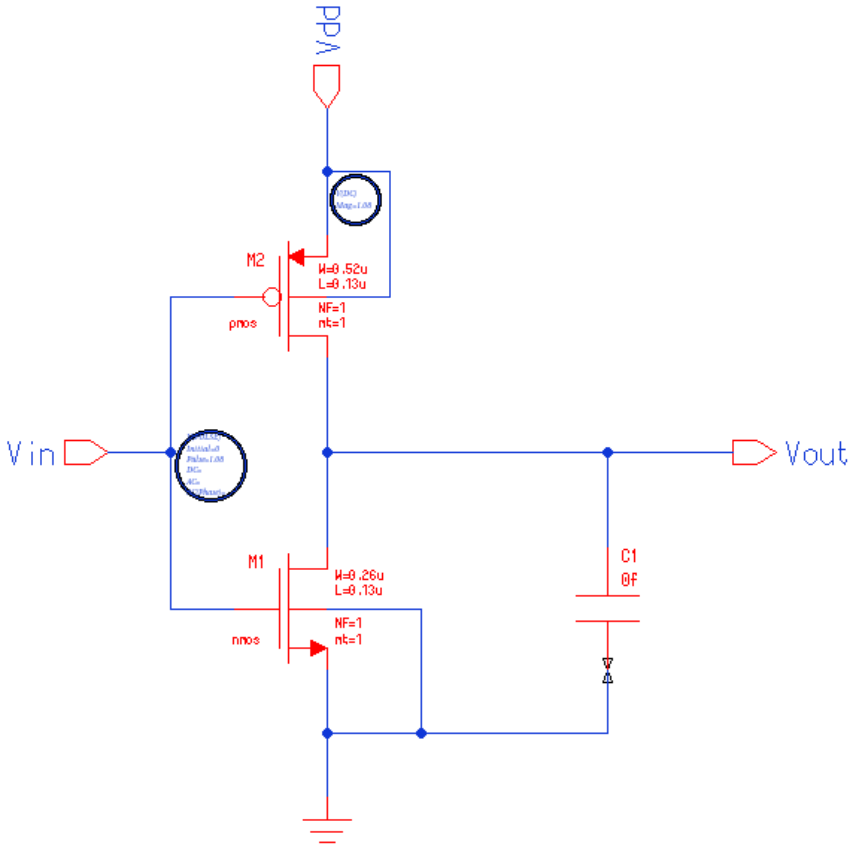

Figure 2: Inverter Schematic

The same NMOS sizing was used

To demonstrate the functionality of the inverter an Eldo simulation was run with V_{dd} being held to 1.2V and the input was swept from 0v to 1.2V with a step of 0.01V. The resulting waveform can be seen in Figure 3.

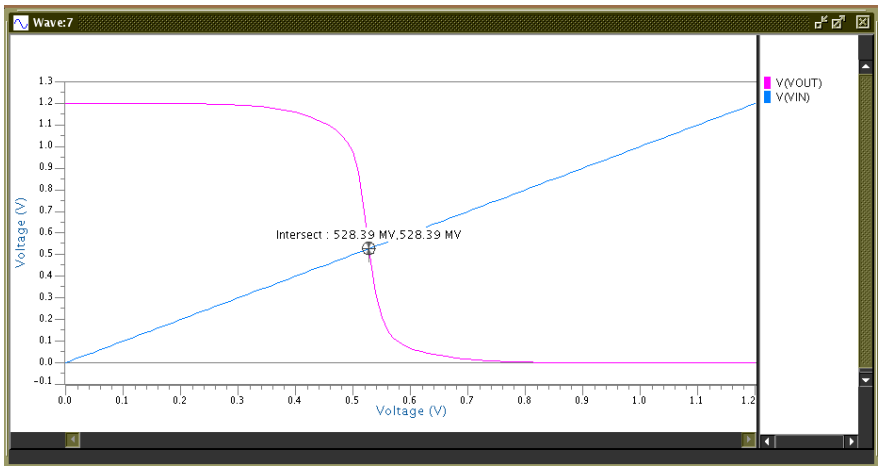

Figure 3: Inverter Voltage Characteristics

If the input is low, the output is high and vice-versa. The transition from low output to high

output is relatively quick. The intersection of the input and output was measured to be (528mV, 5.28mV). Since this value is slightly lower than half of V_{dd}(1.2V) indicating that there is some loss in the transistors.

To see how the changing parameters effects the output, the PMOS width was reduced to 0.13μm. The simulation was re-run and recorded in Figure 4.

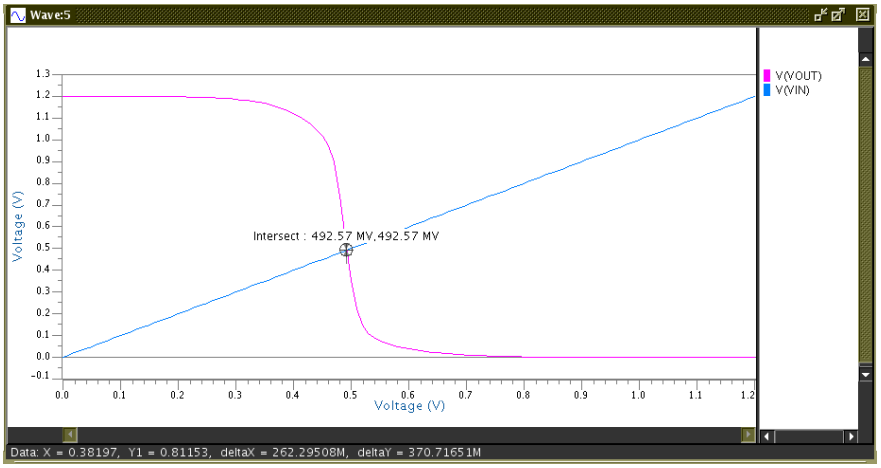

Figure 4: Inverter Simulation with Shorted PMOS Width

The shorter PMOS width shifted the crossover point to a lower voltage, so the inverter stays low longer than it stays high. The crossover point shifts higher if the PMOS width is increased.

3 Results and Analysis

Data tables must be properly presented and label.

Simulations results include waveforms showing the values as they were measured. For a given simulation, all of the measurements should appear on a single plot.

3.1 NMOS

The Eldo simulation was setup to sweep V_{dd} from 0v to 1.2V, stepping by 0.01v. The gate voltage was also swept from 0v to 1.2V with a step of 0.3V. The resulting waveform was captured in Figure 3.

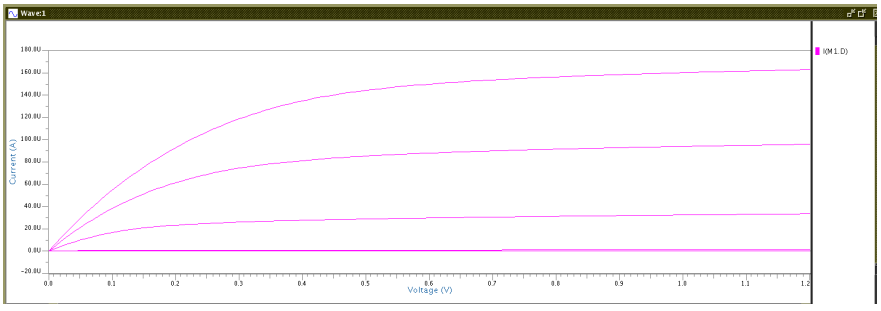

Figure 5: IV Characteristics of NMOS transistor

As the simulation illustrates, at low gate voltages, the current increases linearly, then the current stops increasing once the transistor is saturated. As the drain voltage increases, the gate voltage increases, the saturation region shifts rightward.

3.2 Inverter

The timing characteristics of the inverter were simulated with a transient simulation. V_{dd} was held to 1.2V and the gate voltage was forced to be a pulse with the following properties:

- Magnitude: 1.2V
- Width: 5nS
- Rise Time: 0.1nS
- Fall Time: 0.1nS
- Period: 10ns

The simulation had a temperature of $25\,\mathrm{deg}\,C$. The resulting output is shown in Figure 6.

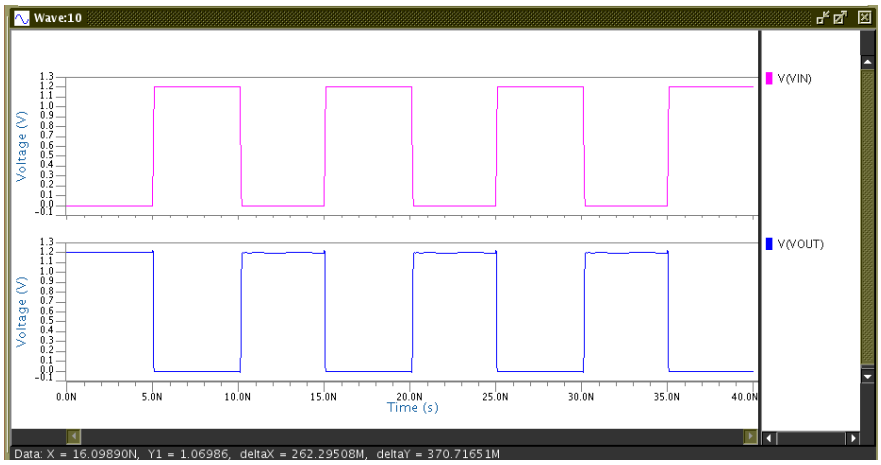

Figure 6: Transient Simulation of Inverter

The waveform was enhanced to highlight the rising and falling edges. Figure 7 shows the falling edge of the output.

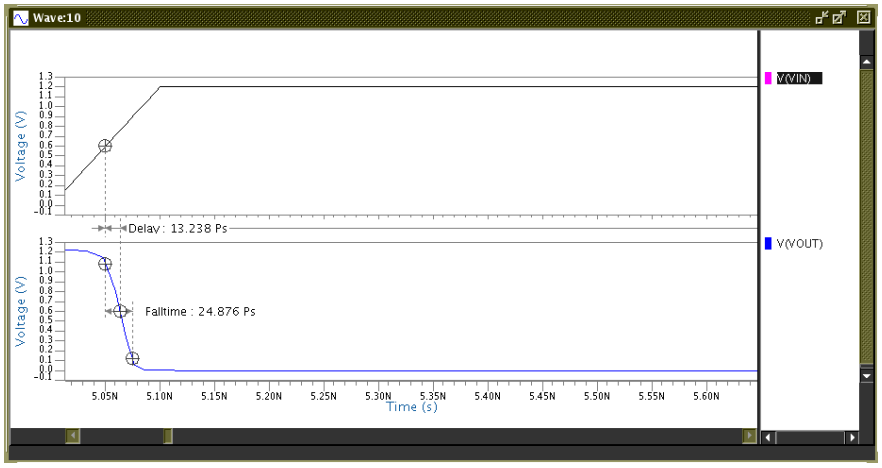

Figure 7: Transient Simulation of Inverter Fall Time and Propagation Delay High to Low. Temp = 25 deg C; C1 = 0fF;

The fall time and the propagation delay from low to high was measured and recorded in Figure 9.

The rise time and the propagation delay from high to low was in Figure 8.

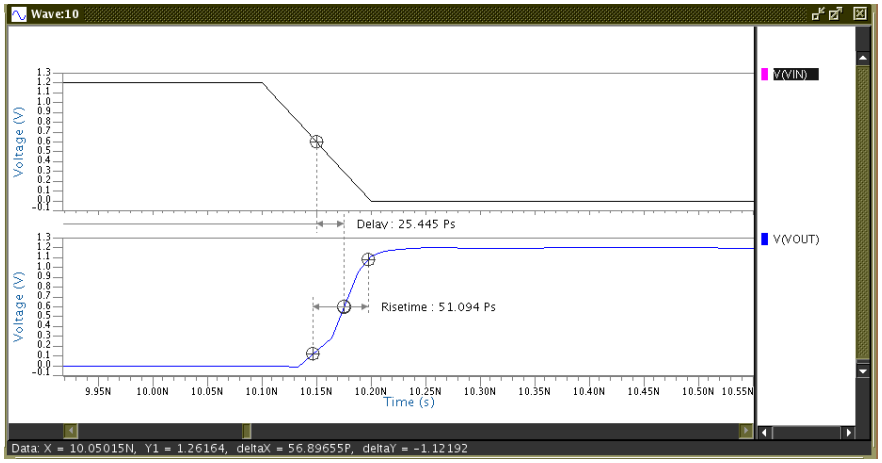

Figure 8: Transient Simulation of Inverter Rise Time and Propagation Delay Low to High. Temp = 25 deg C; C1 = 0fF;

The time to rise took much longer than the time to fall. This is due to the PMOS having a larger channel than the NMOS.

The simulation was repeated with a load capacitor of 120fF. The rise and fall times were increased by over a magnitude.

The simulation was repeated at 125 deg C and a V_{dd} of 1.08V. The higher temperature and lower voltage represent a worse case scenario. The measurements were recorded in Figure 9.

The Rise Time was increased 10%. The increased temperature slows the response of the transistors. The fall time was impacted much more with a slow down of 71%. The propagation delay from high to low was actually lower by 2.7%. This is likely due to the lower voltages. The propagation delay from low to high was increased by 8%. The load capacitor impacted times in the same manor as the nominal case.

Measured Inverter Results							
	Vdd (V)	Temp (°C)	Load (fF)	Rise Time (pS)	Fall Time (pS)	TP,HL (pS)	TP,LH (pS)
Nominal	1.20	25.00	0.00	51.09	24.88	13.24	25.45
	1.20	25.00	120.00	1,740.20	915.55	484.14	816.25
Worst Case	1.08	125.00	0.00	56.41	42.68	12.87	27.56
	1.08	125.00	120.00	2,039.40	1,270.60	603.02	959.53

Figure 9: Measured Inverter Results

The maximum frequency that a transistor can operate properly at can be estimated with the rise/fall times and propagation delays. The input and the throughput have separate frequencies. The maximum input frequency can be estimated with Equation 1. The throughput frequency can be estimated with Equation 2.

$$F_{input,max} = \frac{1}{t_{rise} + t_{fall}} \tag{1}$$

Equation 1: Max Input Frequency

$$F_{throughput,max} = \frac{1}{T_{P,HL} + T_{P,LH}} \tag{2}$$

Equation 2: Max Throughput Frequency

The timing values from Figure 9 were entered into Equation 1 and Equation 2 to obtain the frequency values illustrated in Figure 10.

Calculated Inverter Results					
	Vdd (V)	Temp (°C)	Load (fF)	Finput,max (Hz)	Fthroughput,max (Hz)
Inverter	1.08	125	0	10,091.94	24,729.83
	1.08	125	120	302.11	639.98

Figure 10: Inverter Frequencies

The inverter with nominal voltage and temperature is not spectacularly fast with an input frequency of only 10kHz. Modern transistors are much smaller and would have a much faster switching frequency, but this is a very large transistor. Adding a small capacitive load of 120fF dramatically decreased the maximum frequency of the inverter.

4 Conclusion

This exercise provided a good tutorial for learning the Pyxis schematic and Eldo simulator. The basic properties of a transistor were already known, but were none-the-less proven. This exercise highlighted the incredible sensitivity to capacitance that IC circuits have. Even a small capacitance of 120fF slowed the inverted by over a magnitude, while high temperature and low voltage slowed the inverter by less than 71%. The MOSFETs designed in this exercise were fairly large, which made the frequency response of the inverter very low at 10kHz. Overall this exercise provided a good look at IC design tools and highlighted interesting timing properties of transistors.

Questions

What are the regions of operation for an inverter? Describe the mode of operation for each transistor for the regions.Use the VTC curve that you created as part the exercise.

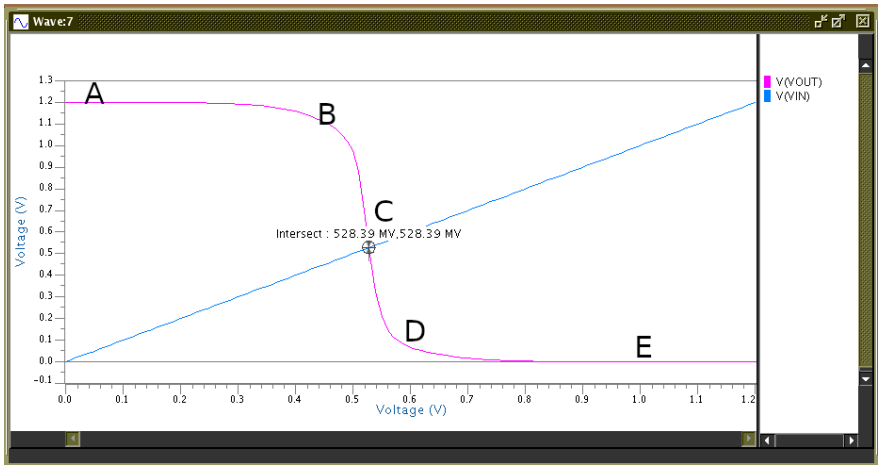

Figure 11: Inverter Modes of Operation

- A - NMOS: Off PMOS: Linear
- B - NMOS: Saturation PMOS: Linear
- C - NMOS: Saturated PMOS: Saturated
- D - NMOS: Linear PMOS: Saturated
- E - NMOS: Linear PMOS: Off

Draw the waveform that would result from a DC sweep of the input of the following circuit. Explain the behavior.

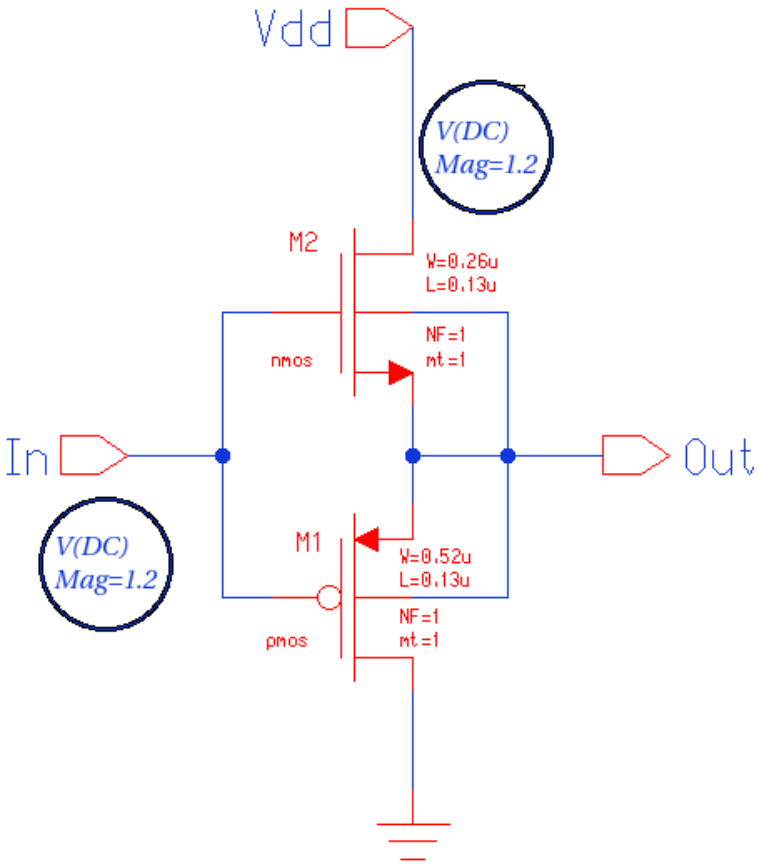

Figure 12: Broken Inverter

The output of this questionable circuit is a curve that follows the input voltage. Both transistors will be in linear operation. This is effectively a terrible, inefficient buffer.

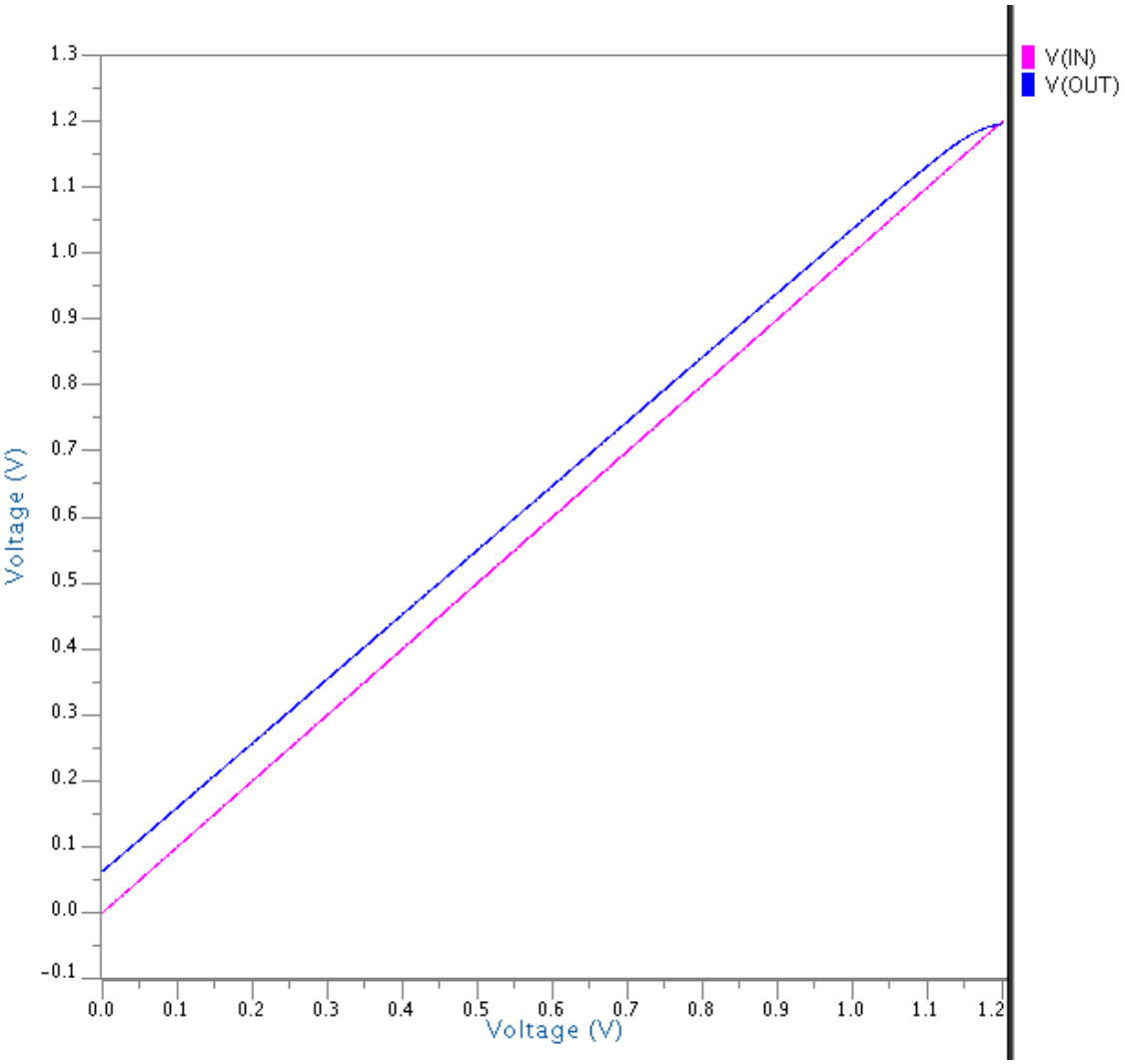

Figure 13: Broken Inverter DC sweep