CMPE-630 Digital IC Design
Laboratory Exercise 3

Mirror Adder

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Contents

1 Abstract

In this exercise, a Mirror Adder was designed, sized, and simulated. The focus of the exercise was mainly on the sizing of the transistors that make up the Mirror Adder. The Mirror Adder has a variety of combinations of transistors, which provide an opportunity to size said transistors. Most notably, the parallel combinations do not yield an increase in width, while the series transistors grow in width proportional to the number of transistors in series. An Eldo simulation was used to verify functionality of the circuit, and then timing values were extracted from the circuit running at 1.08V and 125 degC. The circuit was found to have a maximum input frequency of 9.6GHz and a throughput frequency of 3.1GHz with no load capacitance. When a 120fF load capacitor was applied, the circuit had a maximum input frequency of 293MHz and a throughput frequency of 523MHz, highlighting the disastrous effects of capacitance to a circuit's performance; adding a load capacitance decreased the input frequency by 97%, and throughput frequency was decreased 83.6%. Overall this exercise was successful.

2 Design Methodology and Theory

One of the fundamental design challenges of CMOS circuits is having equal pull strength in both directions. An ideal CMOS circuit only draws power when it is switching; having equal pull strength ensures that the pull is even and draws the least amount of power. The pulling power of a branch of a CMOS circuit is related to it's equivalent resistance. Typically, nMOS transistors have less equivalent resistance because the electrons in the substrate are easier to move than the holes in pMOS transistors. To demonstrate the equivalent resistance of multiple configurations of transistors, a Mirror Adder was designed and sized.

2.1 Functionality

A full adder's functionality is well known and it's truth table is shown in Figure 1.

Full Adder Truth Table				
A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 1: Truth Table for Full Adder

A full adder could be implemented from the truth table in Figure 1, however a Mirror Adder is known to be a simpler and faster circuit. The Mirror Adder schematic can be seen in Figure 2.

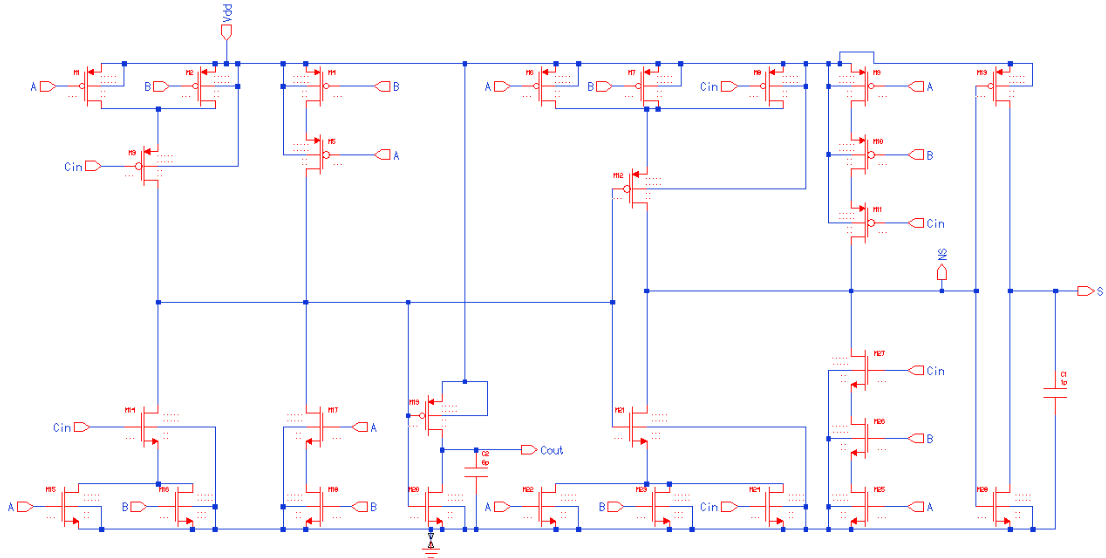

Figure 2: Mirror Adder Schematic

The Mirror Adder supplies the carry out and the sum in one circuit. It also has a maximum series combination of transistors of 3. A trivial implementation of a full adder would require two circuits and would require 4 transistors in series. Having more transistors in series is detrimental to performance because the drain capacitance of the series transistors stack, thus decreasing the frequency response of the system.

2.2 Sizing

To properly size a CMOS circuit for balance, the goal is to maintain the same equivalent resistance as the unit inverter. The unit inverter is the smallest inverter than can be made for a process and can be seen in Figure 3.

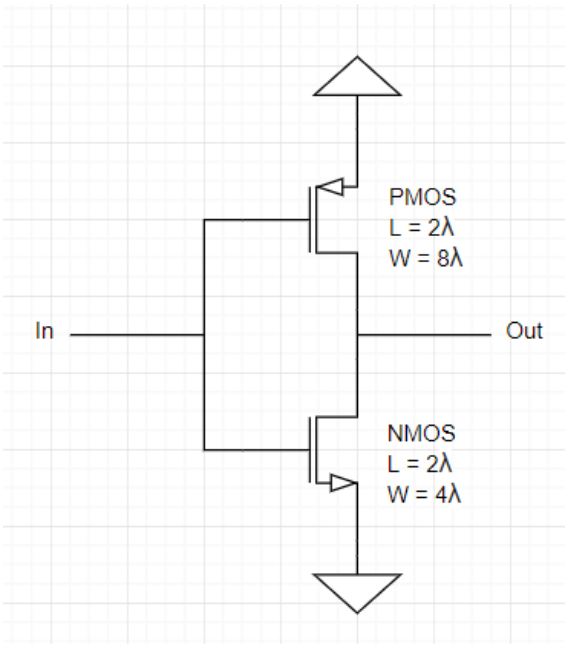

Figure 3: Unit Inverter

To start off, the length of every transistor is twice the process size. There is no reason to make a length any longer than this since it will only decrease performance of a circuit. The width of NMOS and PMOS vary based upon MOS type and configuration. The NMOS width is four times the process size, since this is as small as possible. Historically, the PMOS has about twice the internal resistance of an NMOS. To combat this, the width of the PMOS is double that of the NMOS. Transistors in parallel should not have modified widths, since in the worst case scenario, only one of the transistors will be active. When transistors are in series, current must flow through all of them. The resistance of each individual transistor should be reduced proportional to the number of transistors connected in series; width of transistors in series should be multiplied by the number of transistors in series. Figure 4 shows these sizing rules applied to the Mirror Adder.

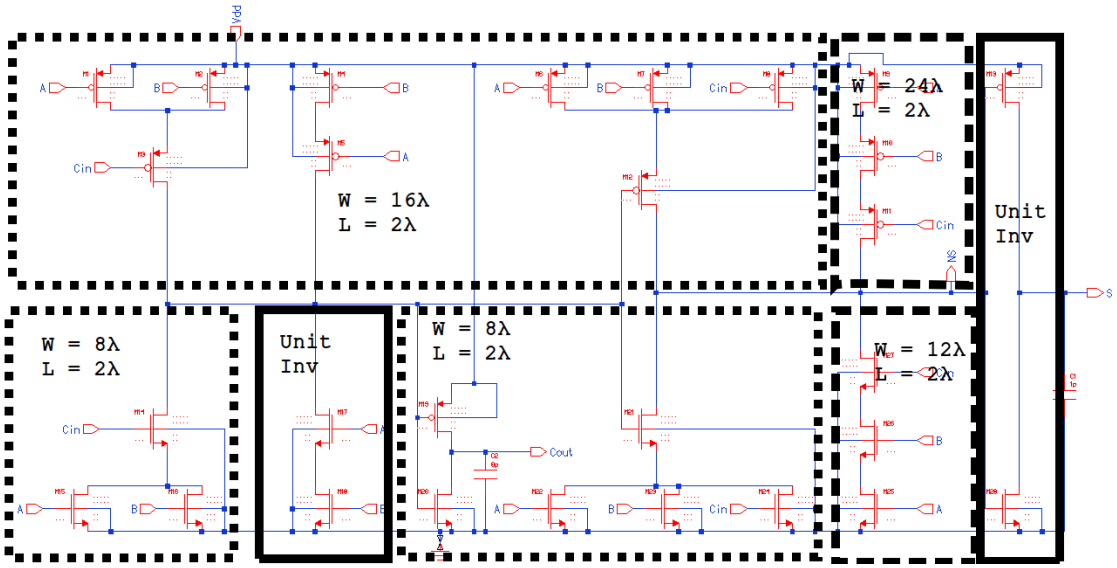

Figure 4: Mirror Adder Transistor Sizing

3 Results and Analysis

An Eldo transient simulation was used to verify functionality and extract timing data from the Mirror Adder. To do this, the inputs A, B, and C_{in} were pulsed in accordance to the truth table in Figure 1. A was pulsed with a period of 40ns, B was pulsed with a period of 80ns, and C_{in} was pulsed with a period of 160ns. All signals had a 50% duty cycle.

3.1 Functionality

To test functionality, all input signals and V_{dd} had a magnitude of 1.2V, and no load capacitance was applied. The resulting waveform can be seen in Figure 5.

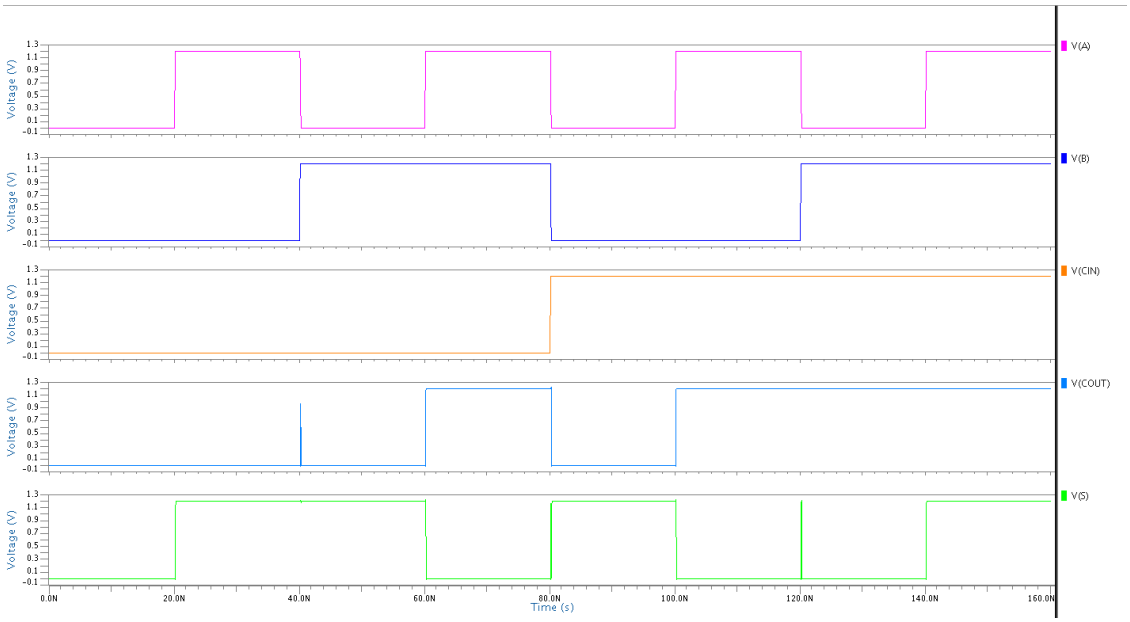

Figure 5: Mirror Adder Transient Simulation for Functionality

To make the graph easier to interpret, the signals were digitized and captured in Figure 6.

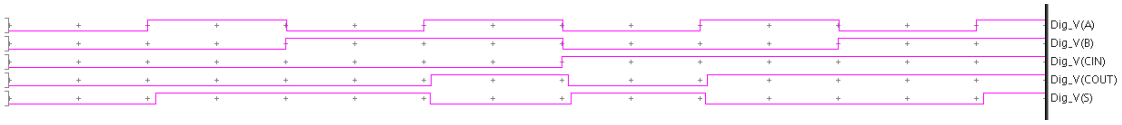

Figure 6: Mirror Adder Transient Simulation with Digitized Inputs

The Eldo simulation verified the functionality of the Mirror Adder. It should be noted that at 40ns, when two of the inputs change simultaneously, C_{out} temporarily spikes.

3.2 Timing

The timing of the circuit was analyzed at a worst-case scenario, with all voltages being 1.08V and the temperature was 125 degC. Then the rise time, fall time, output delay from low to high, and output delay from high to low was measured. The resulting waveform can be seen in Figure 7.

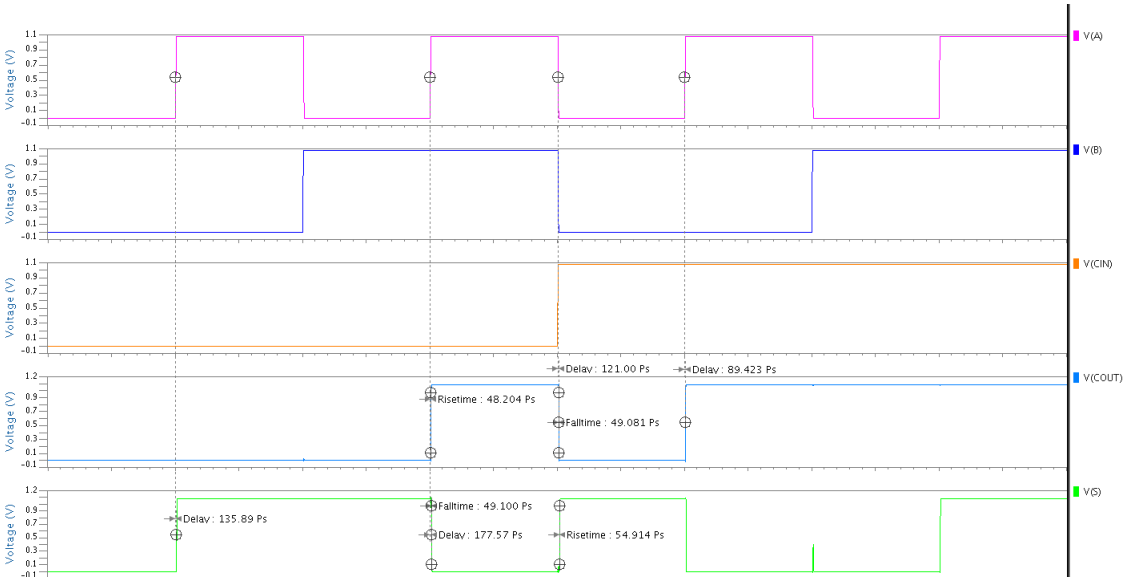

Figure 7: Mirror Adder Transient Simulation for Timing; No Load Capacitance

The measured timing values were recorded in Figure 9 and Figure 10.

Next, the load capacitance was increased to 120fF and all measurements were re0evaluated. The resulting waveform can be seen in Figure 8.

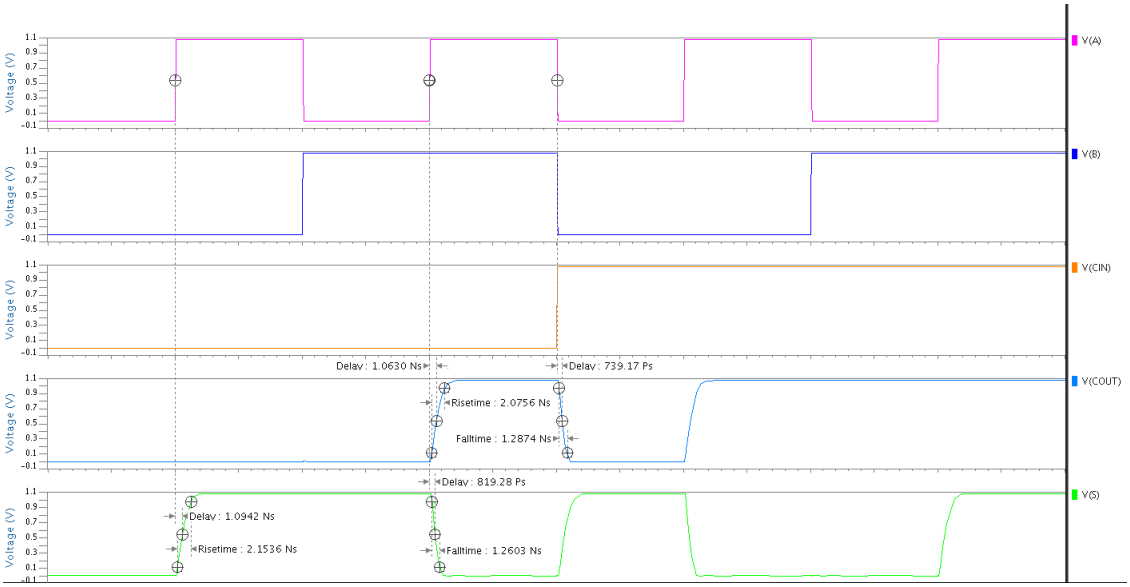

Figure 8: Mirror Adder Transient Simulation for Timing; 120fF Load Capacitance

Again, the measured timing values were recorded in Figure 9 and Figure 10.

Sum							
	Vdd (V)	Temp (°C)	Load (fF)	Rise Time (pS)	Fall Time (pS)	TP,HL (pS)	TP,LH (pS)
Worst Case	1.08	125.00	0.00	54.914	49.10	177.57	135.89
	1.08	125.00	120.00	2,153.60	1,260.30	819.28	1,094.20

Figure 9: Timing Results for Sum

Cout							
	Vdd (V)	Temp (°C)	Load (fF)	Rise Time (pS)	Fall Time (pS)	TP,HL (pS)	TP,LH (pS)
Worst Case	1.08	125.00	0.00	48.20	49.08	121	89.42
	1.08	125.00	120.00	2,075.60	1,287.40	739.17	1,063.00

Figure 10: Timing Results for C_{out}

The capacitor significantly decreased the performance of the circuit. Trying to reduce the capacitance is key in fast circuit design.

The maximum input and throughput frequencies were calculated from the measured timing values according to Equation 1 and Equation 2 respectively.

$$F_{input,max} = \frac{1}{t_{rise} + t_{fall}} \tag{1}$$

Equation 1: Max Input Frequency

$$F_{throughput,max} = \frac{1}{T_{P,HL} + T_{P,LH}} \tag{2}$$

Equation 2: Max Throughput Frequency

The results of the frequency calculations were recorded in Figure 11.

Calculated Maximum Frequency					
	Vdd (V)	Temp (°C)	Load (fF)	Finput,max (kHz)	Fthroughput,max (kHz)
Worst Case	1.08	125	0	9,614,090	3,190,200
	1.08	125	120	292,920	522,608

Figure 11: Frequency Response of Mirror Adder

This circuit has very good frequency response considering the large process that it is utilizing. Adding a load capacitance decreased the input frequency by 97%, and throughput frequency was decreased 83.6%.

4 Conclusion

Balancing transistor sizing is a core technique to integrated circuit design. Ensuring that the pull-up and pull-down network match the resistance of the unit inverter is key to reducing power consumption and speed of a circuit. A Mirror Adder is a simple circuit with a variety of transistor configurations that provides a good practice for transistor sizing. While it is common that PMOS are twice as wide as NMOS, this is not always the case, and this varies from process to process. An important lesson was also learned that schematics must be made larger than first anticipated to allow room for clear wiring, especially for body connections, which tend to be an after though. It was also illustrated that capacitance significantly decreases the performance of a circuit. When the load capacitor was added, the output waveform was drastically altered and adding a load capacitance decreased the input frequency by 97%, and throughput frequency was decreased 83.6%.