ECE 474/574
Fall 2016
Homework 0

Due date: 11.59pm, August 29, 2016
(Note: If you don't complete this homework, you will be dropped from the class!)

1. Sign up on Piazza (sign-up link on Course Syllabus).

2. If you have not done so already, install Xilinx Vivado on your personal computer. You may also use computers in the computer labs, but I strongly recommend that you have it installed on your personal computer.

   Quick Install Instructions (if you've installed it, skip to 3.)
   Use the license-free WebPACK version found here: http://www.xilinx.com/support/download.html. You may be asked to register for an account with Xilinx if you don't already have one. After installation, select the 'Get Free ISE WebPACK…' option. This will lead you to generate a Certificate Based License on the Xilinx website. Make sure 'Vivado Design Suite: HL WebPACK…' is checked, and click Generate Node-Locked License. Click 'Next' until you are prompted that a new license has been emailed to you. Save the license on your computer, go back to the License Manager, select 'Load License', and click on 'Copy License…' Navigate to the location where you saved the license, and select the license to install.

   You may also use a different design tool (e.g., Altera's Quartus), if you prefer.

3. Design and simulate the following circuit, with Verilog, using *(a)* **Procedural design**; and *(b)* **Structural design**.

   "I have two friends from the hiking club and two friends from the basketball team. I will go to a party if, and only if, at least one friend from each team comes with me. Your circuit should output 1 if I go to the party and 0 otherwise."

   You must write one testbench to functionally simulate your circuit. Both procedural and structural designs should output the same waveform with the same testbench.

   Compress (e.g., zip or tar) all your Verilog files (behavioral descriptions and testbench) into one file, and submit on D2L.