CpE 5220
Mini-Project 1
Simple Gates Using VHDL

Goals:

- To create simple gates using the following methods
  - Using basic 2 input gate version as components (30 points)
  - Using primitive gates (OR2, AND2, NOT gates) as components (30 points)
  - Using behavior model (30 points)
  - Using equation model (15 points)
- Implement the following types of gates using VHDL
  - 4 input gate
  - Type

Name	Type
Brandon Valley	NAND, OR, XOR
Justin Chau	NOR, OR, XNOR
Reily Kuechler	NAND, OR, XNOR
Aniesa Parrigon	NOR, OR, XOR
Logan Reed	NAND, OR, XOR
Ryan Reed	NOR, OR, XNOR
Taylor Rhodes	NAND, OR, XNOR
Tyler Tracy	NOR, OR, XOR
Andrew Wheat	NAND, OR, XOR

- Simulation must be performed using a testbench and must be complete for all possible input cases.
- All possible implementations must be executed.
- All models must be synthesized in Quartus. A tutorial on how to view the synthesis is available on Canvas.

Deliverables:

- Presentations: Please plan to present outside class hours either during office hours or via Zoom session. You must present by Sunday, February 9, 2020, 9:00 pm. Please work with me to setup a suitable time for a Zoom session. Set times will be approved on a FIFO basis.
- Submission: Please submit all deliverables, as mentioned in the course outline, by 11:59 pm on Monday, February 10, 2020.