CpE 5220
Mini-Project 2
Combinational Circuits: Datapath Components

NOTE: For VHDL, use of process statement, for system model, is not allowed at this stage!

Goals:

- To create combinational circuits using either one, or the other, or both of the following methods
  - Using basic gates (equation model)
  - Using behavior model
- Implement the following systems using the HDL specified (210 points)
  - Implement the assigned systems in MP1 using Verilog and SystemC
    - Basically repeat MP1 using Verilog and SystemC
    - For Verilog do not use the "Always" block
    - ***Additional Required Step*****
  - A 4:2 encoder: The input is 4-bit (3 down to 0). Input line 0 has the highest priority (both models). (90 points)
    - Include a VALID output bit
    - VHDL, Verilog and SystemC only
    - For Verilog, implement the system both ways, with and without the "Always" block.
    - ***Additional Required Step*****
  - Using the 4:2 encoder created above, a 2:1 encoder and gates of your choice, create an 8:3 encoder using the component model (40 points)
    - VHDL and Verilog
    - ***Additional Required Step*****
  - A 2:4 decoder with active low outputs (both models) (40 points)
    - VHDL and SystemC
    - ***Additional Required Step*****
  - A SN74145 (do some research and find the datasheet) decoder (behavior model only) (45 points)
    - Additional feature. Say the chip has ONE active high Chip Select and TWO active low chip select lines
    - VHDL, Verilog and SystemC
    - ***Additional Required Step*****
  - A 1:4 DeMUX (behavior model only) (15 points): Verilog
  - A 1:8 DeMUX (behavior model only) (30 points): Verilog and SystemC
    - ***Additional Required Step*****
  - A 1:8 DeMUX using 1:4 DeMUX as components (20 points): Verilog
    - ***Additional Required Step*****
  - A 4:1 MUX with active high enable (behavior model only) (15 points): SystemC
  - A 8:1 MUX with active high enable (behavior model only) (20 points): Verilog
    - Do not use the "Always" Block
    - ***Additional Required Step*****
  - A 8:1 MUX using 2:1 MUX as components (15 points) Verilog

- A 8-bit 4:1 MUX with active high enable (behavior model only) (40 points)
  - Verilog and SystemC
  - ***Additional Required Step*****
- A 2-bit 4:1 MUX Using 4:1 MUX as components (40 points)
  - VHDL & Verilog
  - ***Additional Required Step*****

- Consider a microprocessor basic instruction set.

Partial Machine Code	Instruction	Type
0011	X1	LOGIC
1010	X2	ARITHMETIC
1011	X3	ARITHMETIC
0100	X4	LOGIC
1100	X5	ARITHMETIC
0010	X6	LOGIC
1110	X7	LOGIC
1111	X8	BYPASS

Only the most significant 4-bits are shown for the 8 instructions in the set. The most significant 3-bits are used for the basic decoding scheme. The remaining bits are used for additional decoding. The ALU block has 3 basic sub-systems: LOGIC, ARITHMETIC and BYPASS. Each of these blocks will perform the necessary operation depending on the instruction. What needs to be designed is the routing technique to the final ACCUMULATOR register, which is the output of the ALU unit. This routing is managed by a MUX. Design the routing system setup for the select lines of the MUX. (Behavior model only): VHDL, Verilog and SystemC (45 points)

- Simulation must be performed using a testbench and must be complete.
- NOTE: For enable control, assign a high impedance state 'Z', to the output/s, when the system is disabled.
- **For ***Additional Required Step***: Open and compile the model in Quartus and view the synthesized system under RTL viewer. Demonstrate the process and results, and include results in report. A small tutorial is available on Canvas.

Deliverables:

- Presentations: Please plan to present outside class hours either during office hours or via Zoom session. You must present by Sunday, February 24, 2019, 10:00 pm. Please work with me to setup a suitable time for a Zoom session. Set times will be approved on a FIFO basis.
- Submission: Please submit all deliverables, as mentioned in the course outline, by Tuesday, February 29, 2020.

Grading:

- Presentation: 70%
- Report: 30%