Lab Code [10 points]
Filename: chipInterface.sv

```
 1 `default_nettype none
 2
 3 module chipInterface
 4   (input logic SW[5:0],
 5    output logic LEDR[17:16]);
 6
 7    zorgian_nor zorgnor (.a(SW[5]), .b(SW[4]), .c(SW[3]), .d(SW[2]),
 8                         .e(SW[1]), .f(SW[0]),
 9                         .valid(LEDR[17]), .vowel(LEDR[16]));
10
11 endmodule: chipInterface
12
13
```

Lab Code [10 points]
Filename: system_nand.sv

```
1 `default_nettype none
2 module system();
3   logic a, b, c, d, e, f, valid, vowel;
4
5   zorgian_nand zNand1 (a, b, c, d, e, f, valid, vowel);
6   Tester tNor (a, b, c, d, e, f, valid, vowel);
7
8 endmodule: system
```

Lab Code [10 points]
Filename: system_nor.sv

```
1 `default_nettype none
2 module system();
3   logic a, b, c, d, e, f, valid, vowel;
4
5   zorgian_nor zNor1 (a, b, c, d, e, f, valid, vowel);
6   Tester tNor (a, b, c, d, e, f, valid, vowel);
7
8 endmodule: system
```

Lab Code [10 points]
Filename: tester_nor.sv

```
 1 module Tester (output logic a, b, c, d, e, f,
 2                input logic valid, vowel);
 3
 4   // Valid
 5   // abc=100 --> 0
 6   // def=100 --> 0
 7   // def=111 --> 0
 8   // def=101 --> 1 (so long as abc isn't 100)
 9   //
10
11   // Vowel
12   // 0 wherever Valid is 0
13   // def=010 --> 1 for all valid
14   // abc=110 or 001 --> 0 for all valid
15
16   initial begin
17     $monitor($time,,
18      "a = %b, b = %b, c = %b, d = %b, e = %b, f = %b, valid = %b, vowel = %b",
19       a, b, c, d, e, f, valid, vowel);
20         {a, b, c} = 3'b100;
21         {d, e, f} = 3'b111; //also def=111 test //because in 3 k-groups
22
23     #10 {d, e, f} = 3'b010;
24         {a, b, c} = 3'b011; // vowel=1
25
26     #10 {d, e, f} = 3'b100;
27         {a, b, c} = 3'b100; //also abc=100 test //k-groups
28     #10 {a, b, c} = 3'b101; //k-groups
29
30     #10 {d, e, f} = 3'b111;
31         {a, b, c} = 3'b011; //k-groups
32
33     #10 {d, e, f} = 3'b101;
34         {a, b, c} = 3'b101;
35     #10 {a, b, c} = 3'b000;
36
37     // valid=1, vowel=0
38     #10 {a, b, c} = 3'b110;
39         {d, e, f} = 3'b011;
40     #10 {a, b, c} = 3'b001;
41         {d, e, f} = 3'b110;
42
43     #10 $finish;
44   end
45
46 endmodule: Tester
```

Lab Code [10 points]
Filename: zorgian_nand.sv

```
 1 `default_nettype none
 2
 3 module zorgian_nand
 4   (input logic a, b, c, d, e, f,
 5    output logic valid, vowel);
 6
 7    logic va1, va2, va3, va4, va5, va6, va7,
 8          va8, va9, va10, va11, va12, va13, va14,
 9          int1, int2, nint1, nint2, int3, int4,
10          int5, nint4, nint5, int6, nint6, int7,
11          nint7, int8, nint8, int9, nint9, int10,
12          int11, nint10, nint11, int12, nint12, int13,
13          int14, nint13, nint14, int15, nint15,
14          int16, nint16, int17, nint17, int18, nint18,
15          int19, nint19, int20, nint20, int21, nint21,
16          int22, nint22, int23, nint23,
17          vo1, vo2, vo3,
18          nvo1, nvo2, nvo3,
19          intv1, nintv1, intv2, nintv2, intv3, nintv3,
20          intv4, nintv4, intv5, nintv5, intv6, nintv6,
21          no1, no2, no3, no4,
22          o1, o2, o3, o4,
23          not_a, not_b, not_c, not_d, not_e, not_f;
24
25    not (not_a, a),
26        (not_b, b),
27        (not_c, c),
28        (not_d, d),
29        (not_e, e),
30        (not_f, f),
31
32        (no1, o1),
33        (no2, o2),
34        (no3, o3),
35        (no4, o4),
36
37        (nint1, int1),
38        (nint2, int2),
39        (nint4, int4),
40        (nint5, int5),
41        (nint6, int6),
42        (nint7, int7),
43        (nint8, int8),
44        (nint9, int9),
45        (nint10, int10),
46        (nint11, int11),
47        (nint12, int12),
48        (nint13, int13),
49        (nint14, int14),
50        (nint15, int15),
51        (nint16, int16),
52        (nint17, int17),
53        (nint18, int18),
54        (nint19, int19),
55        (nint20, int20),
56        (nint21, int21),
57        (nint22, int22),
58        (nint23, int23),
59
60        (nintv1, intv1),
61        (nintv2, intv2),
62        (nintv3, intv3),
63        (nintv4, intv4),
64        (nintv5, intv5),
65        (nintv6, intv6);
66
67
68    nand (va1, not_b, c, not_e, f),
69         (va2, b, d, not_e, f),
70
```

```
 71          (int1, a, b, c),
 72          (int2, not_d, e),
 73          (va3, nint1, nint2),
 74
 75          (int4, a, not_b, c),
 76          (int5, not_d, f),
 77          (va4, nint4, nint5),
 78
 79          (int6, a, c, not_d),
 80          (int7, not_e, not_f),
 81          (va5, nint6, nint7),
 82
 83          (int8, not_a, b, not_c),
 84          (int9, e, not_f),
 85          (va6, nint8, nint9),
 86
 87          (int10, not_a, b, c),
 88          (int11, not_d, not_e),
 89          (va7, nint10, nint11),
 90
 91          (int12, a, b, not_c),
 92          (int13, not_d, f),
 93          (va8, nint12, nint13),
 94
 95          (int14, a, b, not_c),
 96          (int15, not_d, not_e),
 97          (va9, nint14, nint15),
 98
 99          (int16, not_a, not_b, not_c),
100          (int17, not_d, e),
101          (va10, nint16, nint17),
102
103          (va11, not_a, d, not_e, f),
104
105          (int18, b, c, not_d),
106          (int19, e, not_f),
107          (va12, nint18, nint19),
108
109          (int20, not_a, not_b, not_d),
110          (int21, not_d, not_e),
111          (va13, nint20, nint21),
112
113          (int22, not_a, not_b, c),
114          (int23, d, e, not_f),
115          (va14, nint22, nint23),
116
117          (o1, va1, va2, va3, va4),
118          (o2, va5, va6, va7, va8),
119          (o3, va9, va10, va11, va12),
120          (o4, va13, va14),
121
122          (valid, no1, no2, no3, no4),
123
124          (intv1, not_a, not_c, not_d),
125          (intv2, e, not_f),
126          (vo1, nintv1, nintv2),
127
128          (intv3, b, c, not_d),
129          (intv4, e, not_f),
130          (vo2, nintv3, nintv4),
131
132          (intv5, a, not_b, c),
133          (intv6, not_d, not_e, f),
134          (vo3, nintv5, nintv6),
135
136          (vowel, vo1, vo2, vo3);
137
138 endmodule: zorgian_nand
139
140
141
```

142
143
144

Lab Code [10 points]
Filename: zorgian_nor.sv

```
 1 `default_nettype none
 2 module zorgian_nor
 3   (input logic a, b, c, d, e, f,
 4    output logic valid, vowel);
 5
 6    logic z1, z2, z3, z4, z5, z6,
 7          z7, z8, z9, z10, z11, z12, z13,
 8          int1, int2, int3, int4, int5, int6,
 9          int7, int8, int9, int10, int11, int12,
10          int13, int14, int15, int16, int17, int18,
11          int19, int20, int21, int22, int23, int24,
12          int25, int26, int27, int28, int29, int30,
13          vo1, vo2, vo3, vo4, vo5,
14          vo6, vo7, vo8, vo9, vo10,
15          vo11, vo12, vo13, nvo11, nvo12, nvo13,
16          no1, no2, no3, no4,
17          o1, o2, o3, o4,
18          not_a, not_b, not_c, not_d, not_e, not_f;
19
20    not (not_a, a),
21        (not_b, b),
22        (not_c, c),
23        (not_d, d),
24        (not_e, e),
25        (not_f, f),
26        (o1, no1),
27        (o2, no2),
28        (o3, no3),
29        (o4, no4),
30        (int19, int1),
31        (int20, int2),
32        (int21, int4),
33        (int22, int5),
34        (int23, int7),
35        (int24, int8),
36        (int25, int10),
37        (int26, int11),
38        (int27, int13),
39        (int28, int14),
40        (int29, int16),
41        (int30, int17),
42        (vo11, nvo11),
43        (vo12, nvo12),
44        (vo13, nvo13);
45
46    nor (z1, not_d, not_e, not_f),
47
48        (int1, a, b, not_c),
49        (int2, d, not_e),
50        // invert
51        (z2, int20, int19),
52
53        (z3, not_a, b, c),
54        (z4, not_a, b, not_e, f),
55        // invert
56        (z5, a, not_b, not_e, not_f),
57
58        (int4, a, c, d),
59        (int5, e, not_f),
60        // invert
61        (z6, int21, int22),
62
63        (int7, a, not_b, c),
64        (int8, d, e),
65        // invert
66        (z7, int23, int24),
67
68        (z8, not_a, c, not_e, f),
69        (z9, not_d, e, f),
70        (z10, not_a, not_d, not_e),
```

```
 71
 72        (int10, not_a, not_b, not_c),
 73        (int11, d, e, not_f),
 74        // invert
 75        (z11, int25, int26),
 76
 77        (int13, a, b, c),
 78        (int14, not_d, not_e),
 79        // invert
 80        (z12, int28, int27),
 81
 82        (no1, z1, z2, z3, z4),
 83        (no2, z5, z6, z7, z8),
 84        (no3, z9, z10, z11, z12),
 85
 86        (int16, a, not_b, not_c),
 87        (int17, not_d, not_e),
 88        // invert
 89        (no4, int30, int29),
 90
 91        (valid, o1, o2, o3, no4),
 92        // (valid, a),
 93
 94
 95        (vo1, c, e),
 96        (vo2, not_e, not_f),
 97        (vo3, not_d, not_e),
 98        (vo4, not_c, not_d),
 99        (vo5, e, f),
100        (vo6, a, e),
101        (vo7, not_b, e),
102        (vo8, not_a, c),
103        (vo9, not_a, b, not_e),
104        (vo10, b, not_c, not_e),
105
106        (nvo11, vo1, vo2, vo3, vo4),
107        (nvo12, vo5, vo6, vo7, vo8),
108        (nvo13, vo9, vo10),
109
110
111        (vowel, vo11, vo12, vo13);
112
113 endmodule: zorgian_nor
114
115
116
117
118
119
```