Problem 7: [6 points]
Filename: hw1prob7.sv

```
 1 `default_nettype none
 2
 3 module hw1prob7
 4   (input logic a, b, c, d,
 5    output logic prime, div3);
 6
 7   logic p1, p2, p3, p4, t1, t2, t3, t4,
 8         t5, t6, a_not, b_not, c_not, d_not;
 9
10   not (a_not, a),
11       (b_not, b),
12       (c_not, c),
13       (d_not, d);
14
15   and (t1, a_not, b_not, c, d),
16       (t2, a_not, b, c, d_not),
17       (t3, a, b_not, c_not, d),
18       (t4, a, b, c_not, d_not),
19       (t5, a, b, c, d),
20       (p2, a_not, b_not, c),
21       (p3, a_not, b, d),
22       (p4, d, p1);
23
24   or (prime, p2, p3, p4),
25      (div3, t1, t2, t6),
26      (t6, t3, t4, t5);
27
28   xor (p1, b, c);
29
30 endmodule: hw1prob7
31
32
33
```

Problem 8: [6 points]
Filename: hw1prob8.sv

```
 1 `default_nettype none
 2 module hw1prob7_test
 3   (input logic prime, div3,
 4    output logic a, b, c, d);
 5
 6    initial begin
 7      $monitor($time,,
 8      "a = %b, b = %b, c = %b, d = %b, prime = %b, div3 = %b",
 9      a, b, c, d, prime, div3);
10      a = 0;
11      b = 0;
12      c = 0;
13      d = 0;
14      #10 d = 1;
15      #10 c = 1;
16          d = 0;
17      #10 d = 1;
18      #10 b = 1;
19          c = 0;
20          d = 0;
21      #10 d = 1;
22      #10 d = 0;
23          c = 1;
24      #10 d = 1;
25      #10 b = 0;
26          c = 0;
27          d = 0;
28          a = 1;
29      #10 d = 1;
30      #10 c = 1;
31          d = 0;
32      #10 d = 1;
33      #10 b = 1;
34          c = 0;
35          d = 0;
36      #10 d = 1;
37      #10 d = 0;
38          c = 1;
39      #10 d = 1;
40      #10 $finish;
41    end
42 endmodule: hw1prob7_test
43
44 module system();
45   logic a_in, b_in, c_in, d_in, p_out, div_out;
46   hw1prob7 INST (.a(a_in), .b(b_in), .c(c_in), .d(d_in),
47                  .prime(p_out), .div3(div_out));
48   hw1prob7_test (.a(a_in), .b(b_in), .c(c_in), .d(d_in),
49                  .prime(p_out), .div3(div_out));
50 endmodule: system
51
```

Problem 12: [12 points] Drill problem
Filename: hw1prob12.sv

```
 1 `default_nettype none
 2 module hw1prob12
 3   (input logic a, b, c,
 4    input logic loc1, loc0,
 5    output logic dir1, dir0);
 6
 7    logic d11, d12, d13, d14, d15, d16, d17, d01, d02, d03,
 8          d04, d05, d06, n_b, n_c, n_loc1, n_loc0;
 9
10    not    (n_loc1, loc1),
11           (n_loc0, loc0),
12           (dir1, loc0),
13           (n_b, b),
14           (n_c, c);
15
16    and    (d01, loc1, loc0),
17           (d02, loc0, n_b),
18           (d03, n_c, n_loc1, loc0),
19           (d04, a, c, loc0),
20           (d05, a, b, c, loc1);
21
22    or     (d06, d01, d02, d03),
23           (dir0, d04, d05, d06);
24 endmodule: hw1prob12
25
26 module circTester
27   (input logic dir1, dir0,
28    output logic a, b, c, loc1, loc0);
29
30    initial begin
31      $monitor($time,,
32               "a = %b, b = %b, c = %b, loc1 = %b, \
33                loc0 = %b, dir1 = %b, dir0 = %b",
34                a, b, c, loc1, loc0, dir1, dir0);
35      for (int i = 0; i < 32; i = i + 1) begin
36        {a, b, c, loc1, loc0} = i;
37        #10;
38      end
39    end
40 endmodule: circTester
41
42 module system();
43   logic a_in, b_in, c_in, l1_in, l0_in, d1_out, d0_out;
44   hw1prob12 INST (.a(a_in), .b(b_in), .c(c_in), .loc1(l1_in),
45                   .loc0(l0_in), .dir1(d1_out), .dir0(d0_out));
46   circTester MEEP (.a(a_in), .b(b_in), .c(c_in), .loc1(l1_in),
47                    .loc0(l0_in), .dir1(d1_out), .dir0(d0_out));
48 endmodule: system
```

Problem 13: [8 points] Drill problem
Filename: hw1prob13.sv

```
 1 `default_nettype none
 2 module hw1prob13
 3   (input logic a, b, c,
 4    output logic f, f1, f2, f3, b_not);
 5
 6
 7    not #1 (b_not, b);
 8    and #6 (f1, b_not, a),
 9           (f2, a, f1);
10    or  #5 (f3, f1, c);
11    xor #9 (f, f2, f3, 1);
12 endmodule: hw1prob13
13
14 module testTable
15   (output logic a, b, c,
16    input logic f, f1, f2, f3, b_not);
17
18    initial begin
19    $monitor($time,,
20             "a = %b, b = %b, c = %b, b_not = %b, \
21              f1 = %b, f2 = %b, f3 = %b, f = %b",
22              a, b, c, b_not, f1, f2, f3, f);
23    a = 1;
24    b = 1;
25    c = 0;
26
27    #12 a = 0;
28        c = 1;
29    #15 $finish;
30    end
31 endmodule: testTable
32
33 module system();
34   logic a, b, c, b_not, f, f1, f2, f3;
35   hw1prob13 up (.a, .b, .c, .b_not, .f1, .f2, .f3, .f);
36   testTable dawg (.a, .b, .c, .b_not, .f1, .f2, .f3, .f);
37 endmodule: system
38
39
```