Problem 1: [8 points] Drill problem
Filename: hw5prob1.sv

```
 1 `default_nettype none
 2
 3 module hw5prob1
 4   (input logic Input, clock, reset_n,
 5    output logic Prob1);
 6
 7   logic [1:0] state, nextState;
 8
 9   always_comb begin
10     nextState[0] = ~Input;
11     nextState[1] = state[0] & Input | state[1] & ~state[0] & ~Input;
12   end
13
14   assign Prob1 = state[1] & state[0];
15
16   always_ff @(posedge clock, negedge reset_n)
17     if (~reset_n)
18       state <= 2'b0;
19     else
20       state <= nextState;
21 endmodule: hw5prob1
22
```

Problem 2: [8 points] Drill problem
Filename: hw5prob2.sv

```
 1 `default_nettype none
 2
 3 module hw5prob2
 4   (input logic Input, clock, reset_n,
 5    output logic Prob2);
 6
 7   logic [1:0] state, nextState;
 8
 9   always_comb begin
10     nextState[0] = ~Input;
11     nextState[1] = state[0] & Input;
12   end
13
14   assign Prob2 = ~state[1] & state[0] & ~Input;
15
16   always_ff @(posedge clock, negedge reset_n)
17     if (~reset_n)
18       state <= 2'b0;
19     else
20       state <= nextState;
21 endmodule: hw5prob2
22
```