Lab Code [5 points]
Filename: Tutorial.sv

```
 1 module Tutorial
 2   (output logic f,
 3    input logic a, b, c, d);
 4
 5    logic f1, f2;
 6
 7    nand g1(f, f1, f2),
 8         g2(f1, a, b),
 9         g3(f2, c, d);
10
11 endmodule: Tutorial
```

Lab Code [5 points]
Filename: chipInterface.sv

```
1 `default_nettype none
2 module chipInterface
3   (input logic SW[17:0],
4    output logic LEDR[17:0]);
5
6    multiplexer DUT (.a(SW[0]), .b(SW[1]), .sel(SW[17]), .f(LEDR[17]));
7 endmodule: chipInterface
```

Lab Code [5 points]
Filename: lab0.sv

```
 1 `default_nettype none
 2
 3 module multiplexer
 4   (output logic f,
 5    input logic a, b, sel);
 6
 7    logic f1, f2, n_sel;
 8
 9    and #2 g1(f1, a, n_sel);
10    and #2 g2(f2, b, sel);
11    or  #2 g3(f, f1, f2);
12    not    g4(n_sel, sel);
13
14 endmodule: multiplexer
15
16 module muxTester
17   (output logic a, b, sel,
18    input logic muxOut);
19
20    initial begin
21    $monitor($time,,
22    "a = %b, b = %b, sel = %b, muxOut = %b",
23    a, b, sel, muxOut);
24    a = 0;
25    b = 0;
26    sel = 0;
27    #10 b = 1;
28    #10 a = 1;
29    #10 b = 0;
30    #10 sel = 1;
31    #10 b = 1;
32    #10 a = 0;
33    #10 b = 0;
34    #10 $finish;
35    end
36
37 endmodule: muxTester
38
39 module system();
40   logic wire_a, wire_b, select, mux_out;
41
42   multiplexer DUT (.a(wire_a), .b(wire_b), .f(mux_out), .sel(select));
43   muxTester mt (.a(wire_a), .b(wire_b), .muxOut(mux_out), .sel(select));
44
45 endmodule: system
```