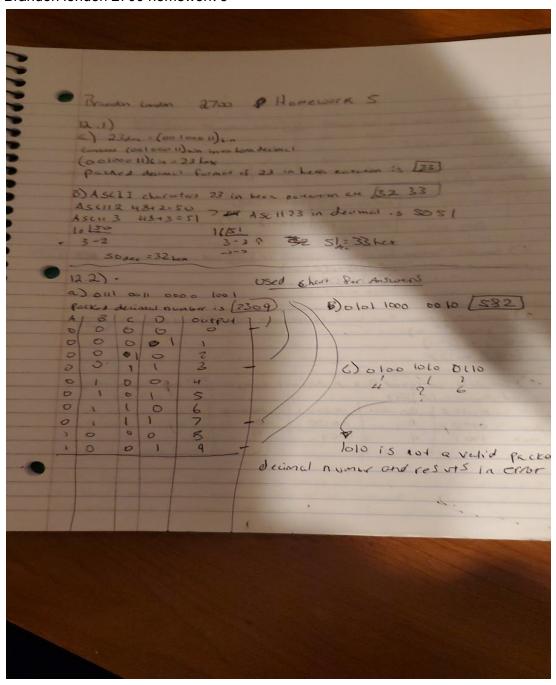
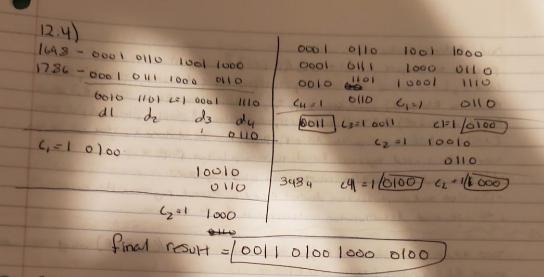
Brandon london 2700 homework 5



	100
	-
(3.2)a)	
/x3=x2/	
$6)/x_3 = (x_2)$	
C)/ Effective address = PG + off set +1	
X3=X1 TX2 T1	-
33:01 102:01	
$d) \chi_3 = \chi_2 + \chi_4$	-
	- 5
Relation ship between various addressing modes is shown above	
13.3) a) The address of the operand remains in the instruction its est as	
immediate value. Thus, in immediate addressing mode, effective address of	
oporno is[14]	
b) A diffess of the operand with differt addressing mode is memory local	tion
1 414	
() in Indires addressing, address of the dark is held in intermedate bearing	
- first checks for the address and then weed to locate and identity the date	
EATU)	٠,
* effective address of the operand is memory pocation whose address is in	
Memory location 14 that is stored in the address x	
The veries a	
d) address of the speaned using sea sate address	
d) address of the speamed using register addressing mode is register to	4/
e) memory location whose address is in register 14	-
minuse address is in regiliter 14	
	To the same

one Address Instruction: Program to compute x = (1+3×4)/(D-EXF) & using on address: land E; Load value of Envil F; muttiply value of E with Estone Ri, Store result in Rload D; road later Dove R; Substant lesuit & with Distance R; State result of (D-EXF) D-EX F in Rload B; load valve of Brull; multiply 3 with CADDA; Add now with ADIVE; Divid & with Astore x; store result in one address ared registers for data manipulation purpose. Addition and subtraction in struction uses Yeg istors. · Division and multiplication doesn't theed a second register. However its assumed Accumulator contains result of the operation Two Address Instruction: Program to compute X: (4+3xc) (D-EXF) wing Two coldress Move RIE; more & to register RI mul RI, F , together. contents of RI (F) is multiplied with F and stone result in RI move R2; D move D to register Rd SUB R2, R1; SUBTRACT CONTENT R1 and TO CO) and stope result in R2 move KI, 3', move B to register KI mul RI, C', multiple register R | (6) with c and store result in R 1 Add RI, A; Add RICE) Div RI, RZ; Divide RI with RZ and store the results in RI. move x, ei; finally stone content of RI tox · The most common instruction in the working language was is two additions boarding Presenctions , each add ress field in the instruction specifics * register * memory word "more instruction in two address moves the data to and from memory locations to registers Three Address Next Page



Descriptions instruction program to compute x = (A18x0/(D-EXF)

Using 2000 address | 2000 Address instructions are the instructions organized

PUSh A; Rish A to stace to stack in which it not used addresses fields for the

Push B; Rish B to stack above said instructions (Add, mul, Dig SUG, Rish Pop

Posh C; Rush C to Stack of prevent sources and destination are both implicit

mv L; multiply B with C in zero address instruction.

Add't Add rest with A address at appeared will be in special register which

Push B; Rish B to stack Is automortically incremented or decremented.

Push E; Rish B to stack for expression (A + BXC)

Push F; Rish B to stack for expression (A + BXC)

Push F; Rish B to stack for expression (A + BXC)

Push F; Rish B to stack for expression (A + BXC)

Push F; Rish B to stack for expression (A + BXC)

Push F; Rish B to stack for expression (B + BC)

Subj subject of add with substract result.

Popx; Rish result of add with substract result.

Popx; Rish result of add with substract result.

Popx; Rish result of add with substract result.

D is first moved "D" to top of the Stack, then is to top of the stack and F to top of stou. Now the context of top of the stone is F. multiply top of sten F and E acc store 12017. SUBTRACT of and store after allelen. 126) Three address instruction: Program to compute x - (A+3×4) (O-EXF) esing three addrewi MUL RI, E. P. mustiply Eard & P & motory Fall Prend SUBRIDORI, Subtract RI (EXF) with Dard store in RI mul Ra, B, (multiply 3 and L and store lesult in Ra Add Rd, A, R2; Add R2 (8xc) with A and store result in R2 Div, RI, RZ', Divide RI by Rz and stare result inx · Every instruction in three address instruction uses processor register or Memory operands * Three Address instruction takes omy 5 instructions to evaluate the given expression where of two address tunes a instructions, one takes 11 instructions and 2000 address takes 12 instructions. 13.1-13.3 instruction itself contains immediate value 20 opperand=20 This load immediate 30 results with data 201. 6) load direct 20 results with Fetching data 407 () in indirect addressing, address of the data is held in intermediate location word 20 contains 40 Thes, load induced to results with fething data 60 d operend = 30 Load immediate 30 results with data [30] e) Load direct 30 results with fetching ded a 50] F. load indirect 30 resurts in fateling data [70]

