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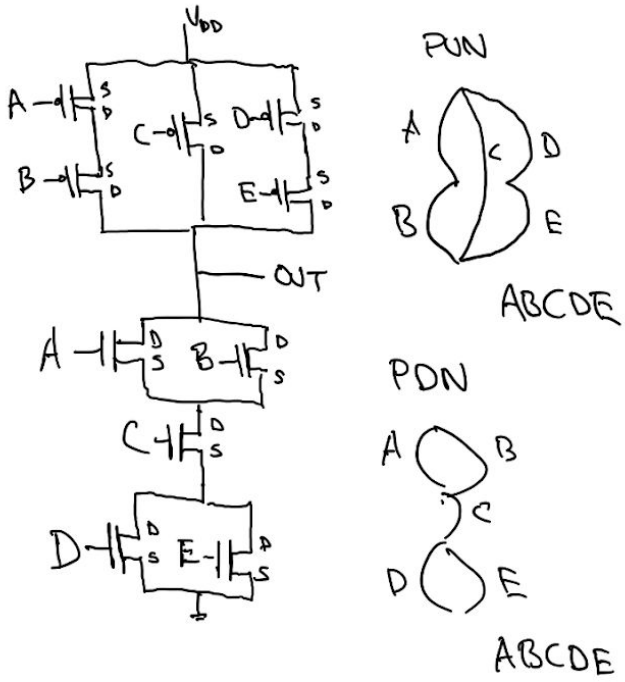
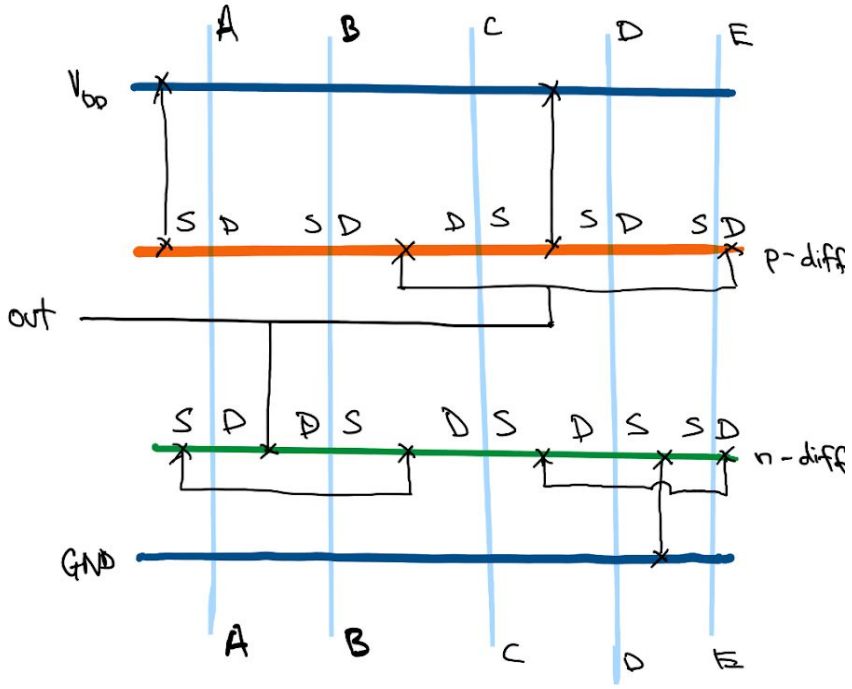
Project 2 EECS119

1. Complete diagram

$$F = !((A+B)\cdot C-(D+E))$$



2. Stick diagram

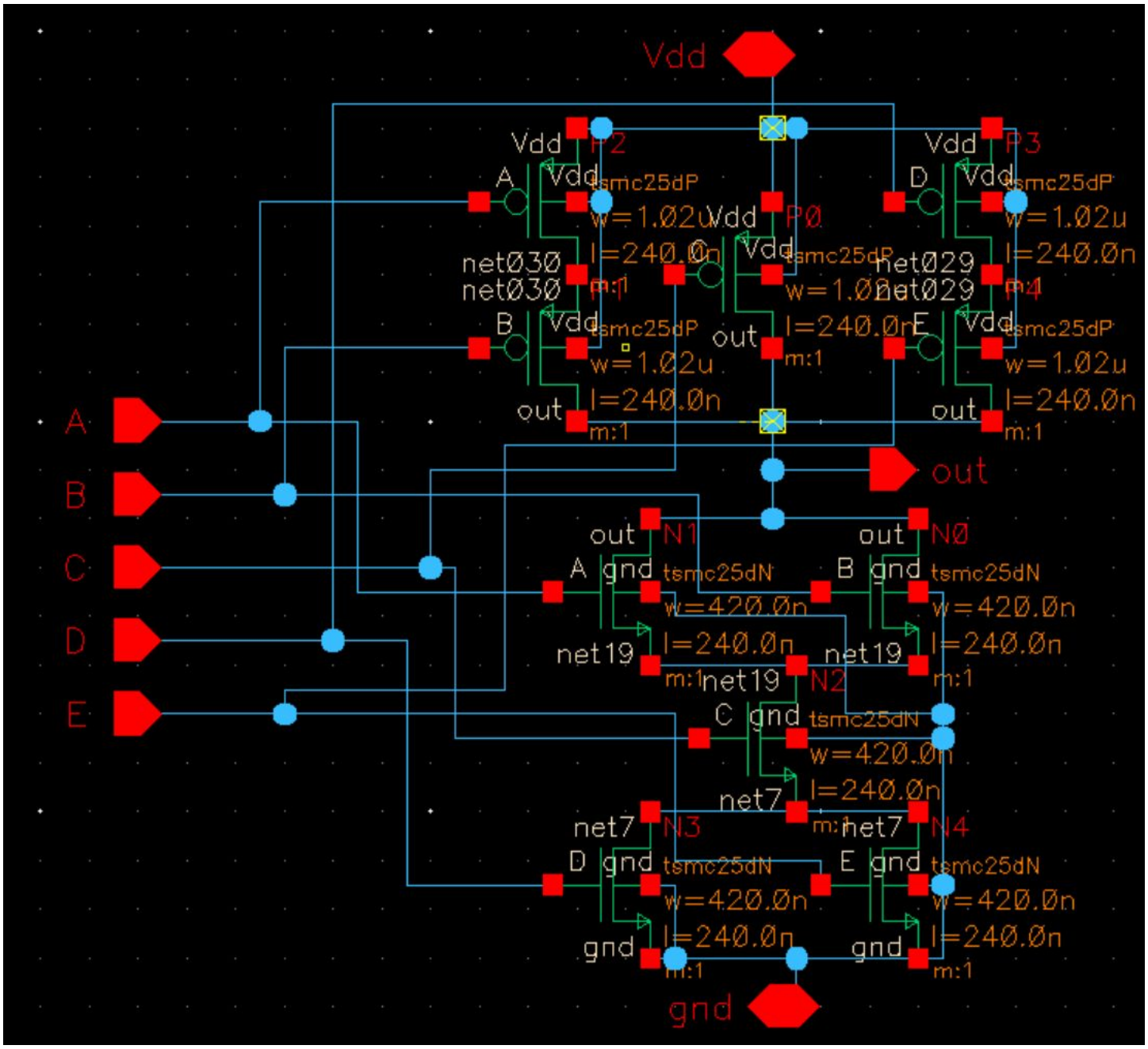


A	B	C	D	E	! ((A|B)&C& (D|E))
1	1	1	1	1	0
0	1	1	1	1	0
1	0	1	1	1	0
0	0	1	1	1	1
1	1	0	1	1	1
0	1	0	1	1	1
1	0	0	1	1	1
0	0	0	1	1	1
1	1	1	0	1	0
0	1	1	0	1	0
1	0	1	0	1	0
0	0	1	0	1	1
1	1	0	0	1	1
0	1	0	0	1	1
1	0	0	0	1	1
0	0	0	0	1	1
1	1	1	1	0	0
0	1	1	1	0	0
1	0	1	1	0	0
0	0	1	1	0	1
1	1	0	1	0	1
0	1	0	1	0	1
1	0	0	1	0	1
0	0	0	1	0	1
1	1	1	0	0	1
0	1	1	0	0	1
1	0	1	0	0	1
0	0	1	0	0	1
1	1	0	0	0	1
0	1	0	0	0	1
1	0	0	0	0	1
0	0	0	0	0	1

3. First make the schematic, create symbol view for test, simulate expected results, create layout in standard cell technique and uninterrupted diffusion regions, extract view and use LVS, extract with parasitic capacitors, then config the test schematic with the extracted_c analog view, then simulate

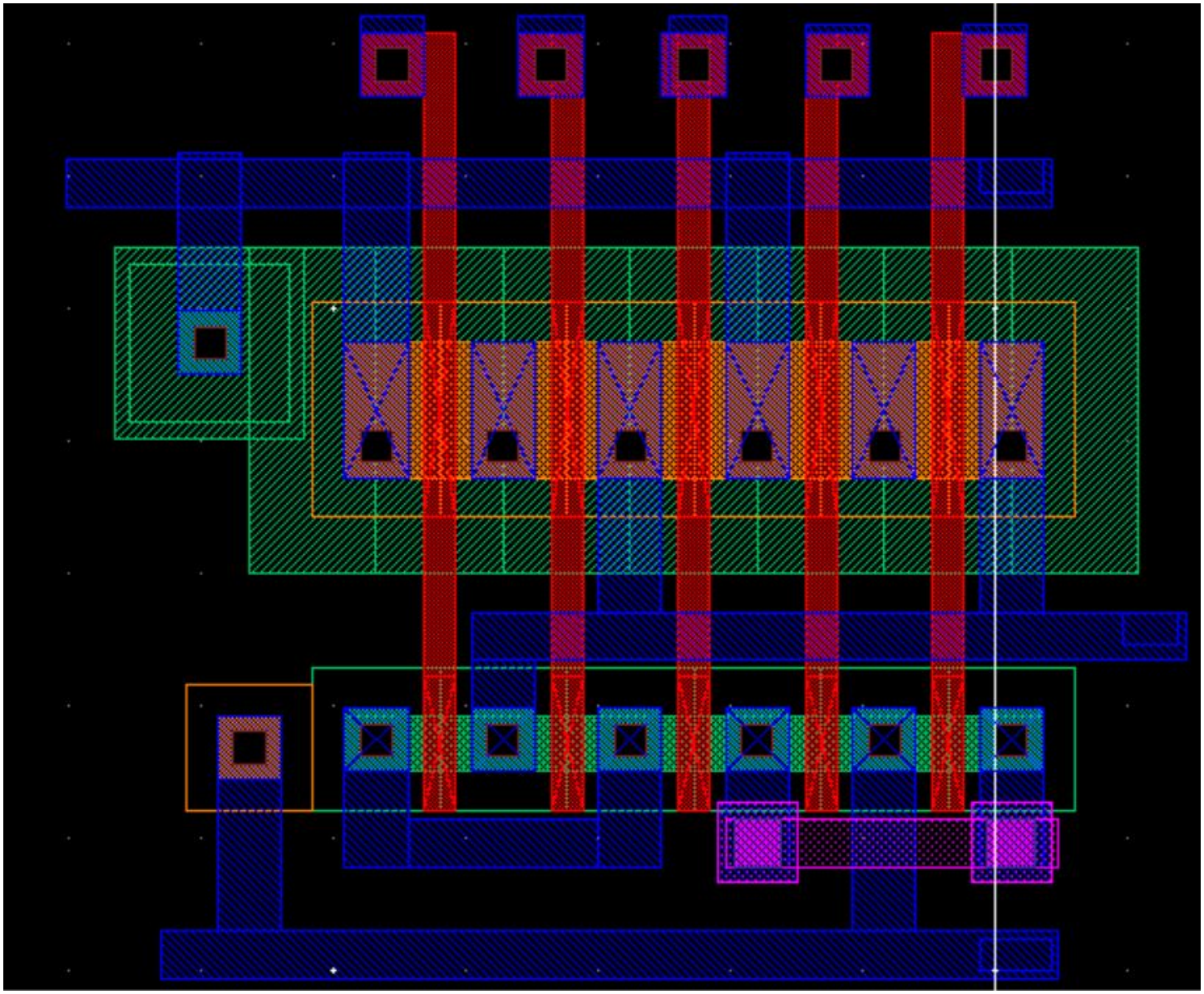
Schematic

Must size W/L? No because we don't care about the delay, just if the output is high or low. My attempt at sizing made the delays/rise and fall times of the output too slow and thus ambiguous.



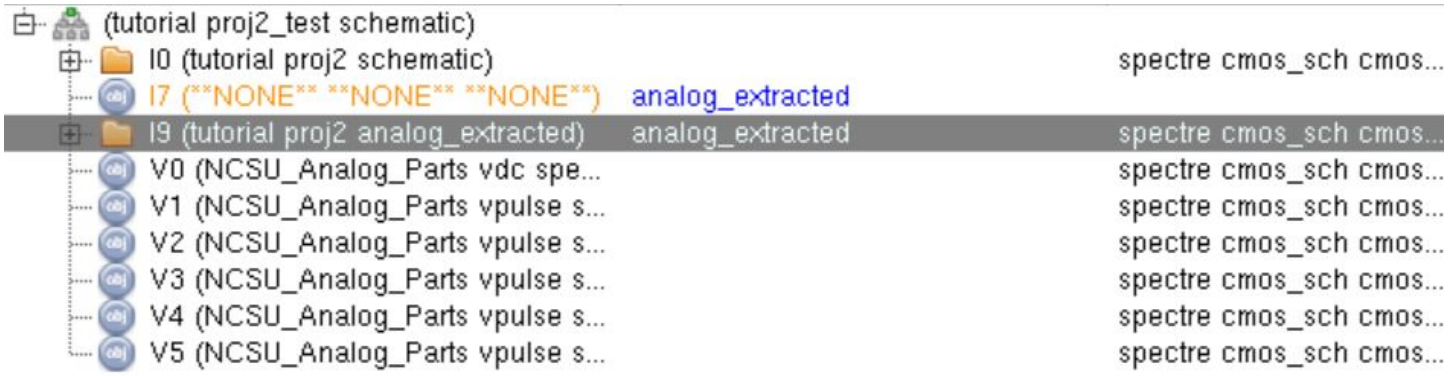
Layout

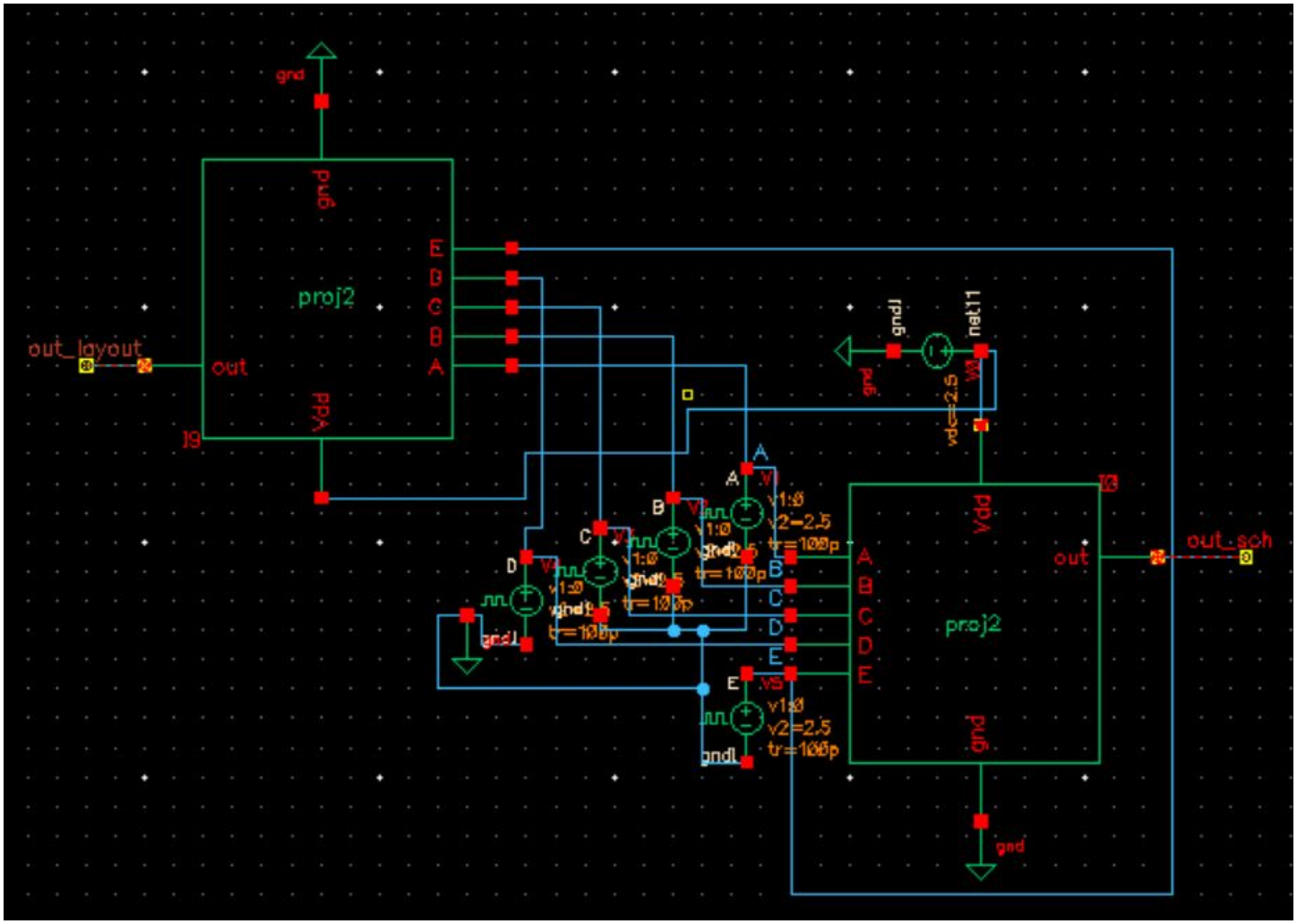
Notes: I used a metal 1 to metal 2 to bypass a metal 1 connection. The input pins are at the top because I could not find enough space to put them in between the networks. Only one bulk connection is needed for each diffusion layer/region. The diffusion regions are uninterrupted, there are just some unnecessary vias at two spots.



4.

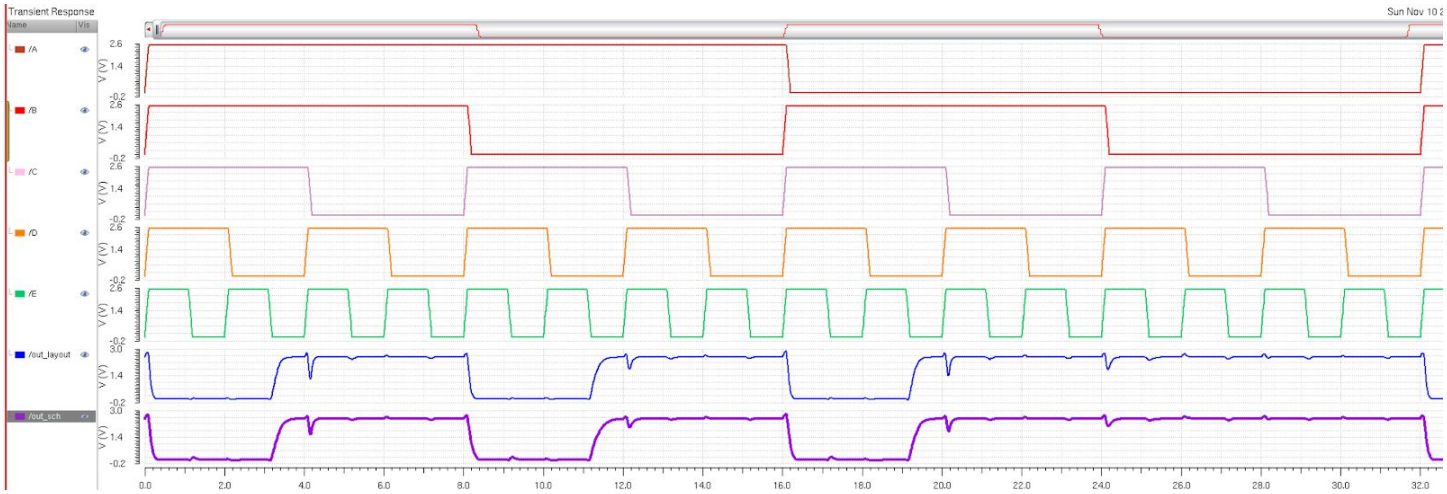
After extraction and LVS, the config view is used to change the test bench for the models.





The inputs are the circuits are vpulse. A has a pulse width and period of 16ns/32ns respectively, B is 8ns/16ns, C is 4ns/8ns, D is 2ns/4ns, E is 1ns/2ns. Thus we can cycle through the outputs in transient mode without having to manually assign values for the inputs.

The results are correct and manually checked as well. We can see that the outputs do have some delay but the circuit logic functions as expected. The rise and fall times are 100ps.



There is not too much difference between the analog extracted versus the schematic. The analog extracted behaves as expected with slower rise and slower drops due to the capacitors as shown below. The noise also comes from the inputs fall and rise times transitions.