EECS 119
Project 4
Report

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Overview:

For this project, our objective is to design and test a 4-bit BCD up/down counter. Like the project description states, depending on the value of the control (up/down) bit, the circuit follows one of the following two count sequences:

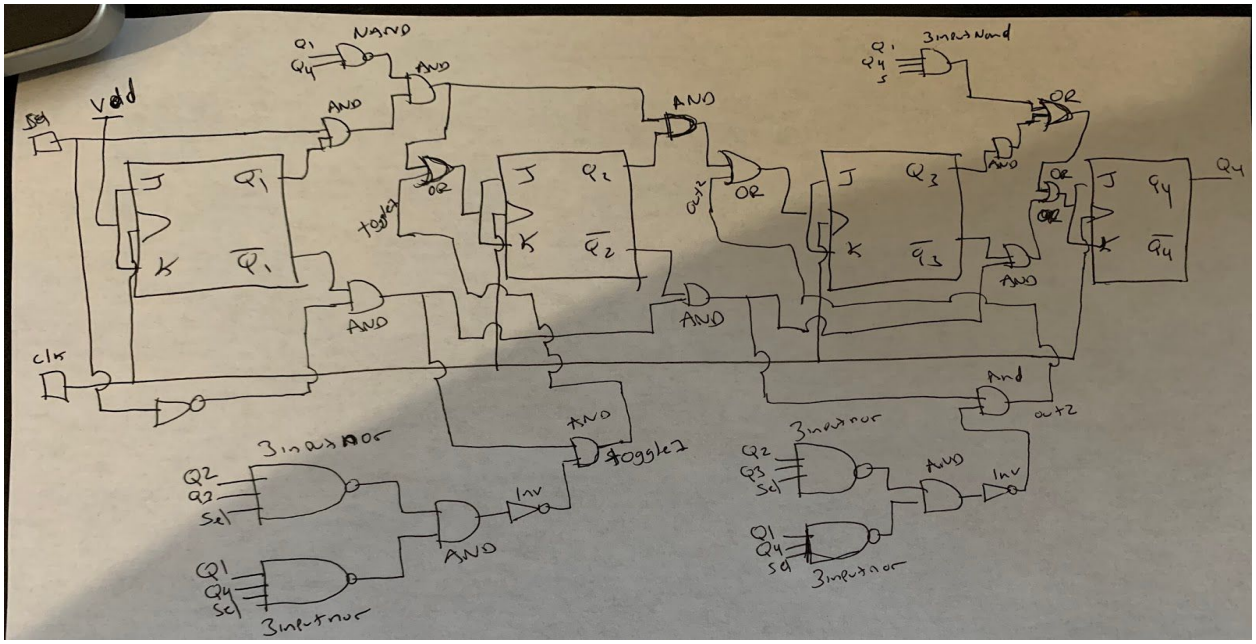
When s=1: 0000-0001-0010-0011-0100-0101-0110-0111-1000-1001-000

s=0: 1001-1000-0111-0110-0101-0100-0011-0010-0001-0000-1001

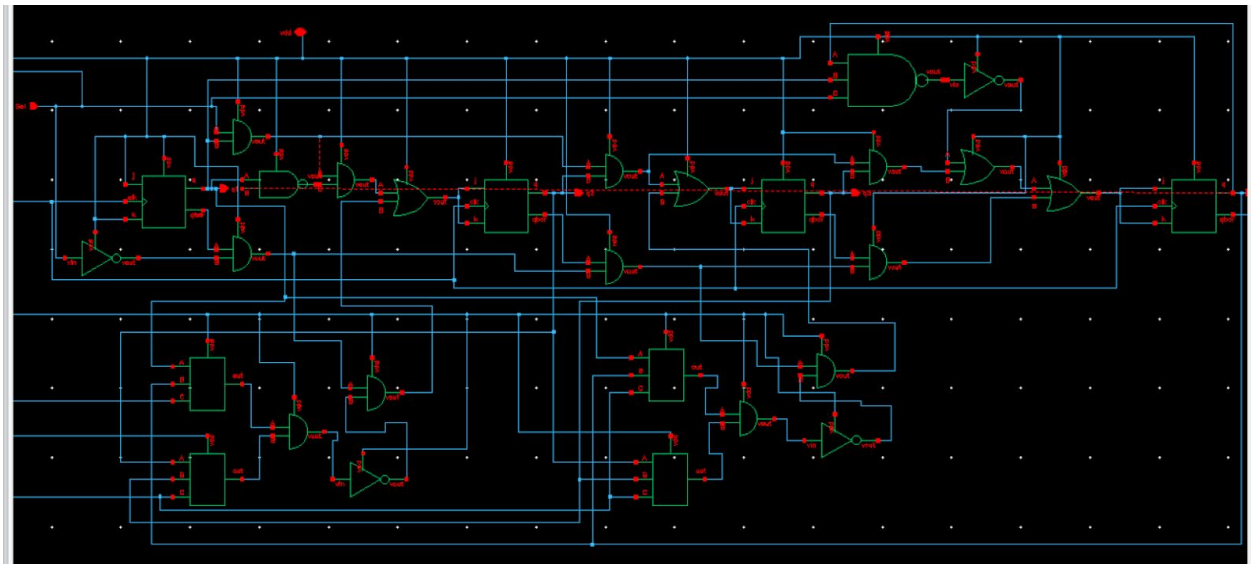
Design:

For our design of the circuit, we laid out all of the individual components necessary to assemble the circuit as a whole. This way, we're able to understand what each component is doing and how it contributes to the overall function of the 4-bit BCD up/down counter. In addition, we were able to start designing each component on Cadence and worked on combining them together as all of the parts were being finished. After designing each individual component we multiplied them and put it into the final design. The hard part would be to connect them all together. Below are each of the required components and the circuit schematics and layouts to make the 4-bit BCD

up/down counter:

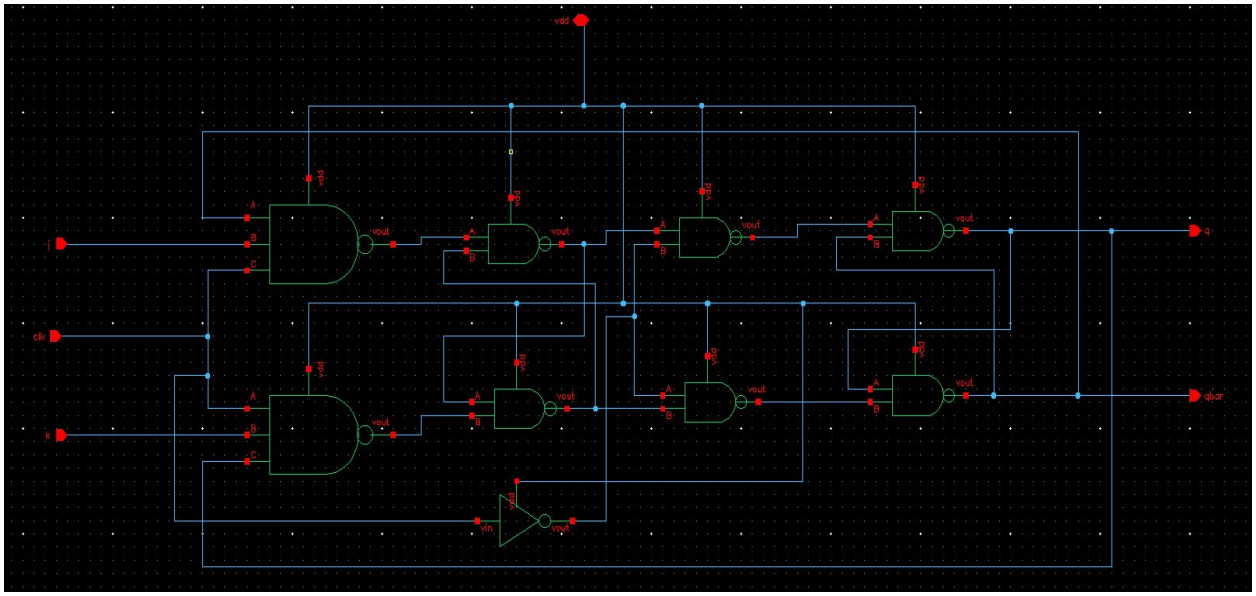


Up/down counter schematic:



We used JK flip flops with mux-like operations to have it stop counting up to 9 and counting down from 9. The components were chosen based on the bit table from 0-9,0 and 9-0,9. For down counter when Select bit is zero (counting down circuitry is enabled) and Q2=Q3=0 and Q1=Q4=0 bits q2 and q3 don't toggle. If select bit is high the circuitry for down counter is not enabled and up counter circuit is enabled.

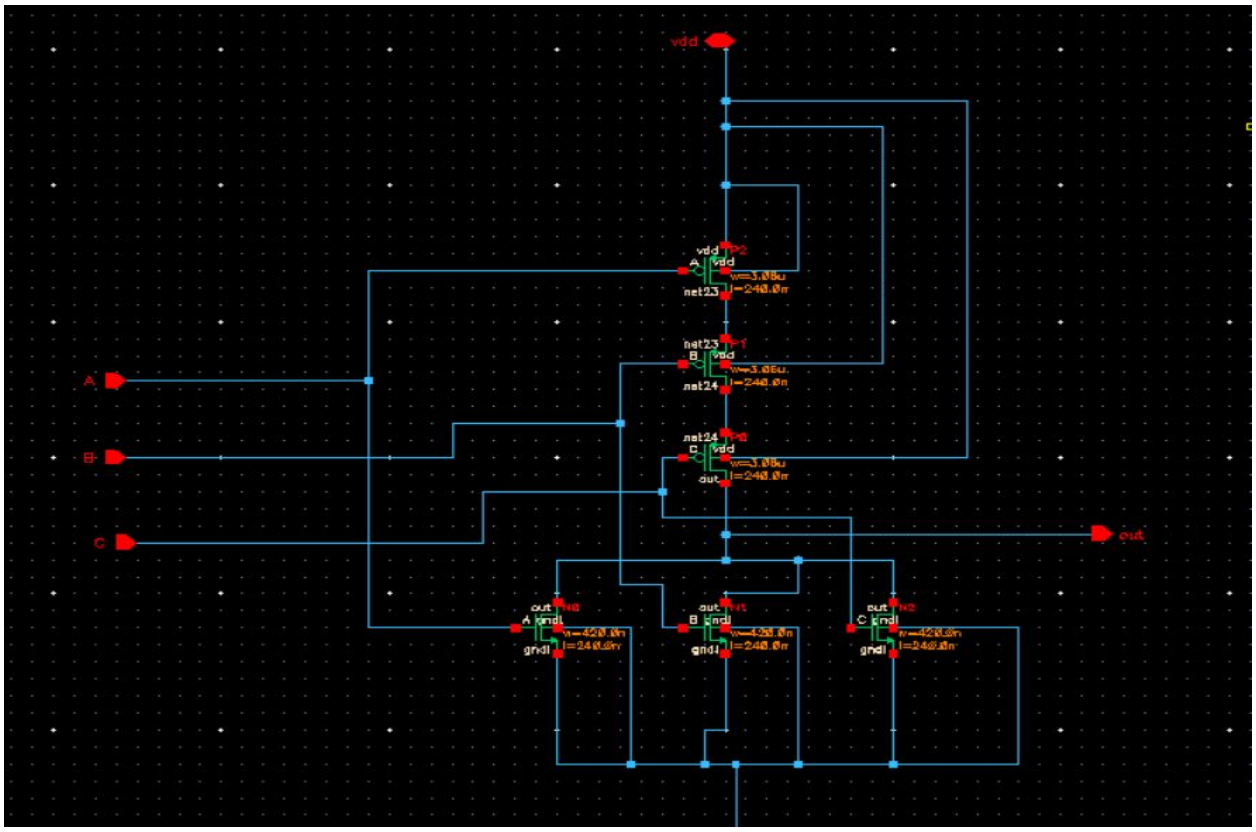
J/K Flip Flop Schematic:



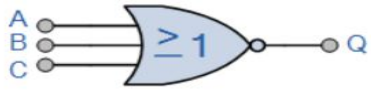
The Truth Table for the JK Function

	Clock	Input		Output		Description
	Clk	J	K	Q	$\overline{Q}$	
same as for the SR Latch	X	0	0	1	0	Memory no change
	X	0	0	0	1	
	⁻↓_	0	1	1	0	Reset Q » 0
	X	0	1	0	1	
	⁻↓_	1	0	0	1	Set Q » 1
	X	1	0	1	0	
toggle action	⁻↓_	1	1	0	1	Toggle
	⁻↓_	1	1	1	0	

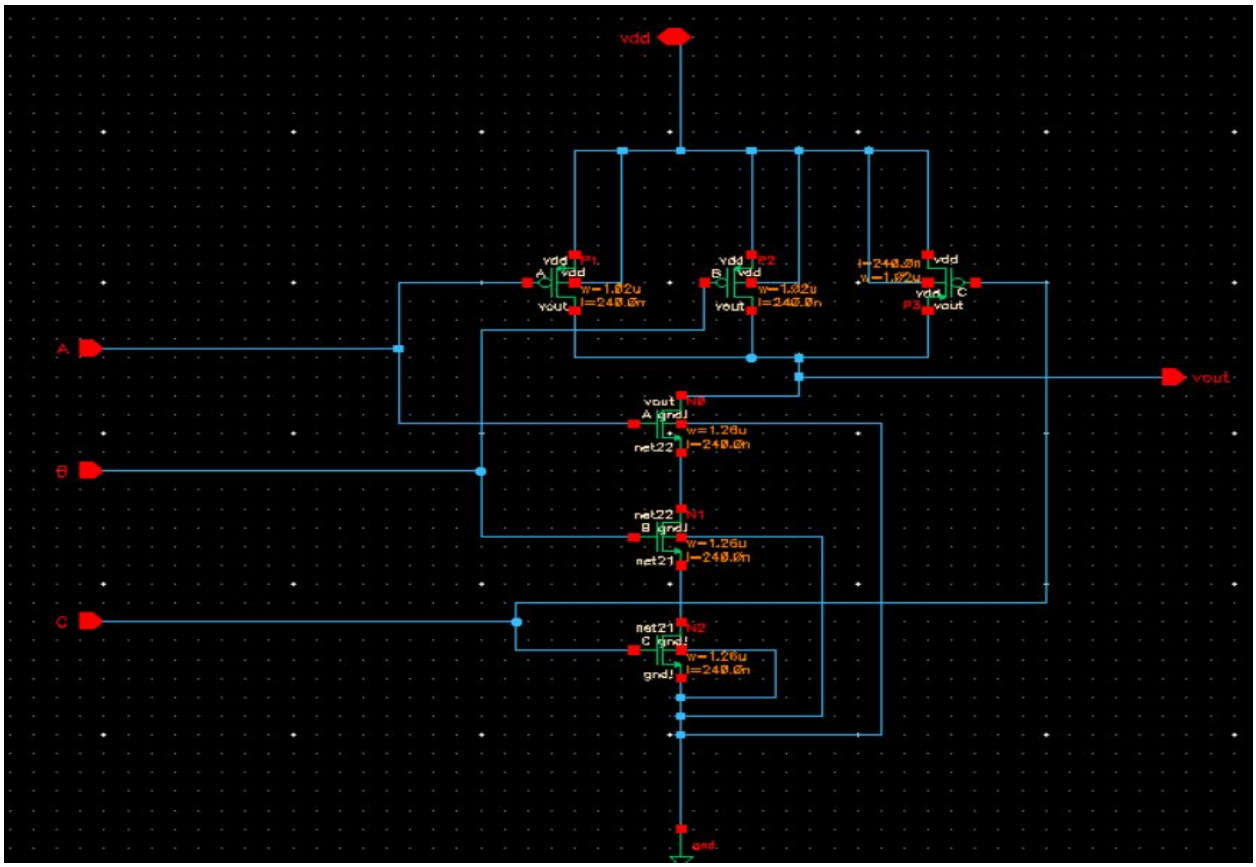
3-Input NOR Gate Schematic:



3-input NOR Gate

Symbol	Truth Table			
 3-input NOR Gate	C	B	A	Q
	0	0	0	1
	0	0	1	0
	0	1	0	0
	0	1	1	0
	1	0	0	0
	1	0	1	0
	1	1	0	0
	1	1	1	0
Boolean Expression $Q = \overline{A+B+C}$	Read as A **OR** B **OR** C gives **NOT** Q			

3-Input NAND Gate Schematic:



3-input Logic NAND Gate

Symbol	Truth Table			
 3-input NAND Gate	C	B	A	Q
	0	0	0	1
	0	0	1	1
	0	1	0	1
	0	1	1	1
	1	0	0	1
	1	0	1	1
	1	1	0	1
	1	1	1	0
Boolean Expression $Q = \overline{A.B.C}$	Read as A **AND** B **AND** C gives **NOT** Q			

Other gates used in the development of our Up/Down Counter were 2-input AND gate, 2-input OR gate, Inverter and a 2-input Nand gate, these gates were developed for project 3 and tested thoroughly in the development of project 3. Thus we omit their schematics and simulations in this report.

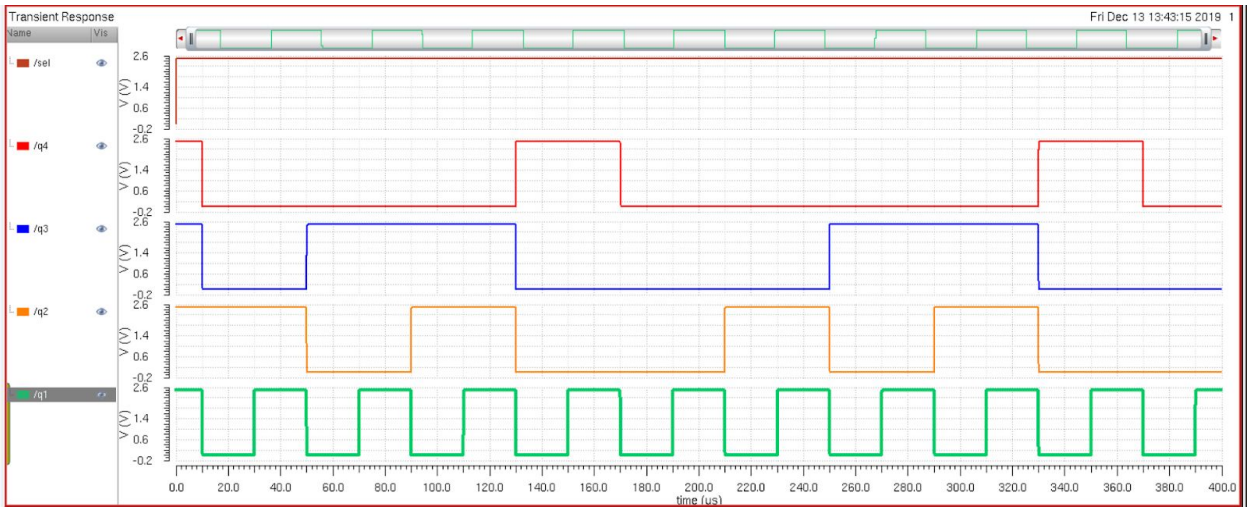
Simulation:

The clock must be pre charged(meaning that all the other inputs must be delayed), and we used V_{pulse} to vary all the inputs to get all possible combinations in one test. This means that there will be some delay time for waiting for the circuit to either count up or count down.

From 180-380.0 is when the up counter runs clearly 0-9-0 then for the down counter, it runs clearly from 9-0-9 starting at 460-630. Down count starts right when select goes low and around one cycle delay it gets to 9-0-9.

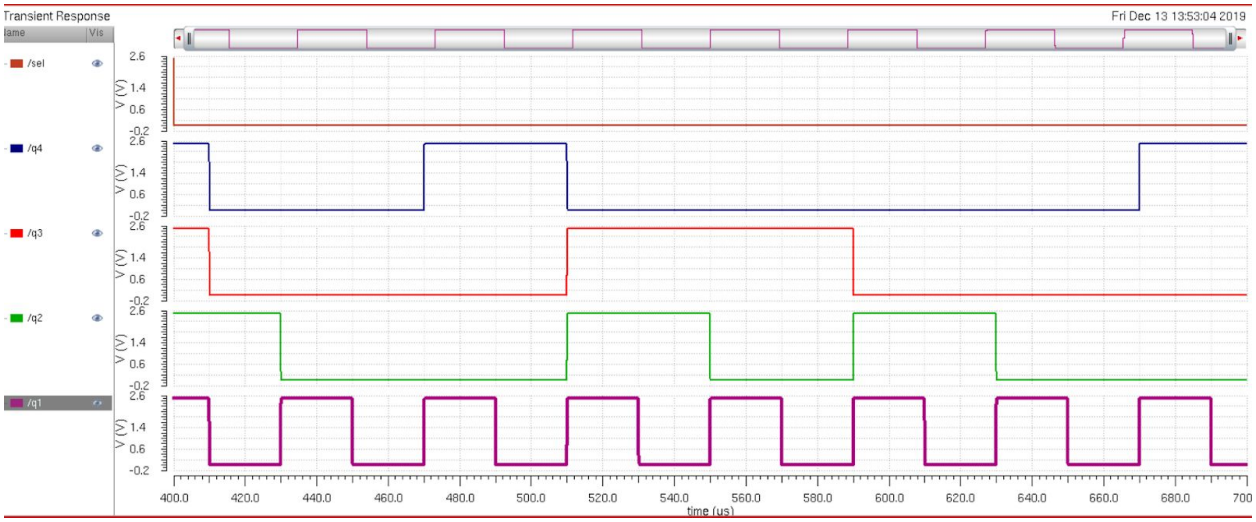
Up Counter Simulation:

The following timing diagram shows the up counter from 0-9-0 starting at 180.0 us up to 380 us.

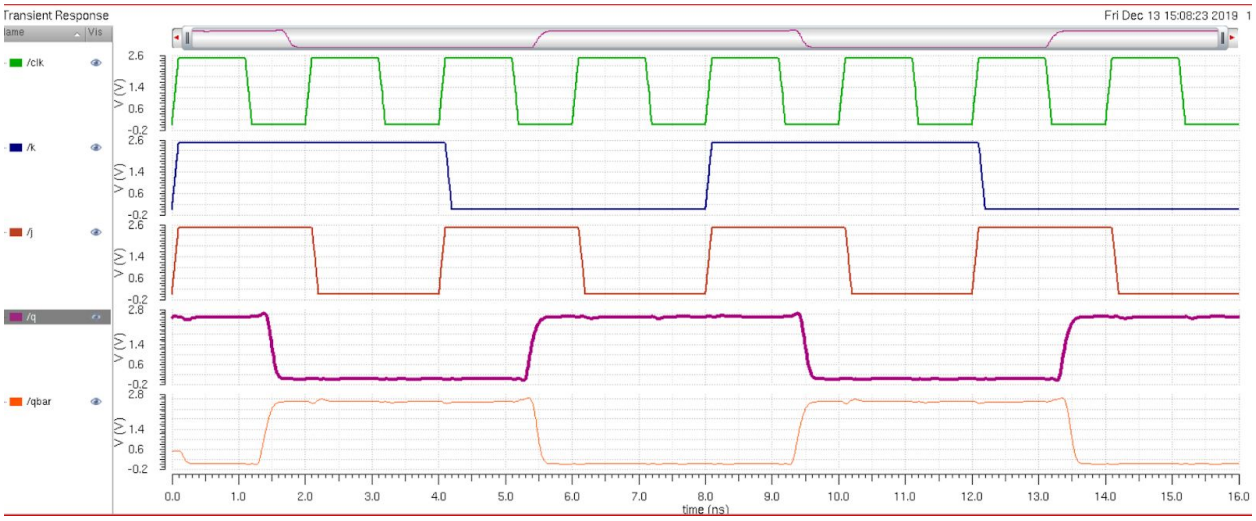


Down Counter simulation:

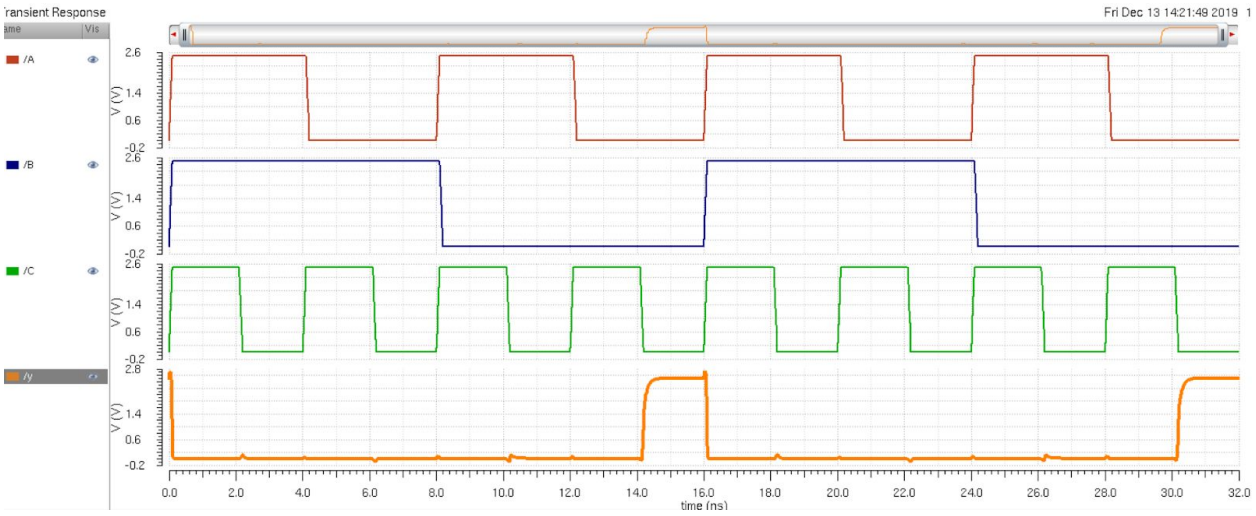
The following timing diagram shows down counter from 9-0-9 starting at 460.0 us up to 680.0 us.



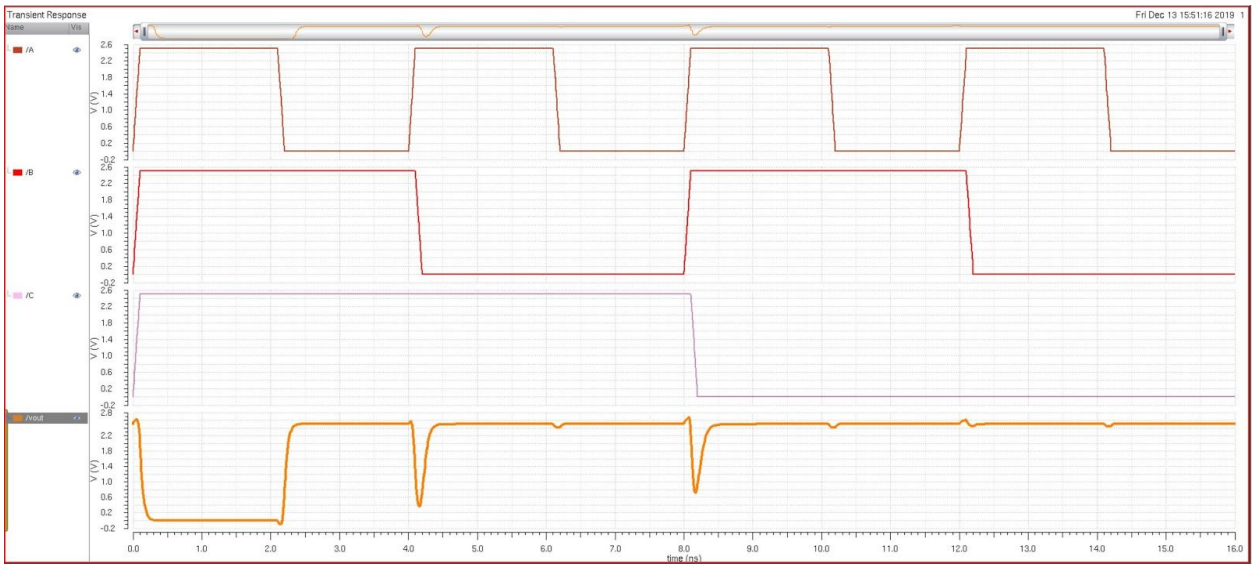
JK Flip Flop simulation:



3-input NOR Gate simulation:



3-input NAND Gate simulation:



Conclusion:

While we did not do the optional and time consuming layout, we were able to create and verify the schematic. It works properly with delays between SEL toggling for the clock to charge.