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## TUTORIAL 4636

# Avoid PC-Layout "Gotchas" in ISM-RF Products

By: Martin Stoehr, Principal Member of the Technical Staff, Applications

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*Abstract: RF products for industrial, scientific, and medical systems (ISM-RF) often feature very compact circuitry. To avoid common design pitfalls and "traps," the PC-board (PCB) layouts for these applications warrant careful attention. Operating in the various ISM frequency bands between 300MHz and 915MHz, these products include receivers and transmitters whose RF power levels range from -120dBm to +13dBm. Topics in the following discussion include inductor orientation, trace coupling, ground via problems, trace length issues, ground plane usage, crystal capacitance, and trace inductors.*

A similar article was published in the February 2011 issues of *Microwaves and RF Magazine*.

## Introduction

Extensive experience with industrial, scientific, and medical radio-frequency (ISM-RF) products has revealed the various pitfalls common to the layout of printed circuit boards (PCBs) for the products. It is not unusual to find significant variations in performance when the same IC is placed on two different circuit boards. Variations in the operating range, harmonic emissions, interference susceptibility, and startup time illustrate the role that layout can play in a successful design.

This article addresses various design oversights, explains why each error causes problems, and recommends how to avoid these traps. It assumes a two-layer PCB with FR-4 dielectric of 0.0625in thickness, and a ground plane on the bottom side of the board. Operating frequencies fall into various bands between 315MHz and 915MHz, with Tx and Rx power levels in the range -120dBm to +13dBm. **Table 1** lists some possible PCB layout problems, their causes, and their effects.



[Click here for an overview of the wireless components used in a typical radio transceiver.](#)

**Table 1. Typical PCB Layout Problems and Effects**

Problem	Cause	Effect
LNA/tank circuit arrangement (receiver)	Inductor orientation	RF feedthrough
Degeneration/ $\pi$ -network arrangement (transmitter)	Inductor orientation	RF feedthrough
Shared ground vias between legs of $\pi$ network	Via parasitics	Feedthrough, RF leakage
Shared ground vias between receiver blocks	Via parasitics	Crosstalk, RF feedthrough, RF leakage
Long traces for decoupling capacitors	Higher-impedance connections	Reduced decoupling
Wide component placement	Increased parasitics, ground loops	Detuning, crosstalk, feedthrough
Colinear traces in the transmitter circuit	Filter bypassing, i.e., power amplifier (PA) directly to antenna	Harmonics radiation
Top-layer copper pours	Parasitic coupling	RF leakage, RF interference
Discontinuous ground plane	Return current concentration	Crosstalk, feedthrough
Crystal connection trace length	Excess capacitance	LO frequency pulling
Crystal connection trace separation	Excess capacitance	LO frequency pulling
Ground plane under crystal pads	Excess capacitance	LO frequency pulling
Planar PCB trace inductors	Poor inductance control	Large footprint, low Q, crosstalk, feedthrough

Most of these problems derive from one of a few common causes. We will discuss each in turn.

## Inductor Orientation

Mutual inductance is present when two inductors (even two PC traces) are in proximity. Current in the first circuit induces a magnetic field that stimulates current in the second circuit (**Figure 1**). This process is similar to the action between primary and secondary windings in a transformer. When the two currents interact through the magnetic field, the resulting voltage is governed by the mutual inductance,  $L_M$ :

$$V_B (V) = L_M \frac{dI_A}{dt}$$

Where  $V_B$  is the injected error voltage in circuit B, and  $I_A$  is the forcing current in circuit A.<sup>1</sup> The value of  $L_M$  is highly sensitive to the distance between circuits, to the loop areas of the inductors (i.e., the magnetic flux), and to the orientation of the loops. Therefore, the best trade-off between circuit compactness and reduced coupling is to properly orient all the inductors.

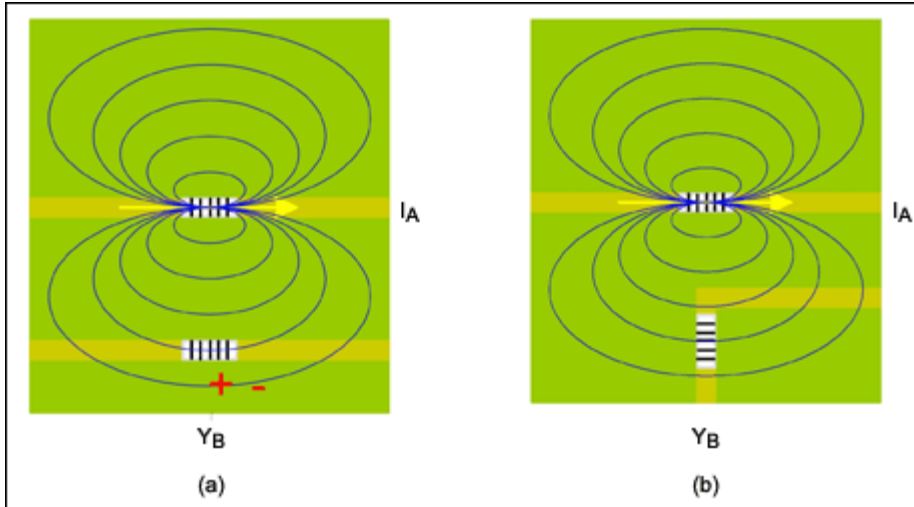


Figure 1. Magnetic field lines show the possibility of mutual inductance based on inductor orientation.

An optimal orientation positions circuit B so the plane of its current loop is parallel to the field lines of circuit A. To accomplish this goal, orient the inductors orthogonally whenever possible. Consider, for example, the circuit board of an evaluation (EV) kit ([MAX7042EVKIT](#)) for a low-power FSK superheterodyne receiver (**Figure 2**). Because the three inductors on this board (L3, L1, and L2) are in proximity, they are oriented at  $0^\circ$ ,  $45^\circ$ , and  $90^\circ$  to minimize their mutual inductance.

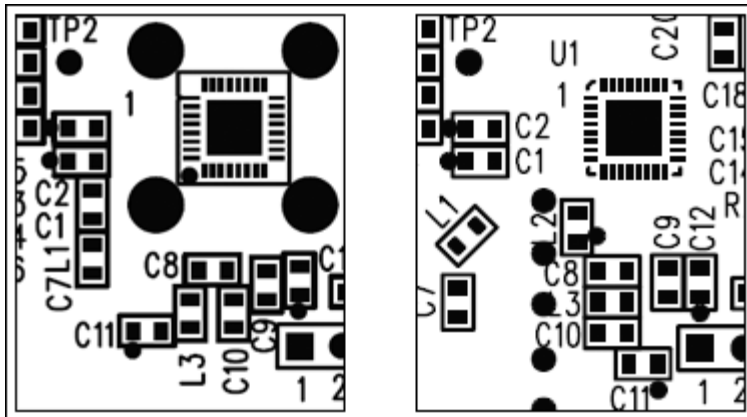


Figure 2. Two different PCB layouts are shown, one with poor component orientation (L1 and L3) and the other, preferable orientation.

In summary, therefore:

- Place inductors far apart when possible.
- Minimize inductor-circuit crosstalk by orienting the inductors at right angles.

## Trace Coupling

Just as inductor orientation can affect the coupling caused by magnetic fields, so too can individual traces if they are positioned too close together. This layout problem also creates what is typically called mutual inductance. Of greatest concern in an RF circuit are those traces associated with sensitive parts of the system, such as the input matching network, the tank circuit in a receiver, and the antenna matching network in a transmitter.

Routing a return current path close to the primary current path minimizes the radiated magnetic field. Such layouts reduce the area of the circuit loop. The ideal low-impedance path for return currents is usually a ground plane under the trace—a placement that effectively limits loop area to the thickness of the dielectric times the length of the trace. A split ground, however, increases the loop area (**Figure 3**). For traces passing over the split, the return current is forced to follow a higher-impedance path that effectively increases the area of the current loop. This layout also makes the trace more susceptible to the effects of mutual inductance.

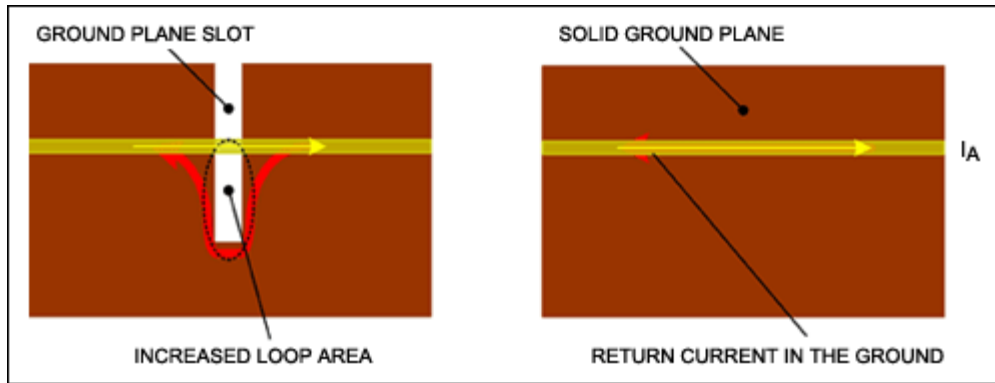


Figure 3. Solid ground planes are always a better choice.

As with physical inductors, the orientation of the traces plays a role in the coupling of magnetic fields. If it becomes necessary to run traces from sensitive circuits close to each other, it is preferable to run them in orthogonal directions to reduce coupling (**Figure 4**). If that cannot be achieved, then consider using a guard trace. Refer to the *Ground Planes and Copper Pours* section below for guidance on the design of guard traces.

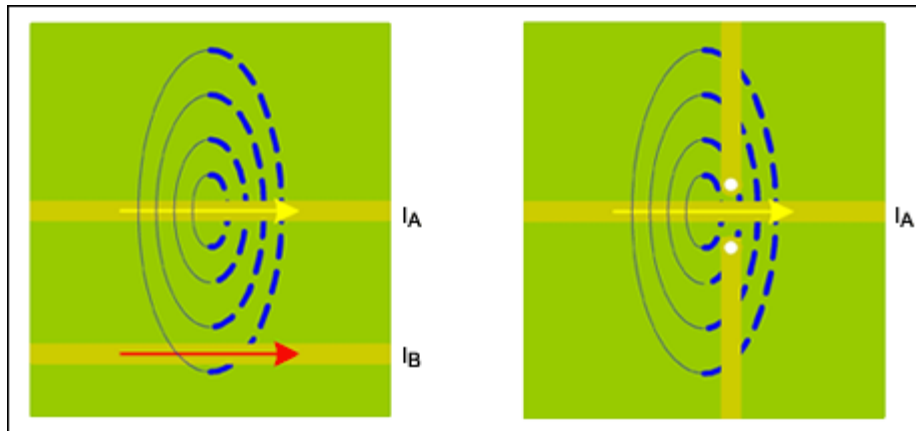


Figure 4. As in Figure 1, magnetic field lines show the possibility of coupling.

In summary, therefore:

- Always provide continuous grounds under traces.
- Orient sensitive traces orthogonally.
- If traces must be run in parallel, ensure adequate separation or use guard traces.

## Ground Vias

The primary cause of RF-layout problems can usually be traced back to nonideal circuit properties, both in the circuit components and in their interconnections. Thin traces act as inductive wires, and a trace

running over a copper plane or next to other traces forms a distributed capacitance with those structures. When it runs through a via, the trace tends to exhibit both inductive and capacitive properties.

Via capacitance comes primarily from the coplanar copper of the via pad and the ground plane, which are separated by a relatively small clearance ring. Secondary effects come from the cylindrical copper of the plated-through hole itself. The effect of parasitic capacitance is typically small, and usually causes only a slight degradation of signal edges in high-speed digital lines. (We are not concerned with those effects here.)

The largest parasitic impact from vias is simply the nonideal inductance exhibited by all interconnects. Because most plated-through hole structures in RF PCB designs tend to be the same size as lumped elements, a simple equation can estimate the influence of a circuit via (**Figure 5**):

$$L_{VIA} \text{ (nH)} = 5.08h \left[ \ln \left( \frac{4h}{d} \right) + 1 \right]$$

Where  $L_{VIA}$  is the lumped inductance of the via,  $h$  is the length of the via in inches, and  $d$  is the diameter of the via in inches.<sup>2</sup>

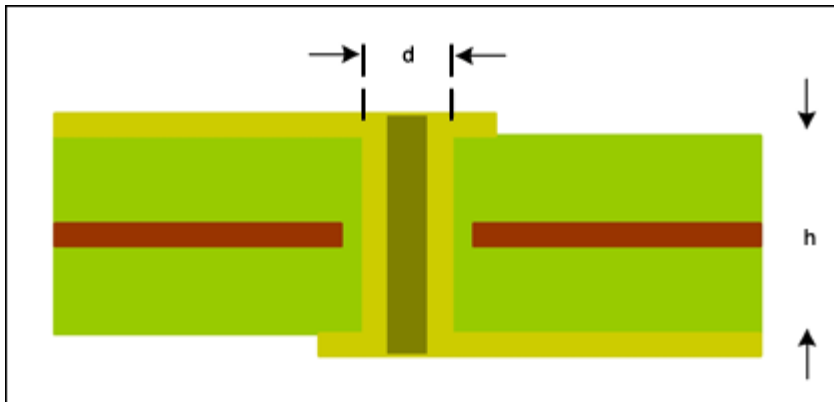


Figure 5. This cross section of a PC board shows the via structure used for estimating parasitics.

Parasitic inductance often has the greatest influence on bypass-capacitor connections. An ideal bypass capacitor provides a high-frequency short between power plane and ground plane, but nonideal vias reduce the low-inductance properties of both ground and power planes. The value of a typical PCB via ( $d = 10$  mils,  $h = 62.5$  mils) is about 1.34nH. Given the operating frequencies of ISM-RF products, vias can, therefore, cause unwanted effects in sensitive blocks such as tank circuits, filter blocks, and matching networks.

Other problems arise when ground vias are shared between sensitive portions of a circuit, such as the two legs of a  $\pi$  network. If you replace an ideal via with an equivalent lumped-element inductor, the resulting schematic looks much different than intended (Figure 6). Like the crosstalk from shared current paths,<sup>3</sup> the resulting increase in shared mutual inductance can greatly amplify crosstalk and feedthrough.

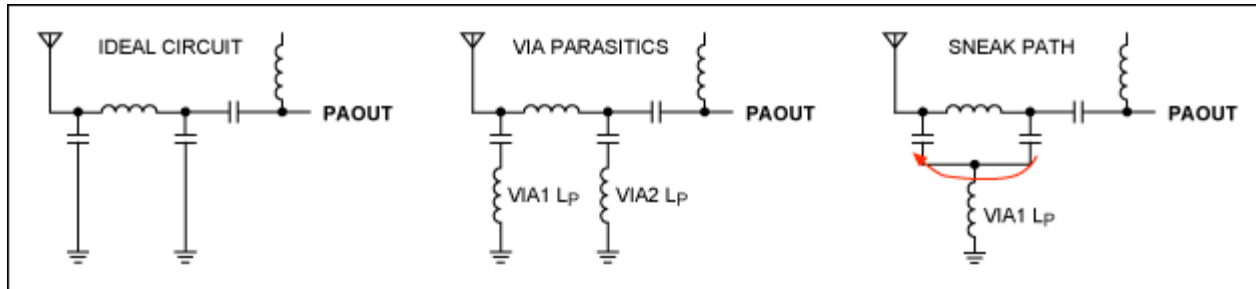


Figure 6. These ideal versus nonideal structures show the possibility of forming a "sneak path."

In summary, therefore:

- Be sure to model the inductance of vias in sensitive circuits.
- Use isolated vias for separate portions of a filter or matching network.
- Note that thinner PCBs reduce the influence of parasitic inductance in vias.

## Trace Lengths

Data sheets for Maxim ISM-RF products often recommend that the high-frequency input and output lines be kept as short as possible to minimize loss and radiation. Again, such loss is typically due to nonideal parasitic properties of the interconnections. Parasitic inductance and capacitance can both influence these circuit layouts, and they are best avoided by using short trace lengths. In general, a 10-mil-wide PCB trace, separated from the ground plane by 0.0625in of FR-4 dielectric, has about 19nH/in of inductance and 1pF/in of capacitance. For an LNA/mixer circuit that includes a 20nH inductor and 3pF capacitor, the proximity of circuit and device can greatly influence the effective component values.

Document IPC-D-317A from the Institute for Printed Circuits<sup>4</sup> provides an industry-standard equation for estimating various impedance parameters of a microstrip PCB trace. That document was superseded in 2003 by IPC-2251,<sup>5</sup> which provides more accurate calculations for various PCB traces. Online calculators are available from various sources, most of which base their equations on those found in IPC-2251. A useful reference for PCB trace-impedance calculations is available at the Missouri University of Science and Technology's Electromagnetic Compatibility Laboratory.<sup>6</sup>

The standard accepted equation for calculating the impedance of a microstrip trace is:

$$Z_0 (\Omega) = \frac{87}{\sqrt{\epsilon_r + 1.41}} \times \ln \left( \frac{5.98h}{0.8w + t} \right)$$

Where  $\epsilon_r$  is the permittivity of the dielectric substrate; h is the trace height above the ground; w is the trace width; and t is the trace thickness (**Figure 7**). This formula produces reasonably accurate results for w/h values between 0.1 and 2.0, and  $\epsilon_r$  values between 1 and 15.<sup>7</sup>

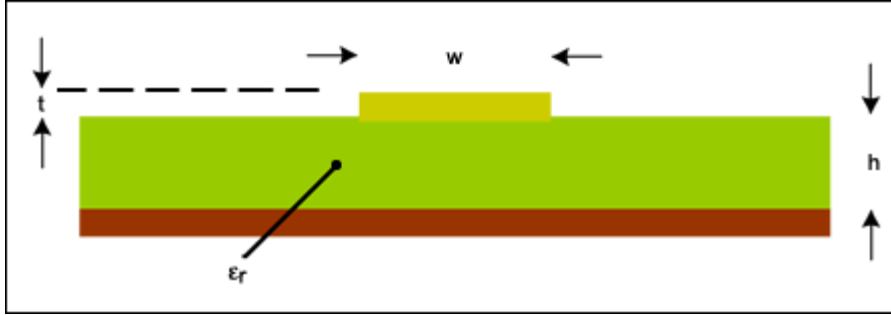


Figure 7. This PCB cross section (like Figure 5) shows the microstrip trace structure used for calculating impedance.

To estimate the effect of trace lengths, it is more useful to determine the detuning effect of trace parasitics on an ideal circuit. In this case we are concerned with stray capacitance and inductance. The standard equation for the characteristic capacitance of a microstrip trace is:

$$C_0 \text{ (pF/in)} = \frac{0.67(\epsilon_r + 1.41)}{\ln\left(\frac{5.98h}{0.8w + t}\right)}$$

Likewise, characteristic inductance from the equation  $Z_0 = \sqrt{\frac{L_0}{C_0}}$  can be calculated using results from the previous equations:

$$L_0 \text{ (nH/in)} = 0.001 \times Z_0^2 \times C_0$$

As an example, consider a PCB 0.0625in thick ( $h = 62.5$  mils) with 1-ounce copper traces ( $t = 1.35$  mils) 0.01in wide ( $w = 10$  mils) over FR-4 material. Note that  $\epsilon_r$  for FR-4 is typically 4.35 farads per meter (F/m), but it can range from 4.0F/m to 4.7F/m. The characteristic values calculated for this example are  $Z_0 = 134\Omega$ ,  $C_0 = 1.04\text{pF/in}$ , and  $L_0 = 18.7\text{nH/in}$ .

A trace length of 12.7mm (0.5in) is not unheard of in an ISM-RF layout, and such traces add about 0.5pF and 9.3nH of parasitics to the circuit (**Figure 8**). That level of parasitic interference on a receiver tank circuit contributes a variation in LC product close to 2% at 315MHz, and 3.5% at 433.92MHz. The extra capacitance and inductance due to trace parasitics can cause a 315MHz tank to peak at 312.17MHz, or a 433.92MHz tank to peak at 426.61MHz.

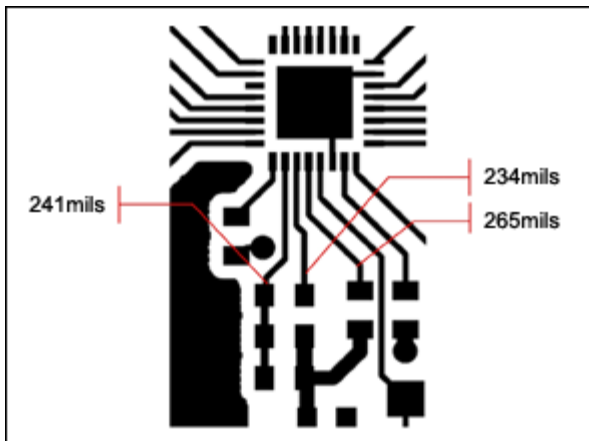


Figure 8. The parasitics of a compact PCB layout can exert influence on a circuit.

For another example, the tank circuit on a Maxim superheterodyne receiver ([MAX7042](#)) recommends component values of 1.2pF and 30nH at 315MHz, or 0pF and 16nH at 433.92MHz. Using the equation for tank circuit oscillation:

$$f_0 \text{ (Hz)} = \frac{1}{2\pi\sqrt{LC}}$$

You can calculate that the 315MHz tank-circuit values implemented on the EV kit already incorporate package and layout parasitics of about 7.3pF and 7.5pF, respectively. Note that the LC product is expressed as a lumped capacitance.

In summary, therefore:

- Keep trace lengths to a minimum.
- Start the layout with critical circuits as close to the device as possible.
- Compensate critical component values for actual layout parasitics.

## Ground Planes and Copper Pours

A ground or power plane defines a common reference voltage and provides that voltage to all parts of the system through a low-impedance connection. In doing so the plane equalizes any electric fields, and thus acts as a good shielding mechanism as well.

DC currents always follow the path of least resistance. Similarly, high-frequency currents always follow the path of least impedance. Thus, for a standard PCB microstrip trace over a ground plane, the return current tries to flow in the area of ground plane just below the trace itself. As noted in the *Trace Coupling* section above, interrupting a ground plane can induce various forms of noise, thereby increasing crosstalk effects through magnetic coupling or by concentrating the current (**Figure 9**).

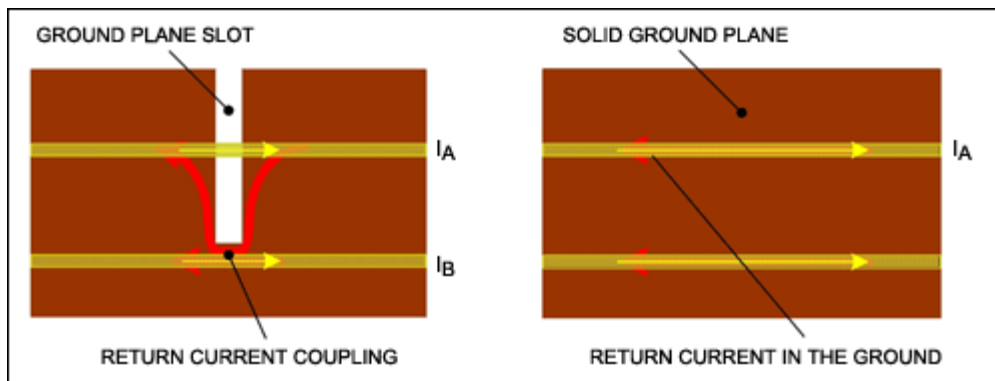


Figure 9. Keep the ground planes solid. Those return currents can cause crosstalk.

Copper pours, also called guard traces, are used where a continuous ground is difficult to implement or where you need to shield sensitive parts of a circuit (**Figure 10**). You can increase the shielding effect of a copper pour by tying the trace to ground at both ends and at multiple locations along its length (i.e., via "stitching").<sup>8</sup> Use caution not to mix guard traces with traces intentionally designed to provide return currents, because that arrangement can cause unwanted crosstalk.



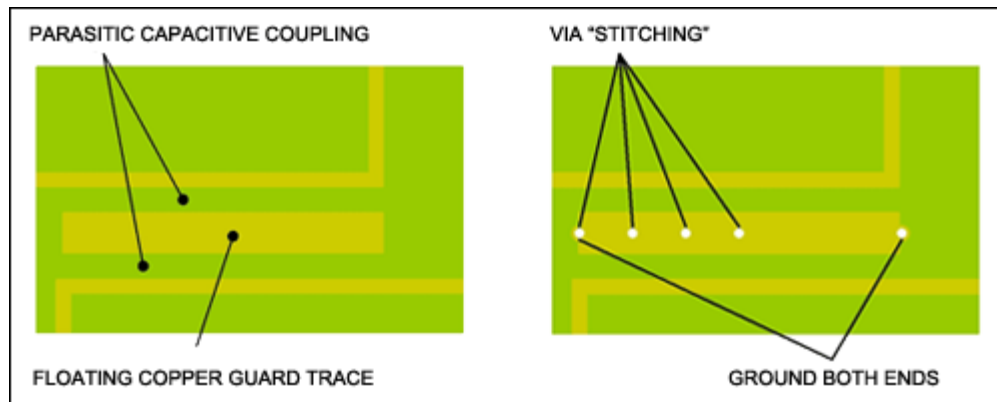


Figure 10. Avoid floating copper in an RF system, and use caution when a fabricator requests the addition of copper thieving structures.

Not grounding a copper pour at all (floating copper) or tying it to ground at only one end can have limited benefit. In some cases, it creates parasitic capacitance that can have a detrimental effect by changing the impedance of nearby traces or acting as an unwanted "sneak" path between portions of a circuit. A common request to manufacturing is that floating copper be placed on a board to provide "copper thieving." Restated simply, the non-circuit copper is added by a fabricator to help ensure a consistent electroplating thickness. These floating copper areas should be avoided because they can interfere with the schematic design.

Finally, be sure to consider the effect of any ground plane near an antenna. Any monopole antenna will regard ground planes, traces, and vias as parts of the counterpoise, and nonideal counterpoise shapes can influence the antenna's radiation efficiency and directionality (radiation pattern). A ground plane, therefore, should not be placed directly under a monopole PCB trace antenna.

In summary, therefore:

- Provide a continuous, low-impedance ground plane whenever possible.
- Ground both ends of copper pours, and stitch vias if possible.
- Do not float copper near the RF circuitry, and do not use copper thieving near the RF circuitry.
- If the board includes multilayer ground planes, provide a ground via wherever the signal trace makes a transition from one side of the plane to the other.

## Excessive Crystal Capacitance

Parasitic capacitance can pull the operating frequency of a crystal oscillator off target.<sup>9</sup> You should, therefore, follow general guidelines to reduce any stray capacitance on the crystal leads, the solder pads, the traces, or the connection to the RF device.

In summary, therefore:

- Use short traces between the crystal and the RF device.
- Keep interconnect traces separated as much as possible.
- If you suspect excessive shunt capacitance, vacate the ground plane under the crystal.

## Planar Trace Inductors

The use of planar trace or PCB spiral inductors is strongly discouraged. The inaccuracies inherent in a typical PCB manufacturing process, such as the width and space tolerances, can greatly affect accuracy of the component value. As a rule, the most controlled and highest-Q inductors are the wirewound variety.

Next are the ceramic-layer inductors typically manufactured by the same companies that produce ceramic multilayer chip capacitors. Nevertheless, some designers must use a spiral trace inductor as a last resort. The standard for calculating the inductance of a planar spiral inductor comes from the classic Wheeler equation:<sup>10</sup>

$$L (\mu\text{H}) = \frac{(a^2 \times n^2)}{(8a + 11c)}$$

Where  $a$  is the average radius of the coil in inches,  $n$  is the number of turns, and  $c$  is the width of the winding core ( $r_{\text{OUTER}} - r_{\text{INNER}}$ ) in inches. For coils with  $c > 0.2a$ ,<sup>11</sup> this calculation is accurate to within 5%.

Many modifications apply when using square, hexagonal, and other shapes for producing a single-layer spiral inductor. A good approximation has been developed for modeling planar inductors on integrated circuit wafers. For that purpose, a modified version of the standard Wheeler equation works well for small geometries and square dimensions:<sup>12</sup>

$$L_{\text{MW}} (\text{H}) = K_1 \times \mu_0 \times \frac{(n^2 \times d_{\text{AVG}})}{(1 + K_2 \times \rho)}$$

Where  $\rho$  is the fill ratio  $\rho = \frac{(d_{\text{OUT}} - d_{\text{IN}})}{(d_{\text{OUT}} + d_{\text{IN}})}$ ,  $n$  is the number of turns,  $d_{\text{AVG}}$  is the average diameter

$d_{\text{AVG}} = \frac{(d_{\text{OUT}} - d_{\text{IN}})}{2}$ , and (for a square spiral)  $K_1 = 2.36$  and  $K_2 = 2.75$ .<sup>13</sup>

The reasons to avoid this form of inductor are numerous. They are typically limited to low-inductance values due to space constraints. The most critical reason to avoid trace inductors is that their small geometry and poor control of critical dimensions often results in an unpredictable inductance value. Other reasons to avoid these PC inductors are no testability by the PCB fabricator for actual inductance values, and a tendency for the inductor to couple noise to other parts of the circuit (see the *Trace Coupling* section above).

In summary, therefore:

- Avoid the use of planar trace inductors.
- Use wire-wound inductors whenever possible.

## Conclusion

As discussed above, a few common PCB layout traps can create problems in an ISM-RF design. You can avoid many of these pitfalls, however, with careful attention to the circuit's nonideal properties. Compensating for these unwanted effects requires a proper treatment of seemingly minor items, such as component orientation, trace length, via placement, and ground plane usage. Following the guidelines above, you can save significant time and money that might otherwise be wasted on correcting mistakes.

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