Nombre: Brayan Ramirez Benítez

Boleta: 2020630592 = 206359

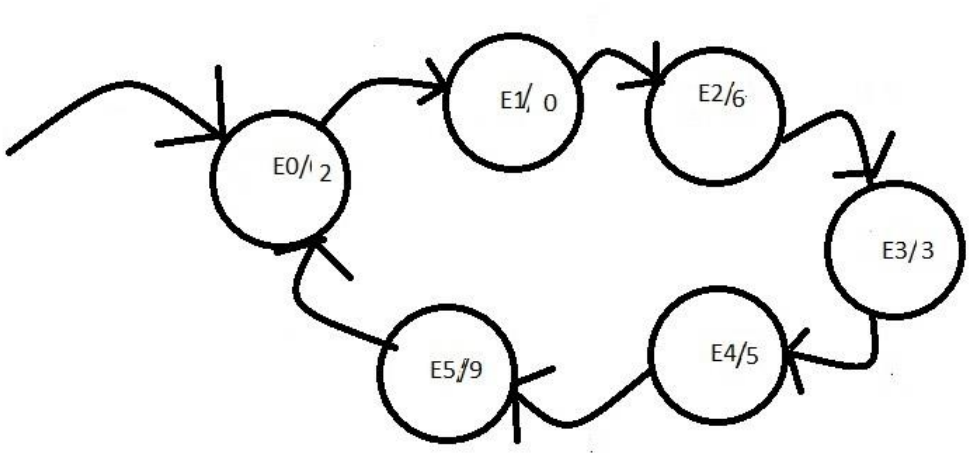
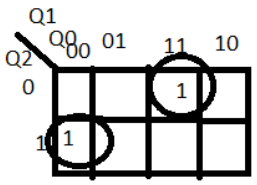


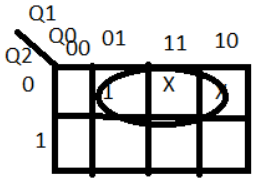
Diagrama de Estados

Estado	Salida	Secuencial	Display
E0	2	000	1101101
E1	0	001	1111110
E2	6	010	1011111
E3	4	011	1111001
E4	5	100	1011011
E5	9	101	1110011

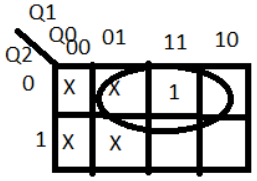
Estado Actual			Estado Siguiente			Diseño			
Q2	Q1	Q0	Q2*	Q1*	Q0*	D	J	K	T
0	0	0	0	0	1	0	0	X	1
0	0	1	0	1	0	0	1	x	1
0	1	0	0	1	1	0	X	0	1
0	1	1	1	0	0	1	x	1	1
1	0	0	1	0	1	1	0	X	1
1	0	1	0	0	0	0	0	X	1



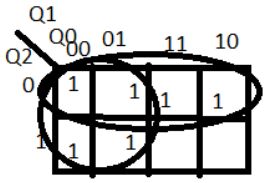
D = Q2'Q1Q0 + Q2Q1'Q0'



J = Q2'Q0

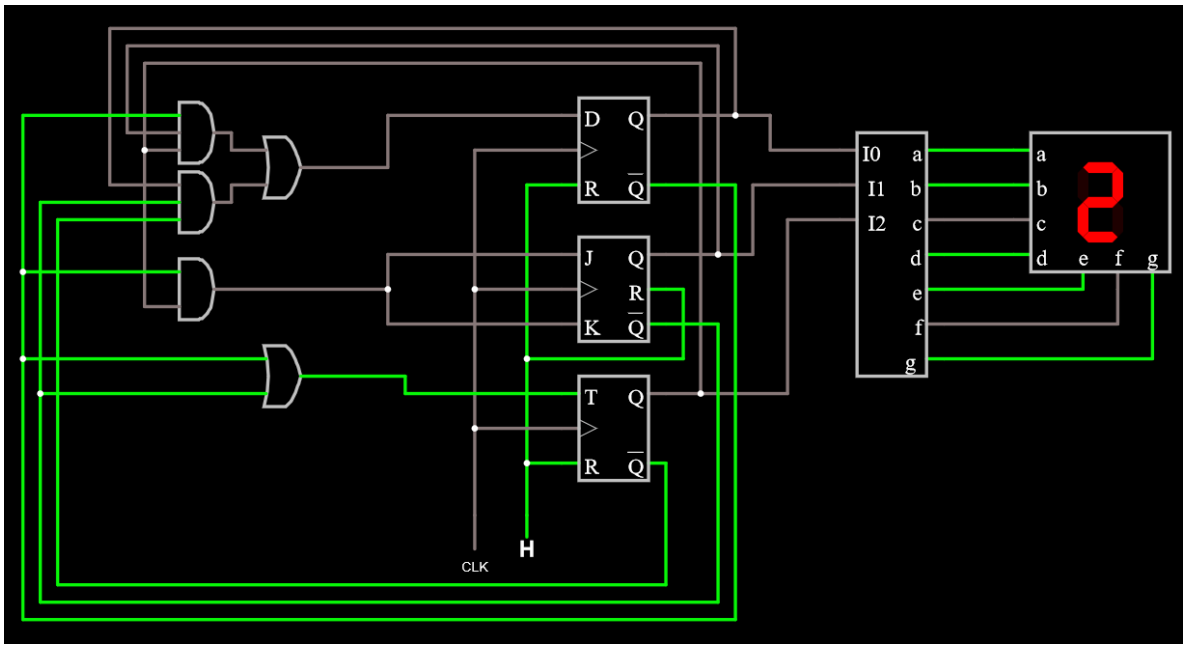


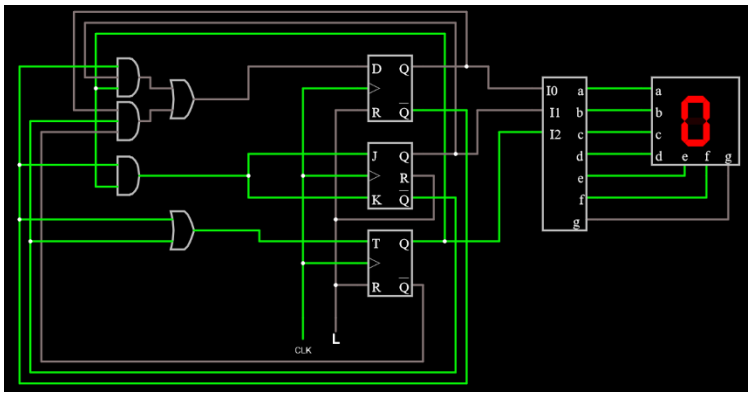
K = Q2'Q0

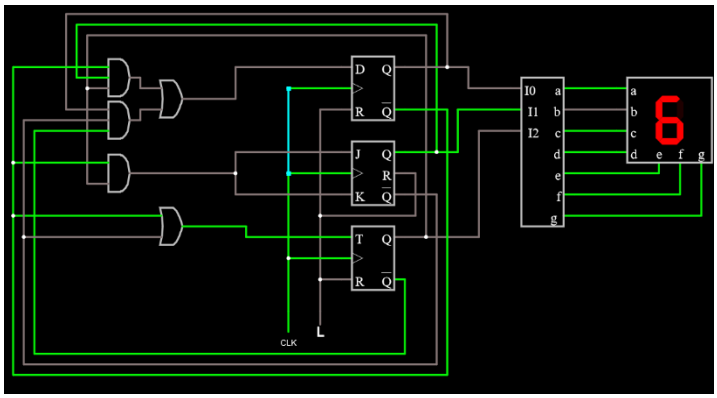


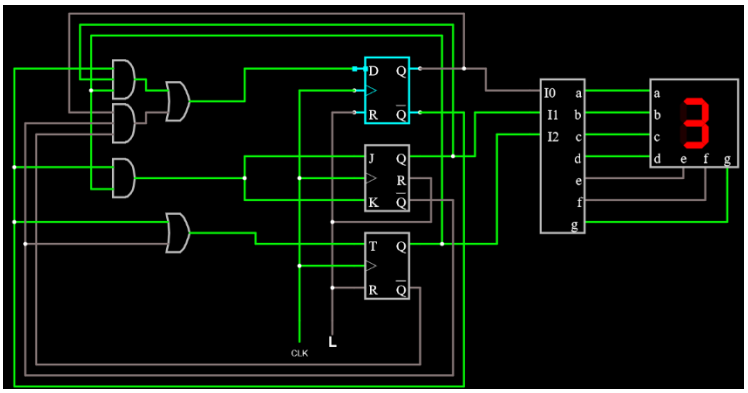
T = Q2' + Q1'

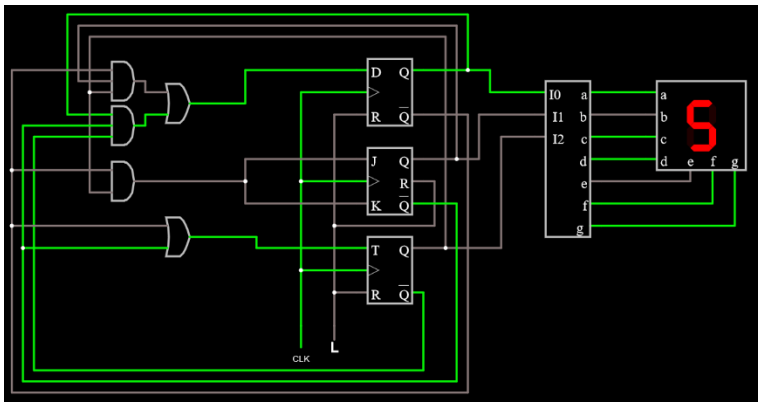
Link: https://tinyurl.com/y8feyb8j

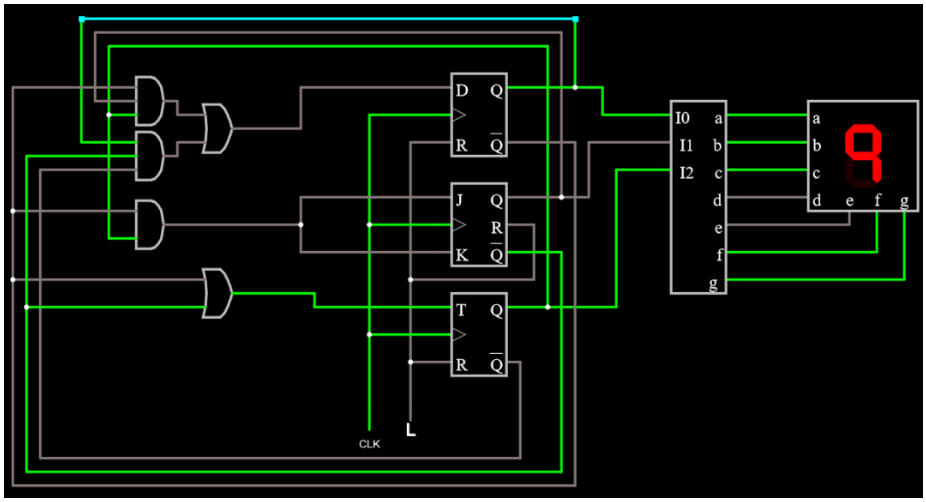



D Q
R Q
J Q
K R Q
T Q
R Q
CLK
L
I0 a
I1 b
I2 c
d
e
f
g
a
b
c
d e f g
0

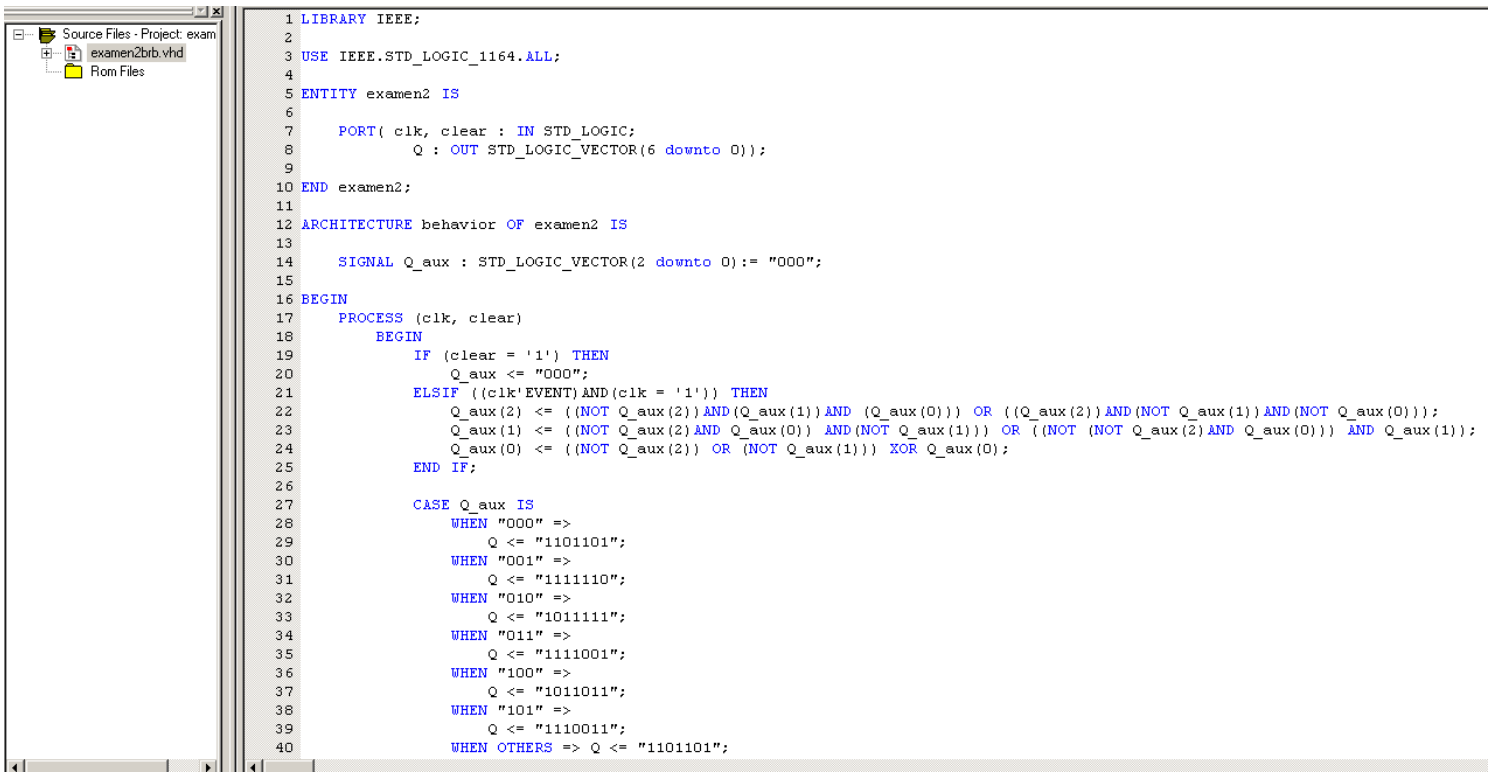

D Q
R Q
J Q
K R Q
T Q
R Q
CLK
L
I0 a
I1 b
I2 c
d
e
f
g
a
b
c
d e f g
6


D Q
R Q
J Q
K R Q
T Q
R Q
CLK
L
I0 a
I1 b
I2 c
d
e
f
g
a
b
c
d e f g
3

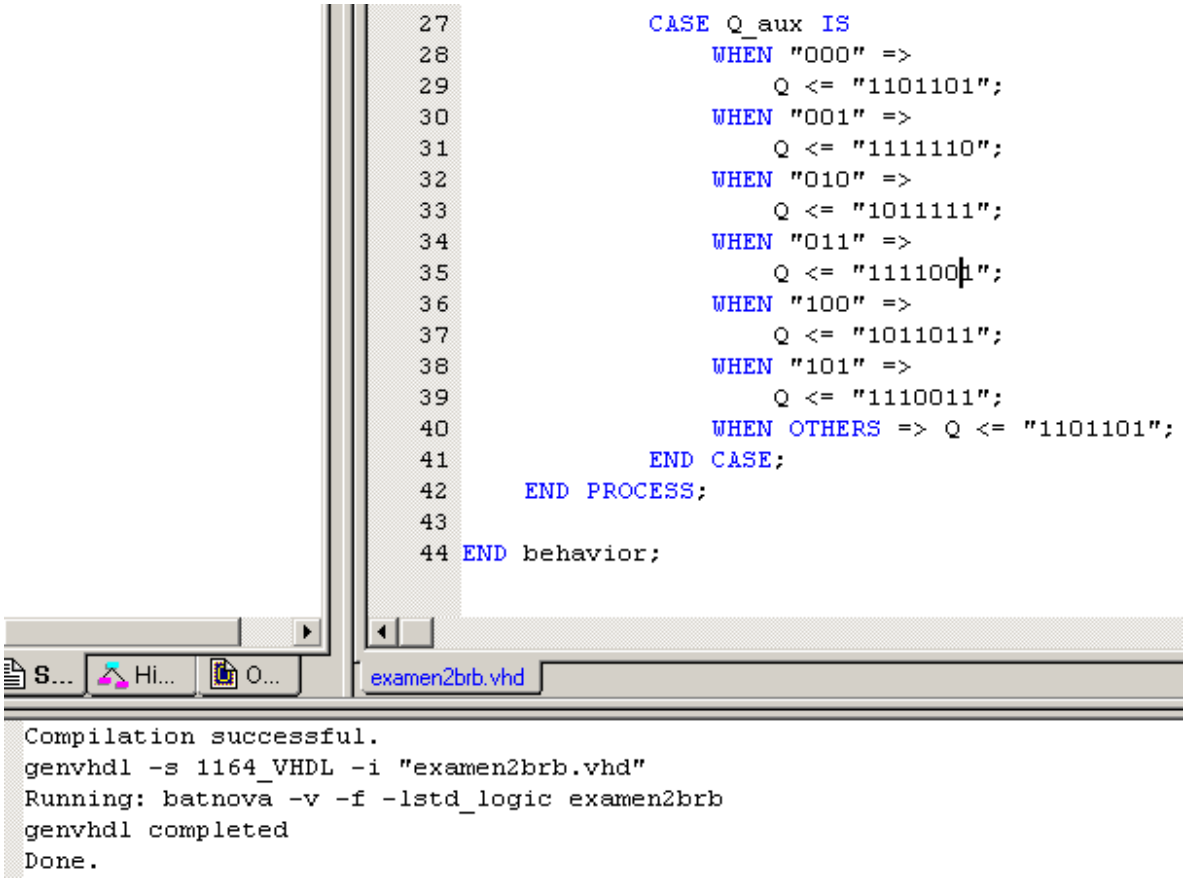

D Q
R Q
J Q
K R Q
T Q
R Q
CLK
L
I0 a
I1 b
I2 c
d
e
f
g
a
b
c
d e f g
5


D Q
R Q
J Q
K R Q
T Q
R Q
CLK
L
I0 a
I1 b
I2 c
d
e
f
g
a
b
c
d e f g
9

Código y simulación



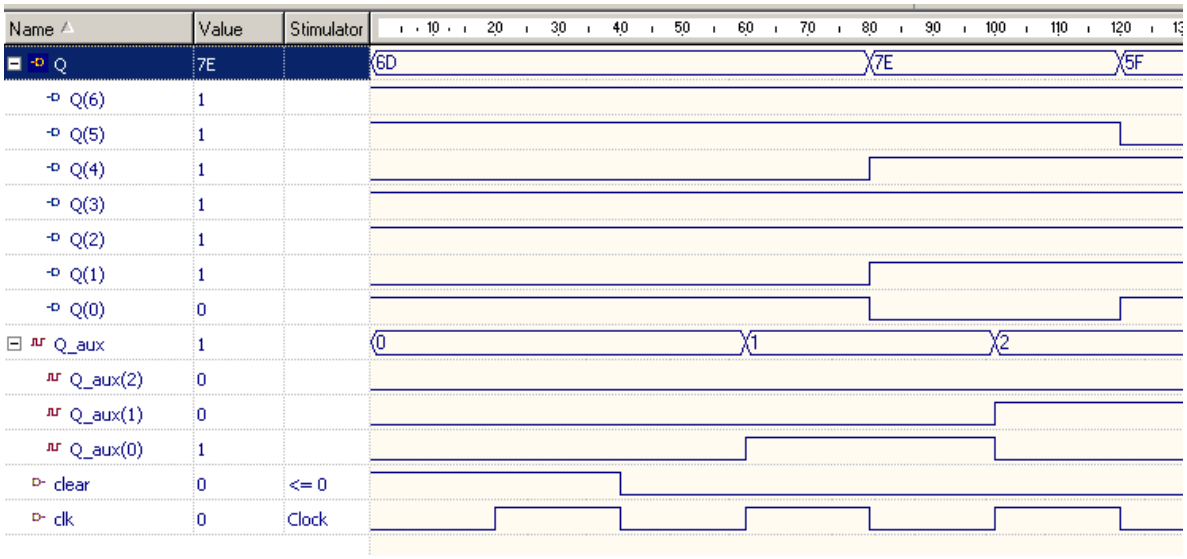

```
LIBRARY IEEE;

USE IEEE.STD_LOGIC_1164.ALL;

ENTITY examen2 IS

    PORT( clk, clear : IN STD_LOGIC;
          Q : OUT STD_LOGIC_VECTOR(6 downto 0));

END examen2;

ARCHITECTURE behavior OF examen2 IS

    SIGNAL Q_aux : STD_LOGIC_VECTOR(2 downto 0):= "000";

BEGIN
    PROCESS (clk, clear)
        BEGIN
            IF (clear = '1') THEN
                Q_aux <= "000";
            ELSIF ((clk'EVENT)AND(clk = '1')) THEN
                Q_aux(2) <= ((NOT Q_aux(2))AND(Q_aux(1))AND (Q_aux(0))) OR ((Q_aux(2))AND(NOT Q_aux(1))AND(NOT Q_aux(0)));
                Q_aux(1) <= ((NOT Q_aux(2)AND Q_aux(0)) AND(NOT Q_aux(1))) OR ((NOT (NOT Q_aux(2)AND Q_aux(0))) AND Q_aux(1));
                Q_aux(0) <= ((NOT Q_aux(2)) OR (NOT Q_aux(1))) XOR Q_aux(0);
            END IF;

            CASE Q_aux IS
                WHEN "000" =>
                    Q <= "1101101";
                WHEN "001" =>
                    Q <= "1111110";
                WHEN "010" =>
                    Q <= "1011111";
                WHEN "011" =>
                    Q <= "1111001";
                WHEN "100" =>
                    Q <= "1011011";
                WHEN "101" =>
                    Q <= "1110011";
                WHEN OTHERS => Q <= "1101101";
```

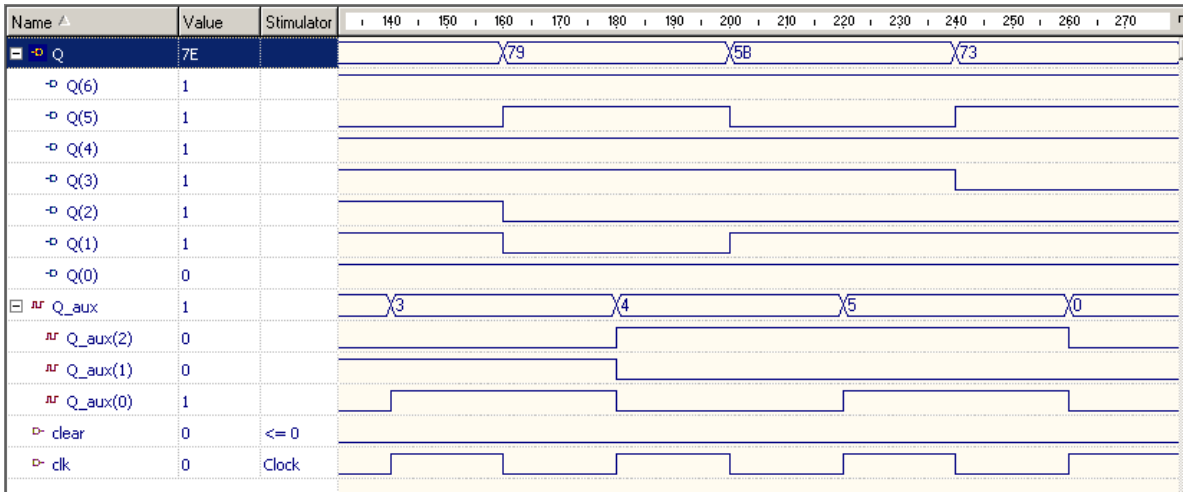


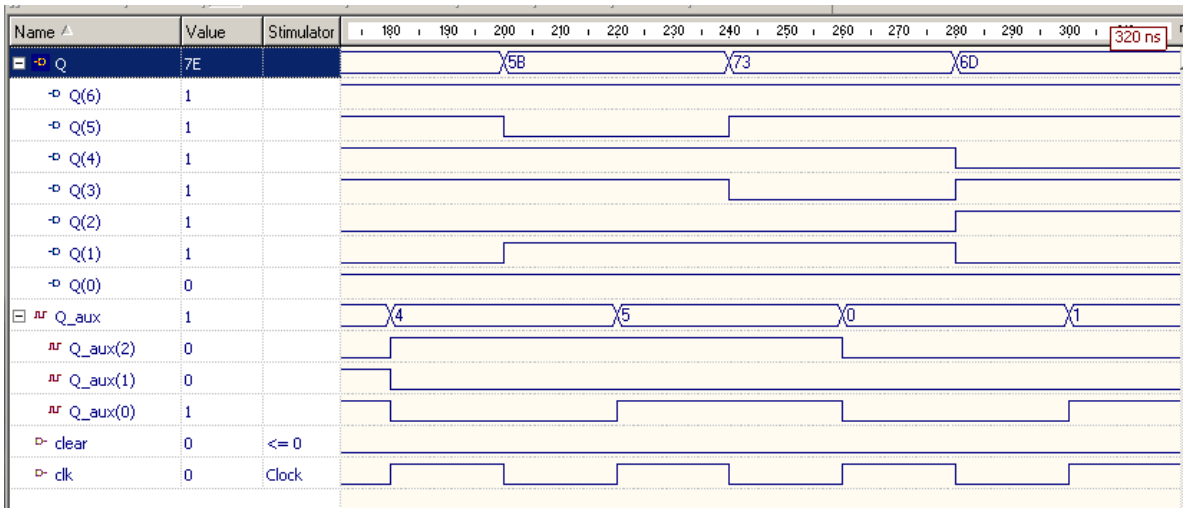
```
            CASE Q_aux IS
                WHEN "000" =>
                    Q <= "1101101";
                WHEN "001" =>
                    Q <= "1111110";
                WHEN "010" =>
                    Q <= "1011111";
                WHEN "011" =>
                    Q <= "1111001";
                WHEN "100" =>
                    Q <= "1011011";
                WHEN "101" =>
                    Q <= "1110011";
                WHEN OTHERS => Q <= "1101101";
            END CASE;
    END PROCESS;

END behavior;
```



```
Compilation successful.
genvhdl -s 1164_VHDL -i "examen2brb.vhd"
Running: batnova -v -f -lstd_logic examen2brb
genvhdl completed
Done.
```


Name
Value
Stimulator
10
20
30
40
50
60
70
80
90
100
110
120
Q
7E
6D
7E
5F
Q(6)
1
Q(5)
1
Q(4)
1
Q(3)
1
Q(2)
1
Q(1)
1
Q(0)
0
Q_aux
1
0
1
2
Q_aux(2)
0
Q_aux(1)
0
Q_aux(0)
1
clear
0
<= 0
clk
0
Clock


Name
Value
Stimulator
140
150
160
170
180
190
200
210
220
230
240
250
260
270
Q
7E
79
5B
73
Q(6)
1
Q(5)
1
Q(4)
1
Q(3)
1
Q(2)
1
Q(1)
1
Q(0)
0
Q_aux
1
3
4
5
0
Q_aux(2)
0
Q_aux(1)
0
Q_aux(0)
1
clear
0
<= 0
clk
0
Clock


Name
Value
Stimulator
180
190
200
210
220
230
240
250
260
270
280
290
300
320 ns
Q
7E
5B
73
6D
Q(6)
1
Q(5)
1
Q(4)
1
Q(3)
1
Q(2)
1
Q(1)
1
Q(0)
0
Q_aux
1
4
5
0
1
Q_aux(2)
0
Q_aux(1)
0
Q_aux(0)
1
clear
0
<= 0
clk
0
Clock