

Examen 1: Brayan Ramirez Benitez

Instrucciones. Una vez terminado el Examen adjuntar en un PDF sus respuestas (imágenes, links de simulaciones, capturas de pantalla, codigovhd,etc.).

Con base en el siguiente circuito, resuelva lo que se pide.

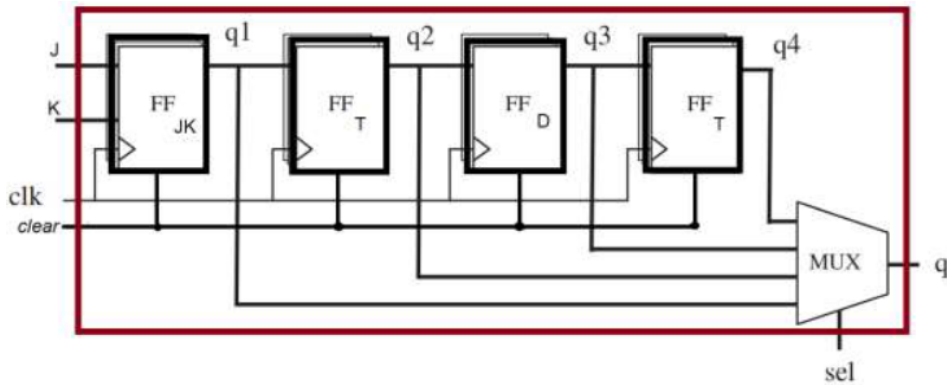
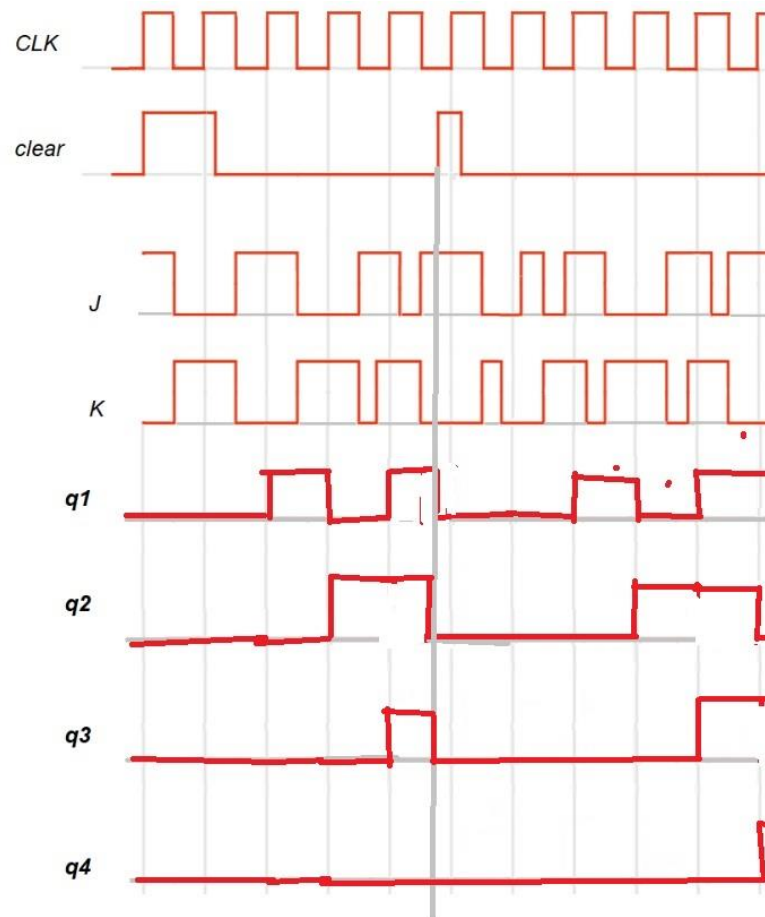


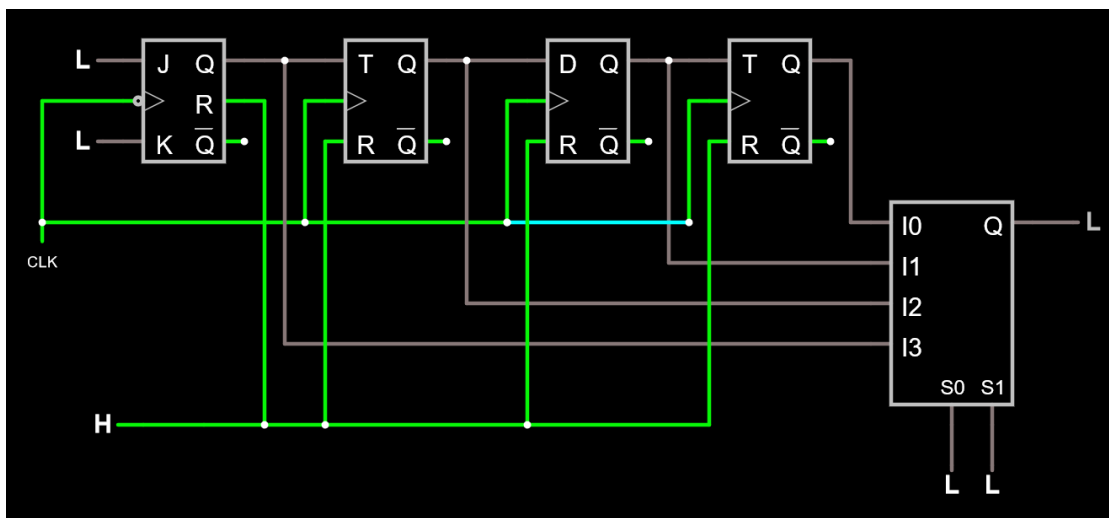
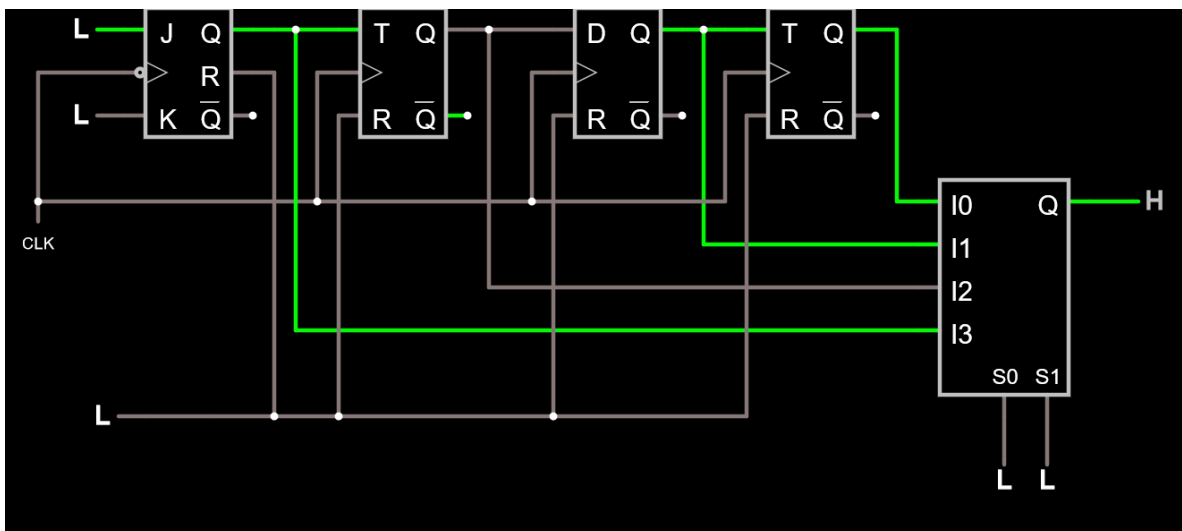
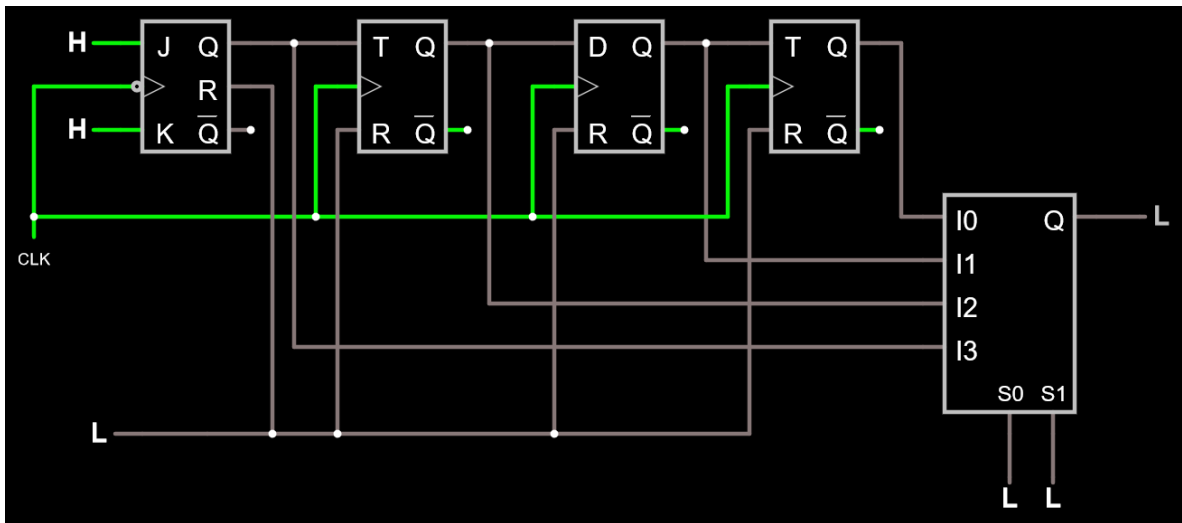
Fig.1

1.-Realice el cronograma de tiempos correspondiente al diagrama lógico de la Fig.1



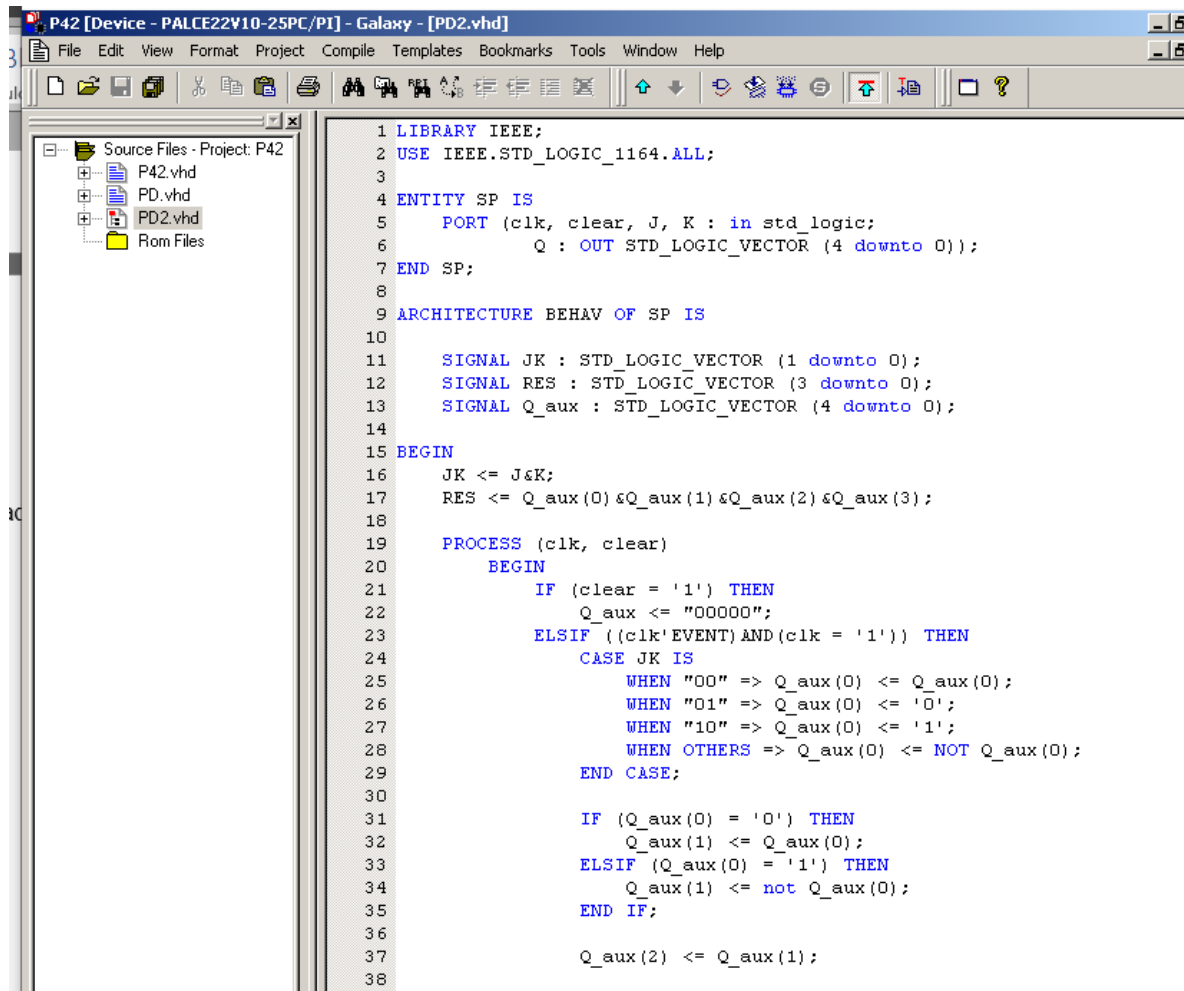
Cronograma de tiempo de la Fig.1

2.-Realice el circuito en Falstad y simule el correcto funcionamiento. (adjuntar el link y capturas de pantalla del circuito realizado, individual).



Link: <https://tinyurl.com/ygox3gpo>

3.-Diseñar el circuito en HDL funcional (adjuntar código VHD en txt. Capturas del código, compilación y simulaciones)



The screenshot shows the GALAXY IDE interface for a project named 'P42'. The left pane displays the 'Source Files - Project: P42' tree with files 'P42.vhd', 'PD.vhd', and 'PD2.vhd'. The main editor window shows the VHD code for 'PD2.vhd'. The code defines an entity 'SP' with inputs 'clk', 'clear', 'J', and 'K', and a 4-bit output 'Q'. The architecture 'BEHAV OF SP' implements a sequential circuit using a process with a clock and clear signal. It uses a 4-bit auxiliary register 'Q_aux' to store the current state and a 3-bit register 'RES' to store the output. The logic for the next state of 'Q_aux' is determined by the inputs 'J' and 'K' and the current state of 'Q_aux'.

```
1 LIBRARY IEEE;
2 USE IEEE.STD_LOGIC_1164.ALL;
3
4 ENTITY SP IS
5     PORT (clk, clear, J, K : in std_logic;
6           Q : OUT STD_LOGIC_VECTOR (4 downto 0));
7 END SP;
8
9 ARCHITECTURE BEHAV OF SP IS
10
11     SIGNAL JK : STD_LOGIC_VECTOR (1 downto 0);
12     SIGNAL RES : STD_LOGIC_VECTOR (3 downto 0);
13     SIGNAL Q_aux : STD_LOGIC_VECTOR (4 downto 0);
14
15 BEGIN
16     JK <= J&K;
17     RES <= Q_aux(0) & Q_aux(1) & Q_aux(2) & Q_aux(3);
18
19     PROCESS (clk, clear)
20     BEGIN
21         IF (clear = '1') THEN
22             Q_aux <= "00000";
23         ELSIF ((clk'EVENT) AND (clk = '1')) THEN
24             CASE JK IS
25                 WHEN "00" => Q_aux(0) <= Q_aux(0);
26                 WHEN "01" => Q_aux(0) <= '0';
27                 WHEN "10" => Q_aux(0) <= '1';
28                 WHEN OTHERS => Q_aux(0) <= NOT Q_aux(0);
29             END CASE;
30
31             IF (Q_aux(0) = '0') THEN
32                 Q_aux(1) <= Q_aux(0);
33             ELSIF (Q_aux(0) = '1') THEN
34                 Q_aux(1) <= not Q_aux(0);
35             END IF;
36
37             Q_aux(2) <= Q_aux(1);
38
```

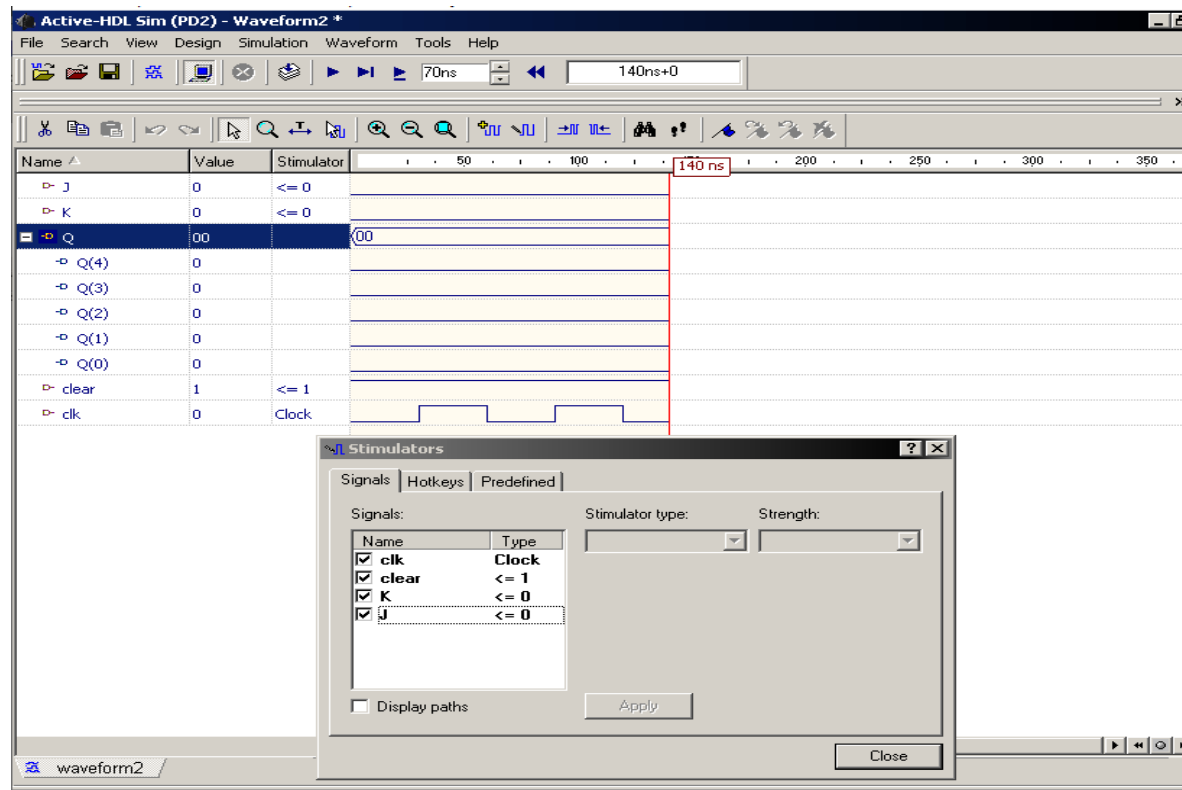
```

38
39         IF (Q_aux(2) = '0') THEN
40             Q_aux(3) <= Q_aux(2);
41         ELSIF (Q_aux(2) = '1') THEN
42             Q_aux(3) <= not Q_aux(2);
43         END IF;
44
45         CASE RES IS
46             WHEN "1011" => Q_aux(4) <= '1';
47             WHEN "1101" => Q_aux(4) <= '1';
48             WHEN OTHERS => Q_aux(4) <= '0';
49         END CASE;
50
51     END IF;
52 END PROCESS;
53 Q <= Q_aux;
54 END BEHAV;

```

PD2.vhd

WARP done.
 Compilation successful.
 genvhdl -s 1164_VHDL -i "PD2.vhd"
 Running: batnova -v -f -lstd_logic PD2
 genvhdl completed
 Done.



Console

• KERNEL: Kernel process initialization phase.
 • ELAB2: Elaboration final pass...
 • ELAB2: Elaboration final pass complete - time: 0.0 [s].
 • KERNEL: Kernel process initialization done.
 • 22:06, lunes, 12 de abril de 2021
 • Simulation has been initialized
 • Selected Top-Level: SP (BEHAV)
 • KERNEL: stopped at time: 70 ns
 • KERNEL: stopped at time: 140 ns