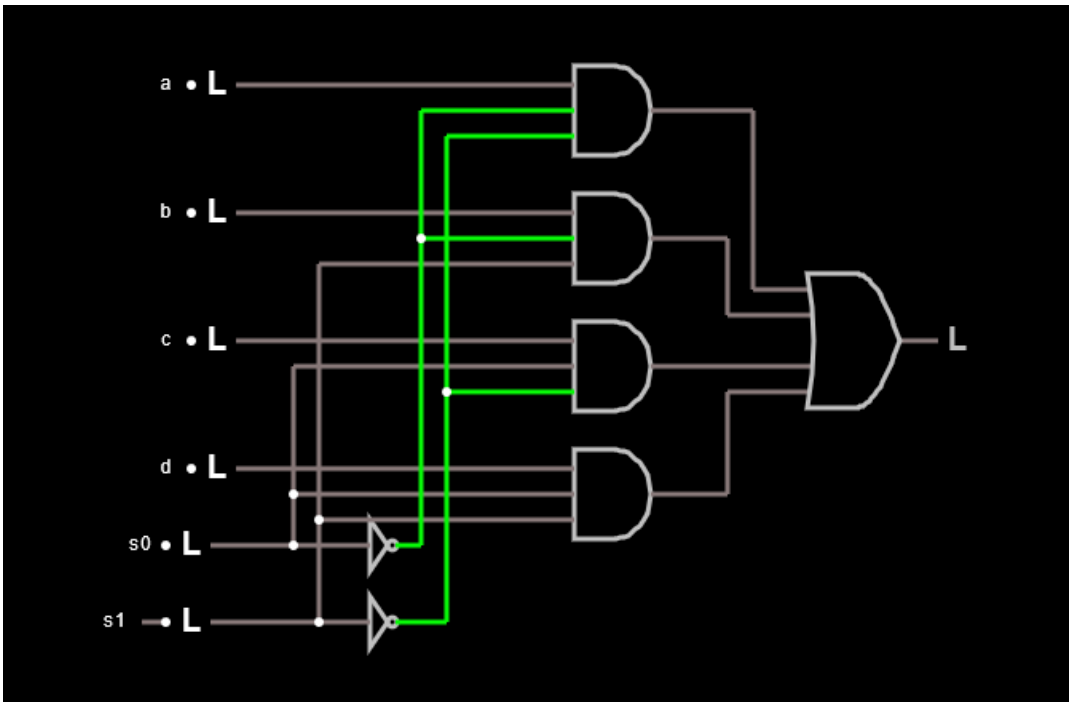
Nombre: Brayan Ramirez Benítez

Compuertas lógicas



Código VHDL

```
 1 library IEEE;
 2 use IEEE.STD_LOGIC_1164.all;
 3 entity mux4to1 is
 4     port (a, b, c,d : in STD_LOGIC_VECTOR(1 downto 0);
 5     s : in STD_LOGIC_VECTOR(1 downto 0);
 6     y : out STD_LOGIC_VECTOR (1 downto 0));
 7 end mux4to1;
 8
 9 architecture mux of mux4to1 is
10 begin
11     y(1) <= (a(1)and not s(1)and not s(0)) or
12             (b(1) and not s(1) and s(0)) or
13             (c(1)and s(1)and not s(0)) or
14             (d(1)and s(1)and s(0));
15     y(0) <= (a(0)and not s(1)and not s(0)) or
16             (b(0) and not s(1) and s(0)) or
17             (c(0)and s(1)and not s(0)) or
18             (d(0)and s(1)and s(0));
19 end mux;
20
```

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Simulaciones