Examen 1: Brayan Ramirez Benitez

Instrucciones. Una vez terminado el Examen adjuntar en un PDF sus respuestas (imágenes, links de simulaciones, capturas de pantalla, codigovhd,etc.).

Con base en el siguiente circuito, resuelva lo que se pide.

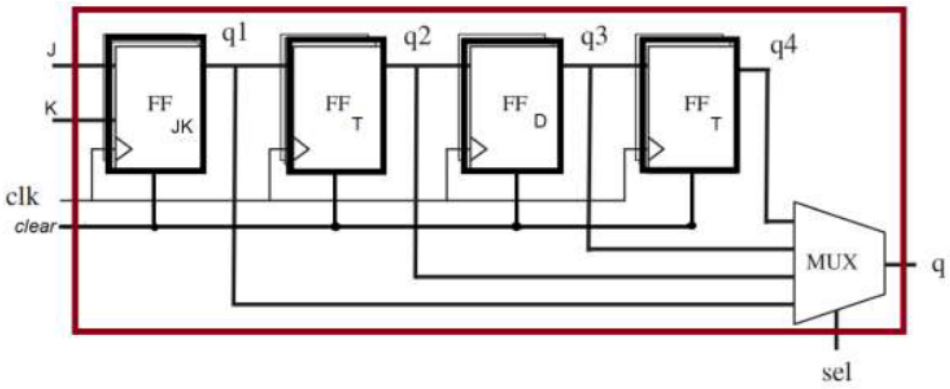
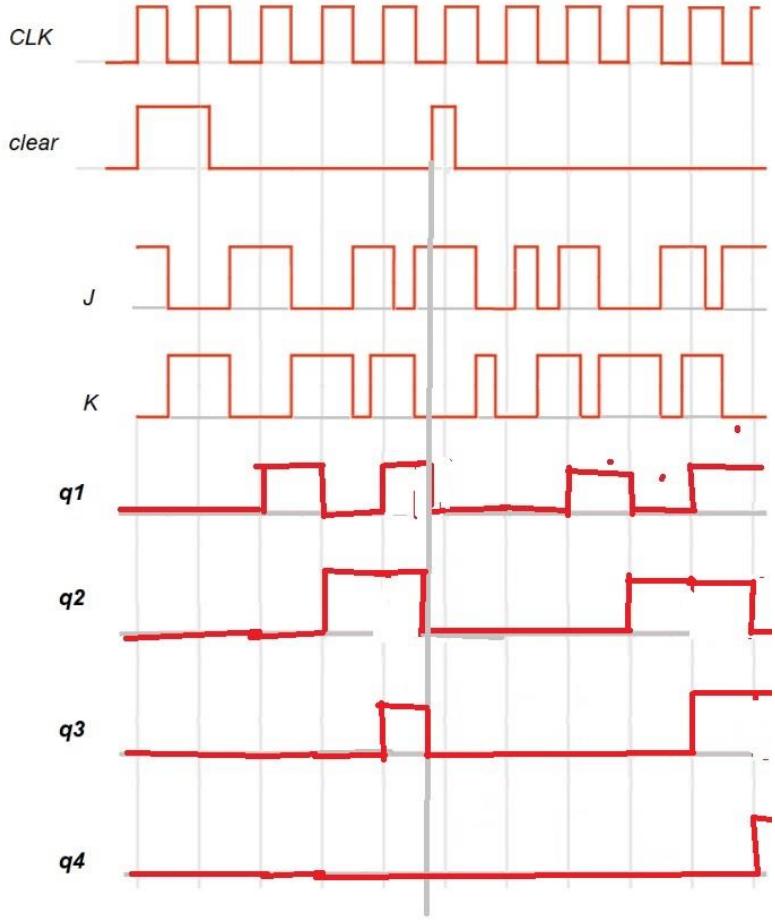


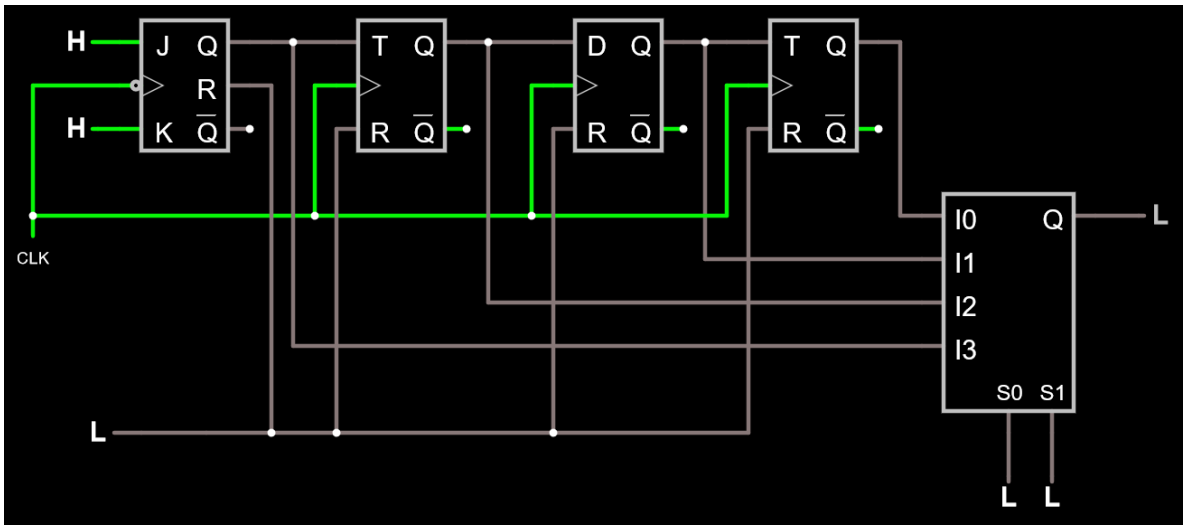
Fig.1

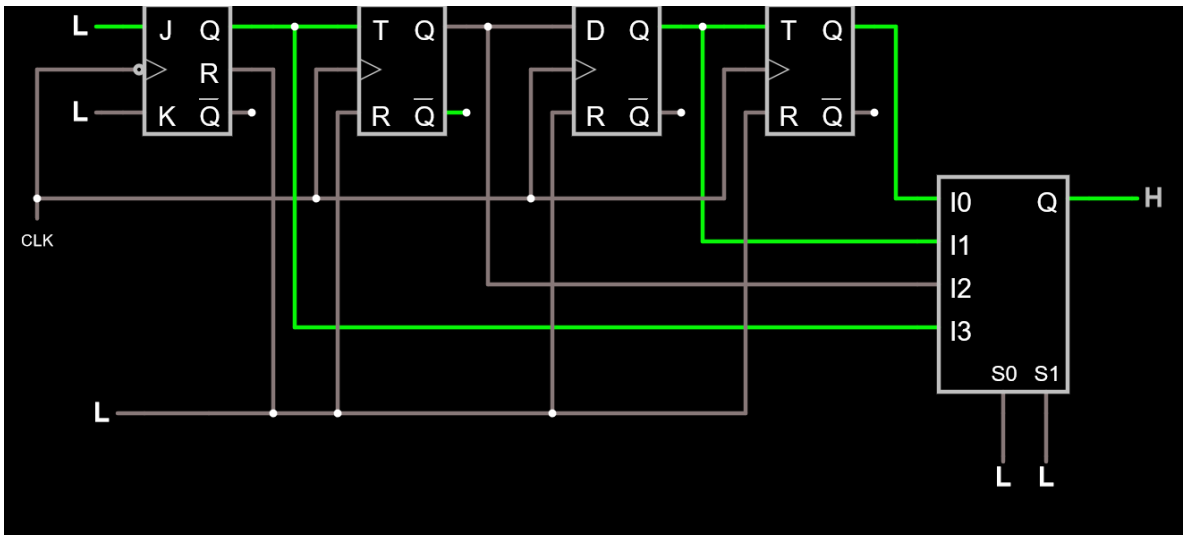
1.-Realice el cronograma de tiempos correspondiente al diagrama lógico de la Fig.1

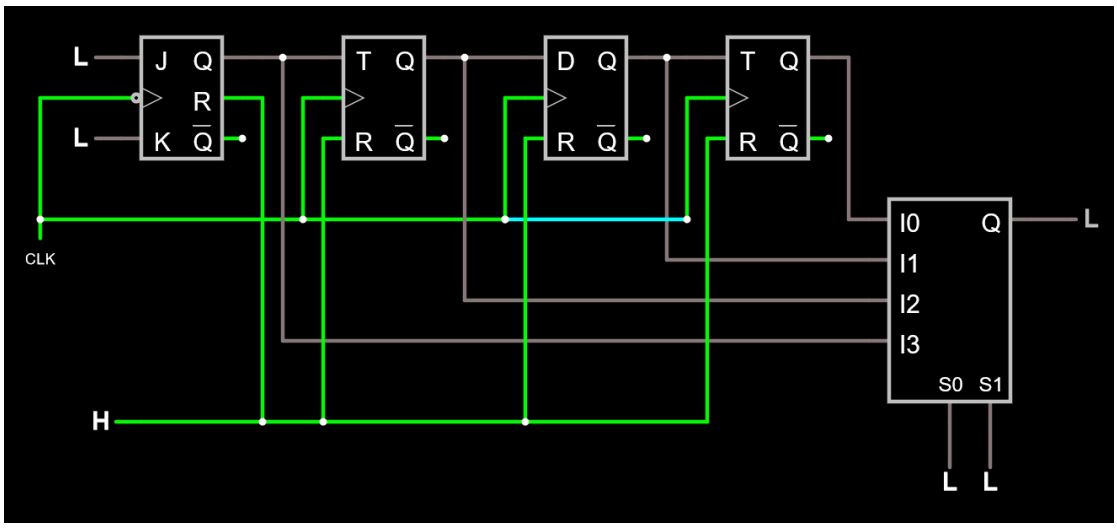


Cronograma de tiempo de la Fig.1

2.-Realice el circuito en Falstad y simule el correcto funcionamiento. (adjuntar el link y capturas de pantalla del circuito realizado, individual).

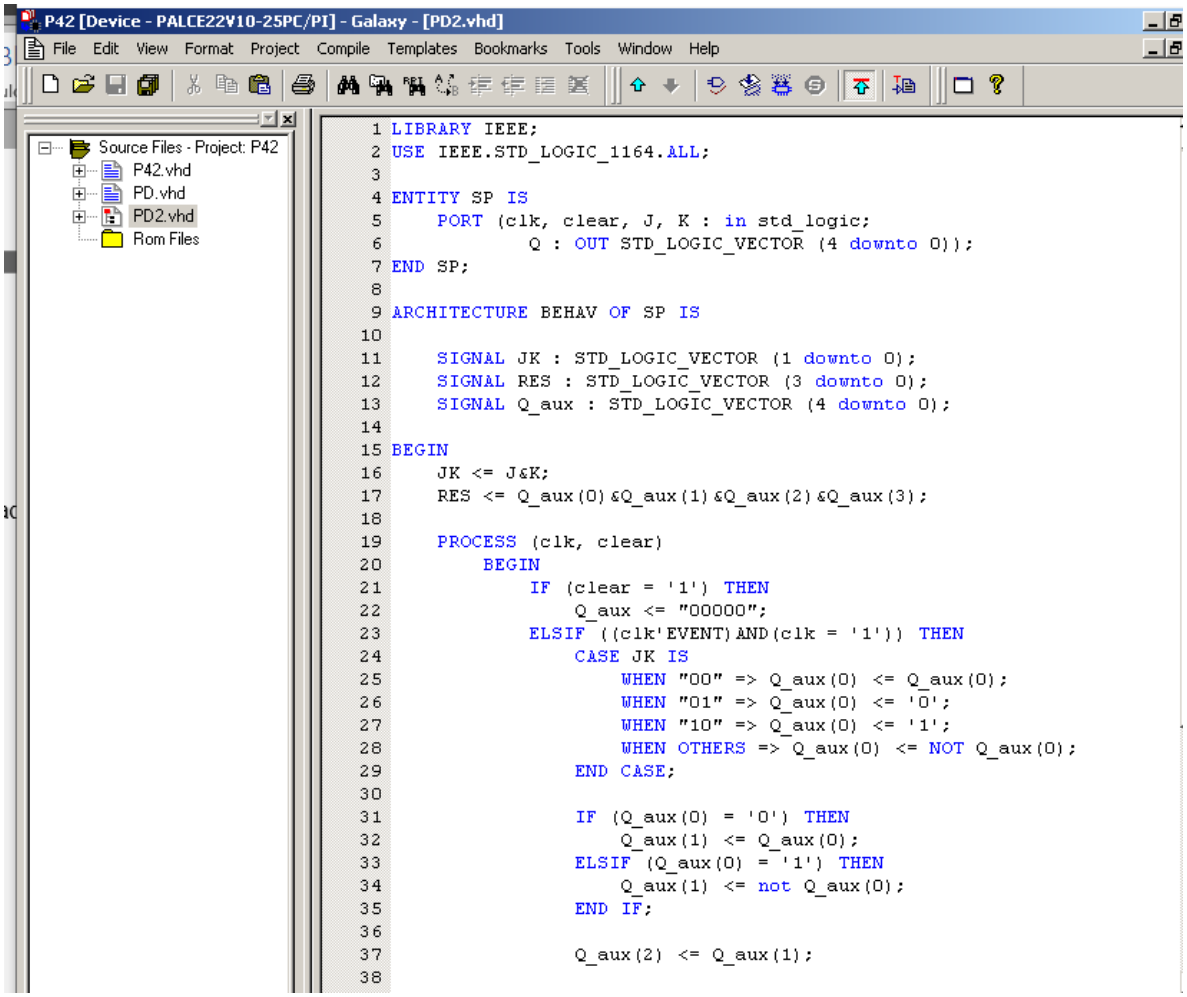






Link: https://tinyurl.com/ygox3gpo

3.-Diseñar el circuito en HDL funcional (adjuntar código VHD en txt. Capturas del código, compilación y simulaciones)



```
38
39                  IF (Q_aux(2) = '0') THEN
40                      Q_aux(3) <= Q_aux(2);
41                  ELSIF (Q_aux(2) = '1') THEN
42                      Q_aux(3) <= not Q_aux(2);
43                  END IF;
44
45                  CASE RES IS
46                      WHEN "1011" => Q_aux(4) <= '1';
47                      WHEN "1101" => Q_aux(4) <= '1';
48                      WHEN OTHERS => Q_aux(4) <= '0';
49                  END CASE;
50
51              END IF;
52      END PROCESS;
53      Q <= Q_aux;
54  END BEHAV;
```

S... Hi... O... PD2.vhd

```
WARP done.
Compilation successful.
genvhdl -s 1164_VHDL -i "PD2.vhd"
Running: batnova -v -f -lstd_logic PD2
genvhdl completed
Done.
```