INSTITUTO POLITÉCNICO NACIONAL

ESCUELA SUPERIOR DE CÓMPUTO

INGENIERIA EN SISTEMAS COMPUTACIONALES

MATERIA: DISEÑO DE SISTEMAS DIGITALES

PROFESOR: TESTA NAVA ALEXIS

PRESENTA:

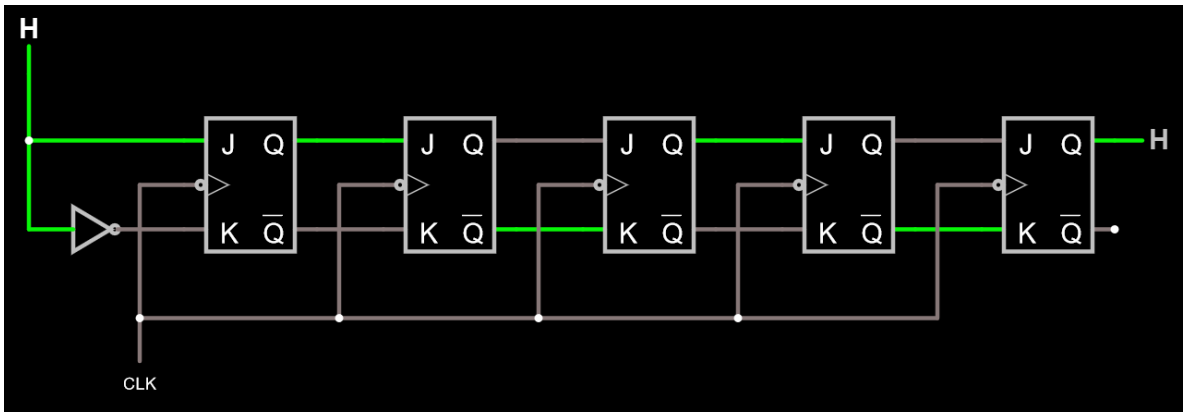
RAMIREZ BENITEZ BRAYAN

GRUPO: 2CV18

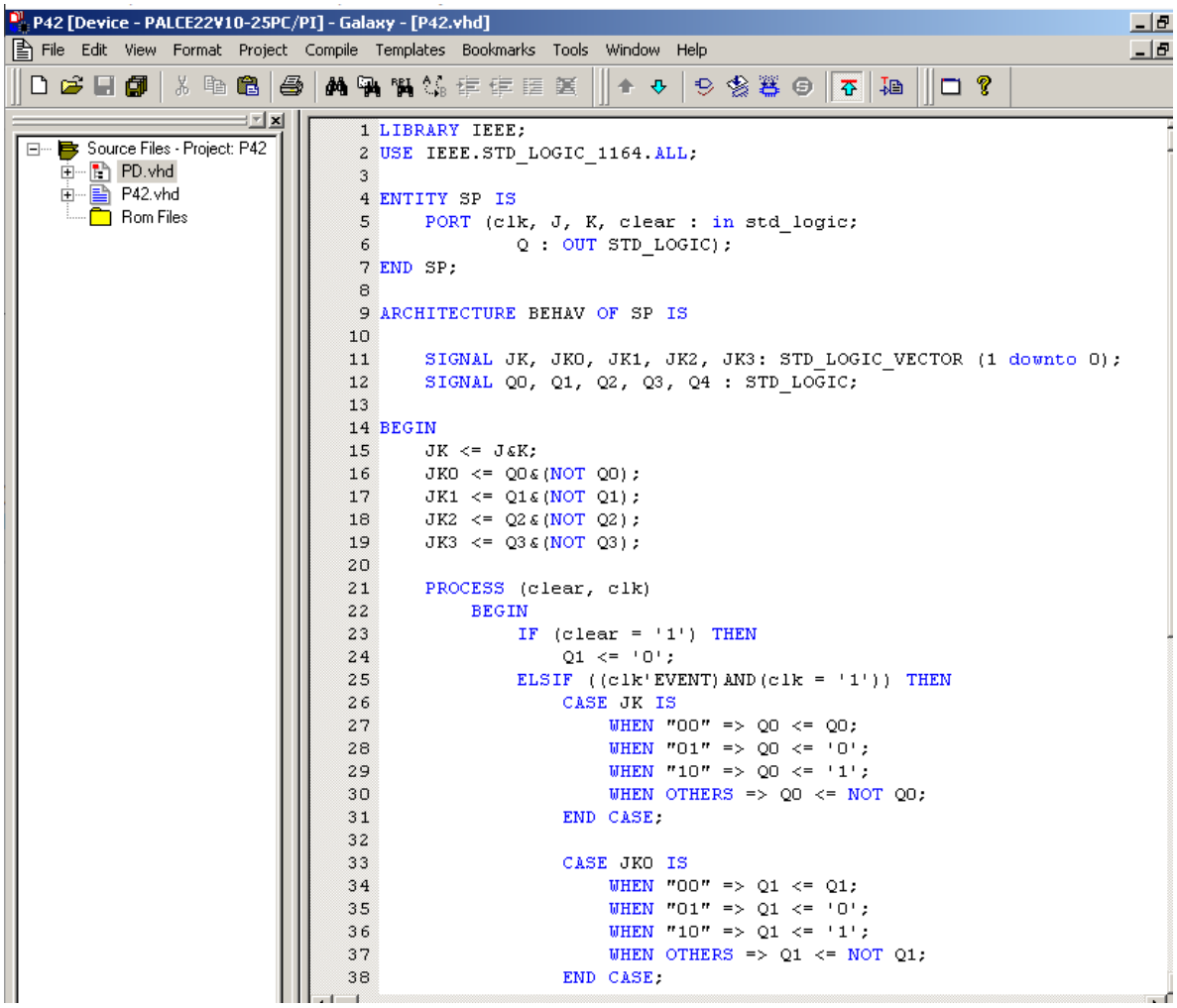
ACTIVIDAD 4

CIUDAD DE MEXICO MARZO DE 2021

Realizar en Falstad y HDL el diseño de los registros:
Entrada Serie - salida Serie (Con JK)



Enlace: https://tinyurl.com/yhrdpeyj



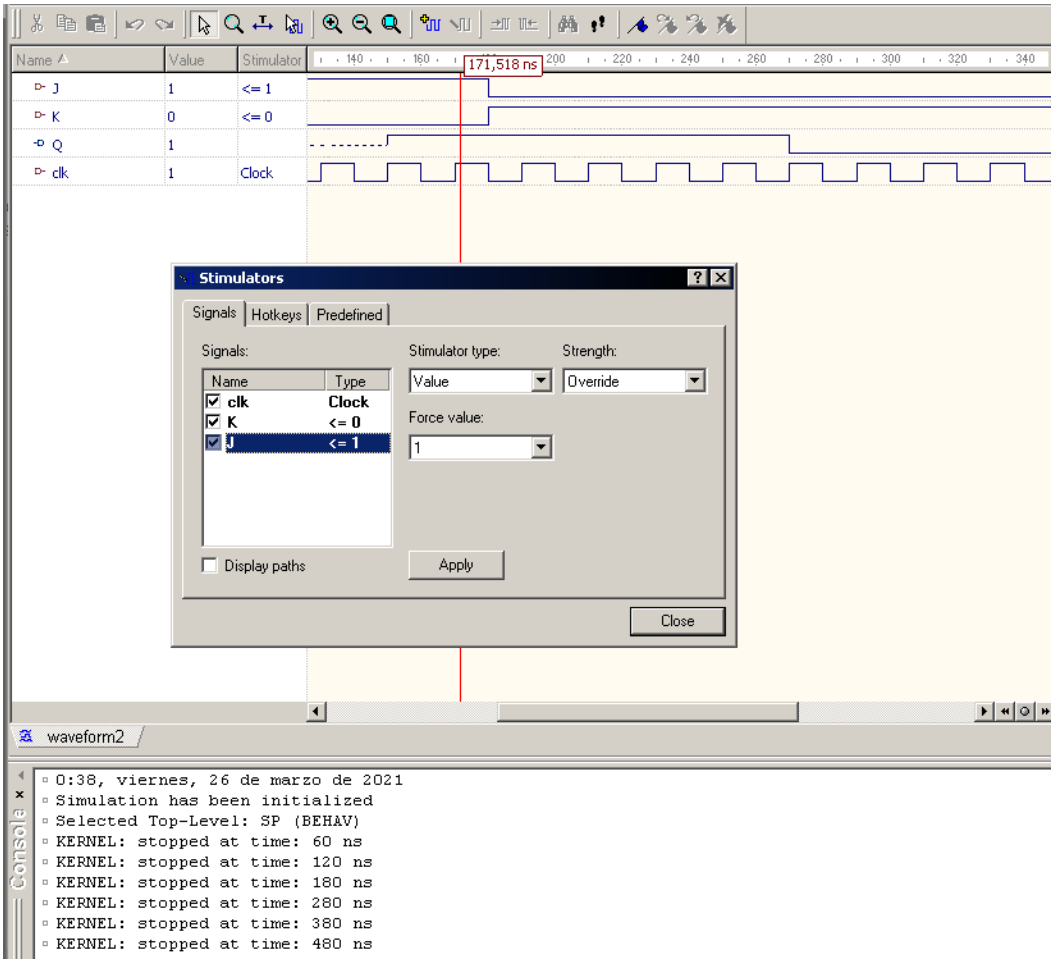

```
1  LIBRARY IEEE;
2  USE IEEE.STD_LOGIC_1164.ALL;
3
4  ENTITY SP IS
5      PORT (clk, J, K, clear : in std_logic;
6            Q : OUT STD_LOGIC);
7  END SP;
8
9  ARCHITECTURE BEHAV OF SP IS
10
11     SIGNAL JK, JK0, JK1, JK2, JK3: STD_LOGIC_VECTOR (1 downto 0);
12     SIGNAL Q0, Q1, Q2, Q3, Q4 : STD_LOGIC;
13
14 BEGIN
15     JK <= J&K;
16     JK0 <= Q0&(NOT Q0);
17     JK1 <= Q1&(NOT Q1);
18     JK2 <= Q2&(NOT Q2);
19     JK3 <= Q3&(NOT Q3);
20
21     PROCESS (clear, clk)
22         BEGIN
23             IF (clear = '1') THEN
24                 Q1 <= '0';
25             ELSIF ((clk'EVENT)AND(clk = '1')) THEN
26                 CASE JK IS
27                     WHEN "00" => Q0 <= Q0;
28                     WHEN "01" => Q0 <= '0';
29                     WHEN "10" => Q0 <= '1';
30                     WHEN OTHERS => Q0 <= NOT Q0;
31                 END CASE;
32
33                 CASE JK0 IS
34                     WHEN "00" => Q1 <= Q1;
35                     WHEN "01" => Q1 <= '0';
36                     WHEN "10" => Q1 <= '1';
37                     WHEN OTHERS => Q1 <= NOT Q1;
38                 END CASE;
```

```
                CASE JK1 IS
                    WHEN "00" => Q2 <= Q2;
                    WHEN "01" => Q2 <= '0';
                    WHEN "10" => Q2 <= '1';
                    WHEN OTHERS => Q2 <= NOT Q2;
                END CASE;

                CASE JK2 IS
                    WHEN "00" => Q3 <= Q3;
                    WHEN "01" => Q3 <= '0';
                    WHEN "10" => Q3 <= '1';
                    WHEN OTHERS => Q3 <= NOT Q3;
                END CASE;

                CASE JK3 IS
                    WHEN "00" => Q4 <= Q4;
                    WHEN "01" => Q4 <= '0';
                    WHEN "10" => Q4 <= '1';
                    WHEN OTHERS => Q4 <= NOT Q4;
                END CASE;

            END IF;
    END PROCESS;
    Q <= Q4;
END BEHAV;
```

S... Hi... O...

P42.vhd | P4.vhd | PD.vhd

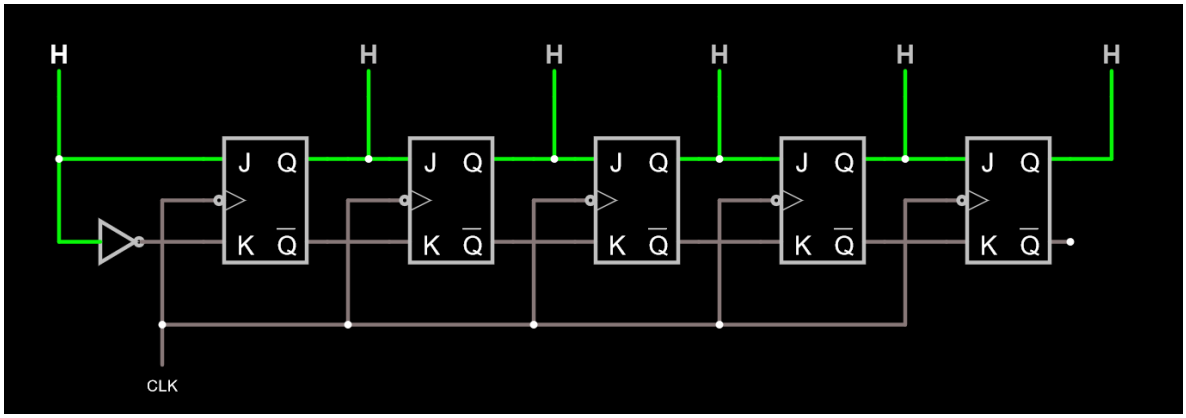
```
WARP done.
Compilation successful.
genvhdl -s 1164_VHDL -i "PD.vhd"
Running: batnova -v -f -lstd_logic PD
genvhdl completed
Done.
```



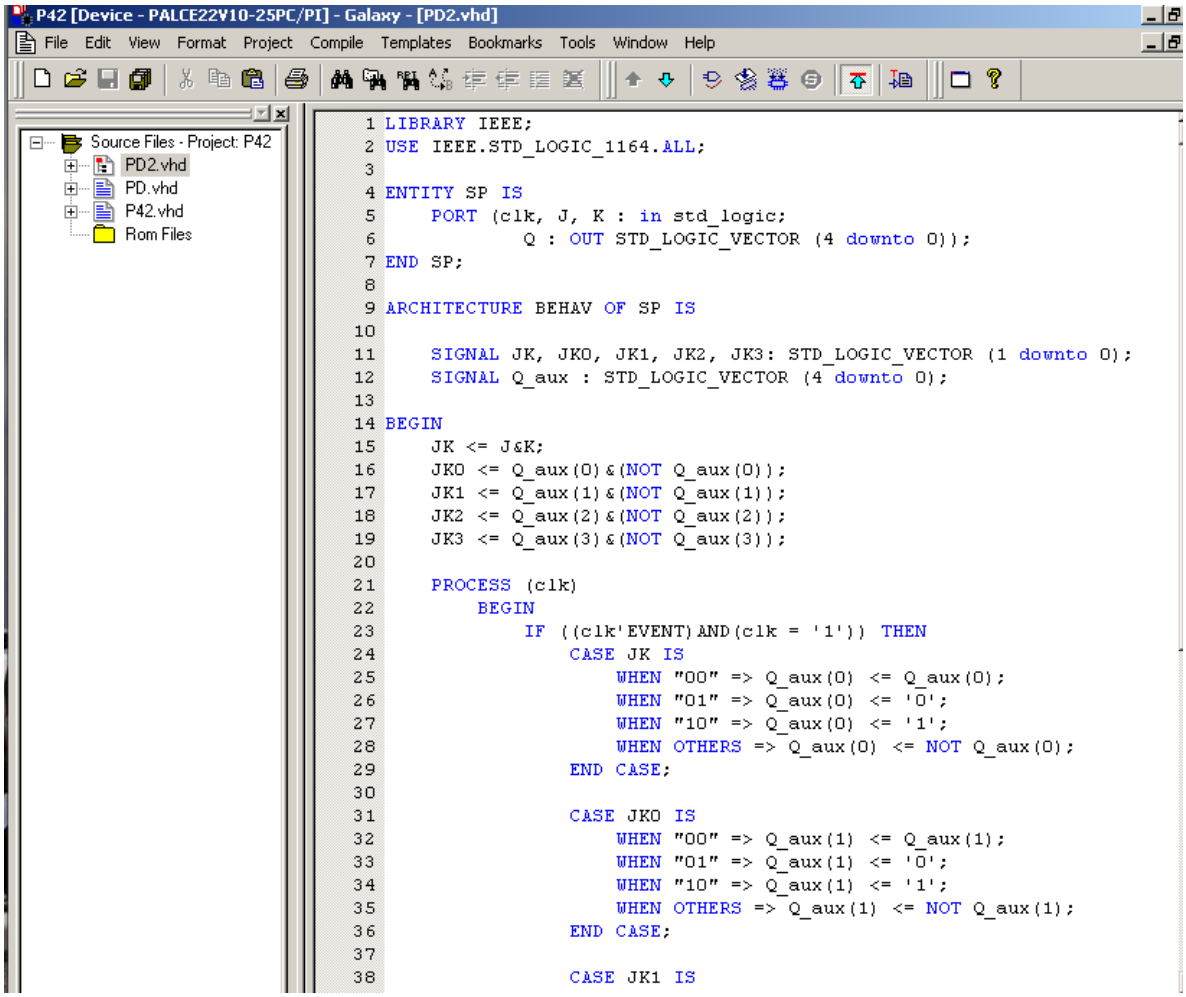

```
0:38, viernes, 26 de marzo de 2021
Simulation has been initialized
Selected Top-Level: SP (BEHAV)
KERNEL: stopped at time: 60 ns
KERNEL: stopped at time: 120 ns
KERNEL: stopped at time: 180 ns
KERNEL: stopped at time: 280 ns
KERNEL: stopped at time: 380 ns
KERNEL: stopped at time: 480 ns
```

Consola

Entrada Serie - salida Paralelo (Con JK)
de 5 bits.



Enlace: https://tinyurl.com/yzh73dag

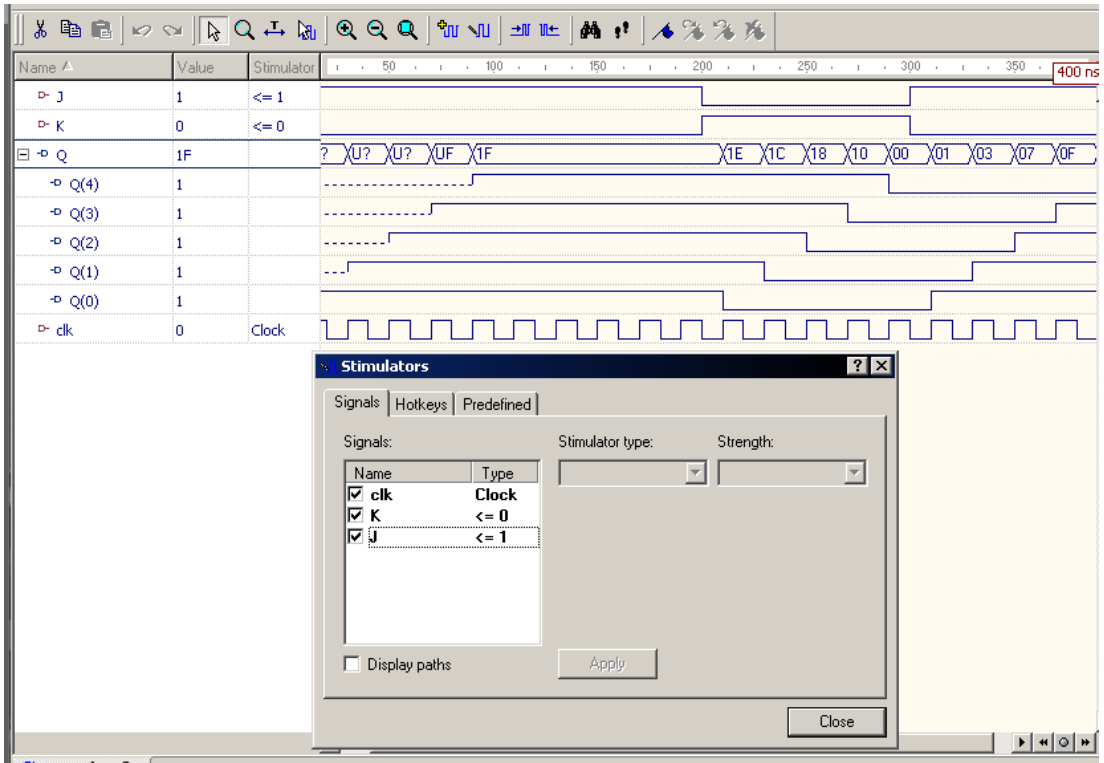



```
1  LIBRARY IEEE;
2  USE IEEE.STD_LOGIC_1164.ALL;
3
4  ENTITY SP IS
5      PORT (clk, J, K : in std_logic;
6            Q : OUT STD_LOGIC_VECTOR (4 downto 0));
7  END SP;
8
9  ARCHITECTURE BEHAV OF SP IS
10
11     SIGNAL JK, JK0, JK1, JK2, JK3: STD_LOGIC_VECTOR (1 downto 0);
12     SIGNAL Q_aux : STD_LOGIC_VECTOR (4 downto 0);
13
14 BEGIN
15     JK <= J&K;
16     JK0 <= Q_aux(0)&(NOT Q_aux(0));
17     JK1 <= Q_aux(1)&(NOT Q_aux(1));
18     JK2 <= Q_aux(2)&(NOT Q_aux(2));
19     JK3 <= Q_aux(3)&(NOT Q_aux(3));
20
21     PROCESS (clk)
22         BEGIN
23             IF ((clk'EVENT)AND(clk = '1')) THEN
24                 CASE JK IS
25                     WHEN "00" => Q_aux(0) <= Q_aux(0);
26                     WHEN "01" => Q_aux(0) <= '0';
27                     WHEN "10" => Q_aux(0) <= '1';
28                     WHEN OTHERS => Q_aux(0) <= NOT Q_aux(0);
29                 END CASE;
30
31                 CASE JK0 IS
32                     WHEN "00" => Q_aux(1) <= Q_aux(1);
33                     WHEN "01" => Q_aux(1) <= '0';
34                     WHEN "10" => Q_aux(1) <= '1';
35                     WHEN OTHERS => Q_aux(1) <= NOT Q_aux(1);
36                 END CASE;
37
38                 CASE JK1 IS
```

```
39                      WHEN "00" => Q_aux(2) <= Q_aux(2);
40                      WHEN "01" => Q_aux(2) <= '0';
41                      WHEN "10" => Q_aux(2) <= '1';
42                      WHEN OTHERS => Q_aux(2) <= NOT Q_aux(2);
43                  END CASE;
44
45                  CASE JK2 IS
46                      WHEN "00" => Q_aux(3) <= Q_aux(3);
47                      WHEN "01" => Q_aux(3) <= '0';
48                      WHEN "10" => Q_aux(3) <= '1';
49                      WHEN OTHERS => Q_aux(3) <= NOT Q_aux(3);
50                  END CASE;
51
52                  CASE JK3 IS
53                      WHEN "00" => Q_aux(4) <= Q_aux(4);
54                      WHEN "01" => Q_aux(4) <= '0';
55                      WHEN "10" => Q_aux(4) <= '1';
56                      WHEN OTHERS => Q_aux(4) <= NOT Q_aux(4);
57                  END CASE;
58
59              END IF;
60      END PROCESS;
61      Q <= Q_aux;
62  END BEHAV;
```

S... Hi... O... PD2.vhd

```
WARP done.
Compilation successful.
genvhdl -s 1164_VHDL -i "PD2.vhd"
Running: batnova -v -f -lstd_logic PD2
genvhdl completed
Done.
```




```
ELAB2: Elaboration final pass complete - time: 0.0 [s].
KERNEL: Kernel process initialization done.
2:10, viernes, 26 de marzo de 2021
Simulation has been initialized
Selected Top-Level: SP (BEHAV)
KERNEL: stopped at time: 100 ns
KERNEL: stopped at time: 200 ns
KERNEL: stopped at time: 300 ns
KERNEL: stopped at time: 400 ns
```