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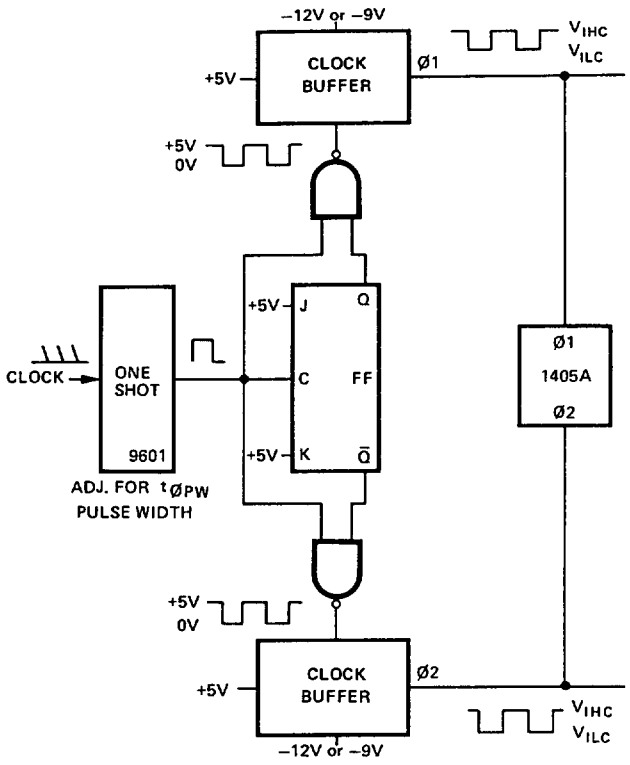
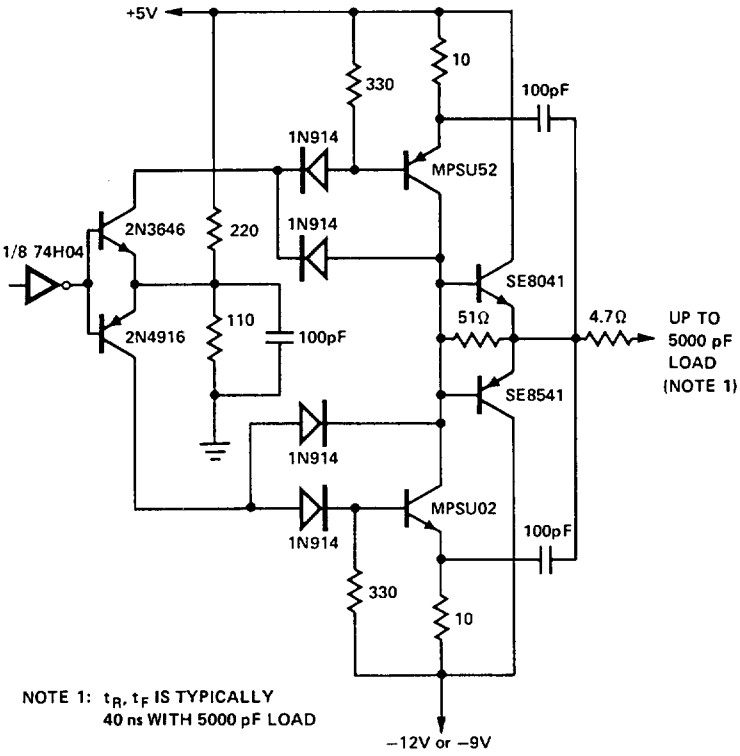
Application Information

Two Phase Clock Generator

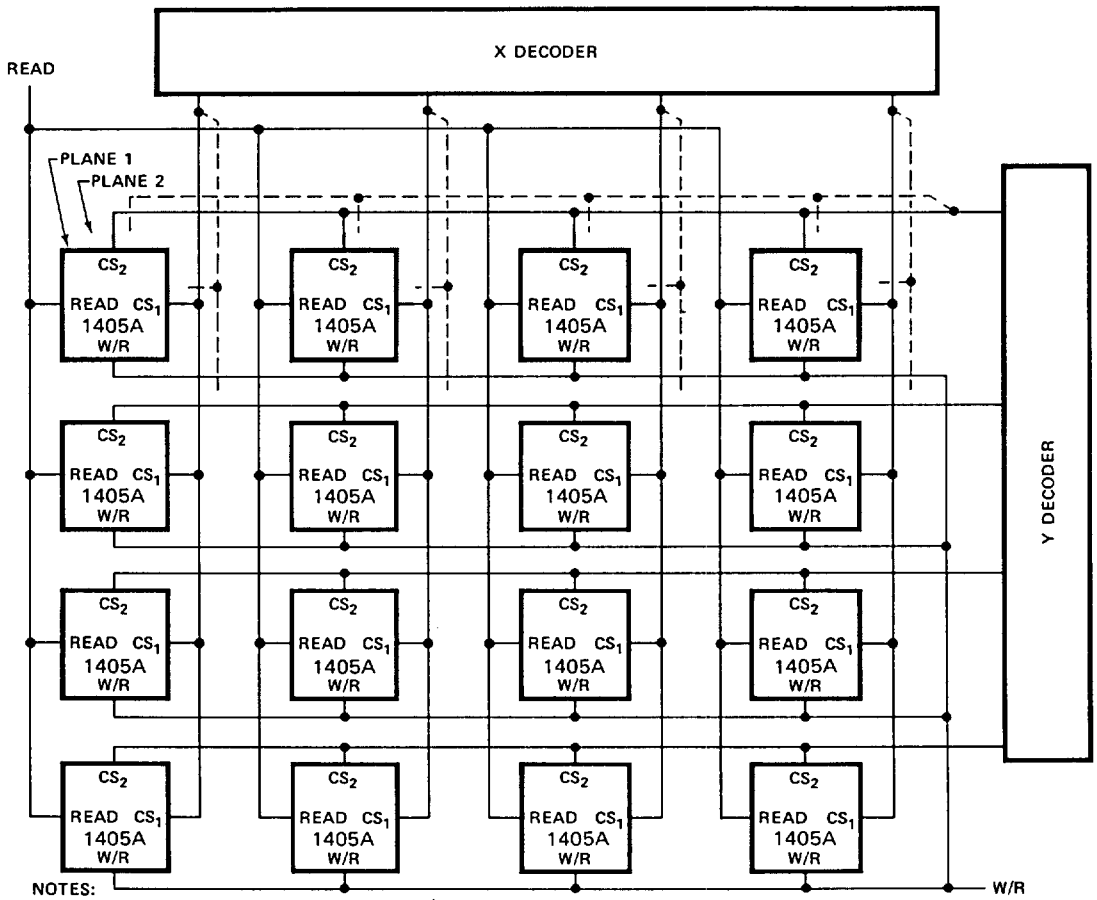


High Speed Clock Buffer



NOTE 1: t_R, t_F IS TYPICALLY 40 ns WITH 5000 pF LOAD

Write/Recirculate Logic



NOTES:
1. Outputs common for each plane
2. All inputs common
3. All ϕ_1's common
4. All ϕ_2's common
5. All V_{CC} common
6. All V_{DD} common

Application Information

4 Bit Recirculating Shift Register

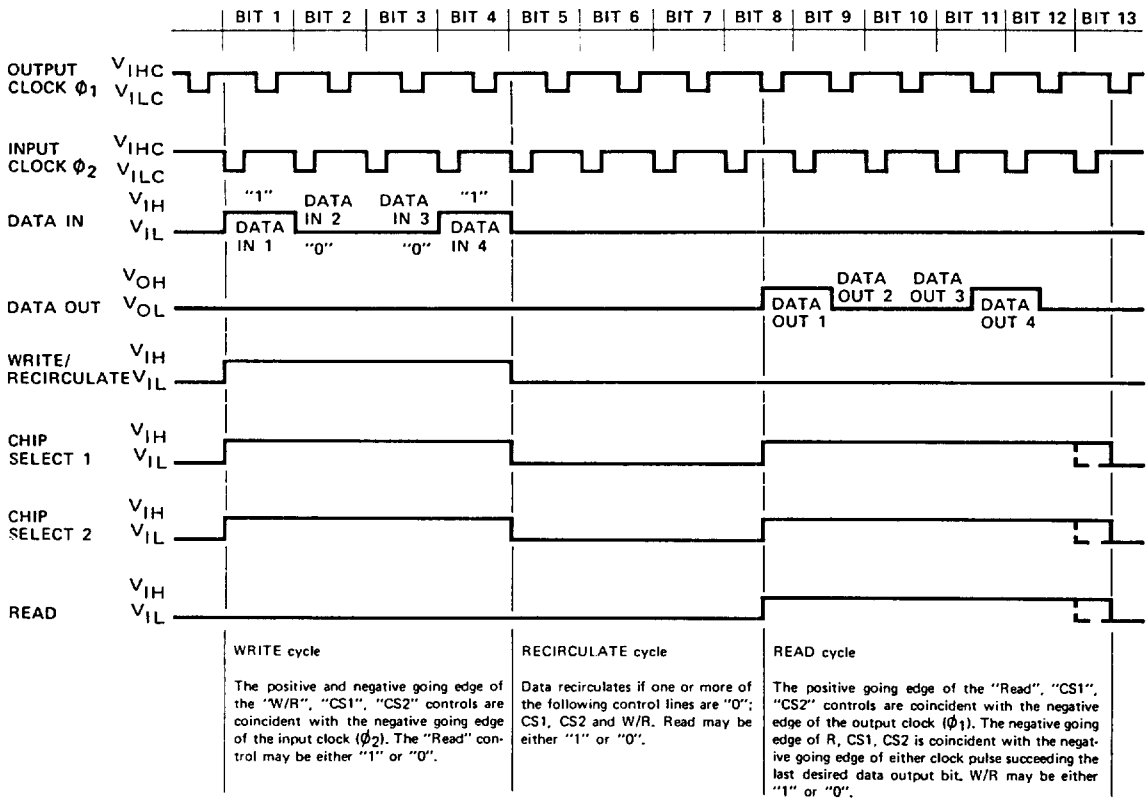
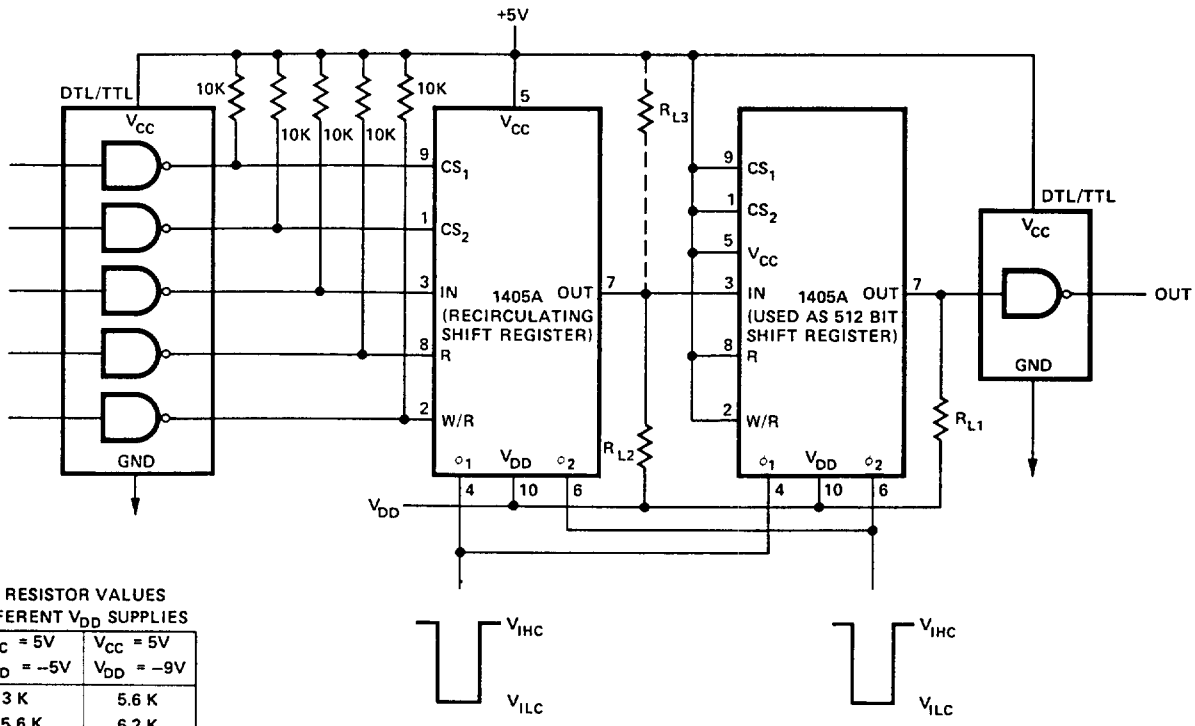


Figure 1

Fig. 1 is a simplified illustration of the timing of a 4 bit recirculating shift register showing the 3 basic modes of operation.

DTL/TTL/MOS Interfaces

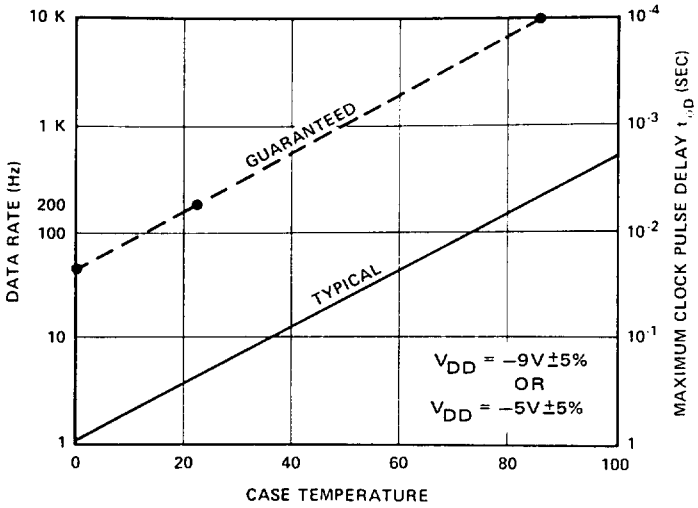


R_L LOAD RESISTOR VALUES FOR DIFFERENT V_{DD} SUPPLIES

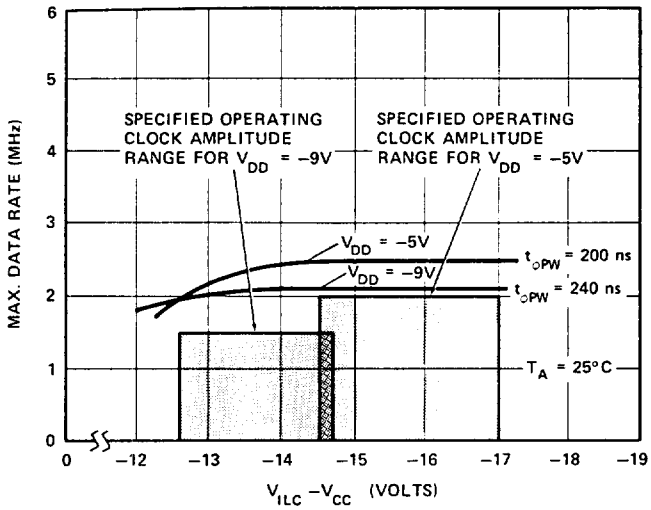
	V_{CC} = 5V, V_{DD} = −5V	V_{CC} = 5V, V_{DD} = −9V
R_{L1}	3 K	5.6 K
R_{L2}	5.6 K	6.2 K
R_{L3}	not required	3.9 K

Typical Characteristics

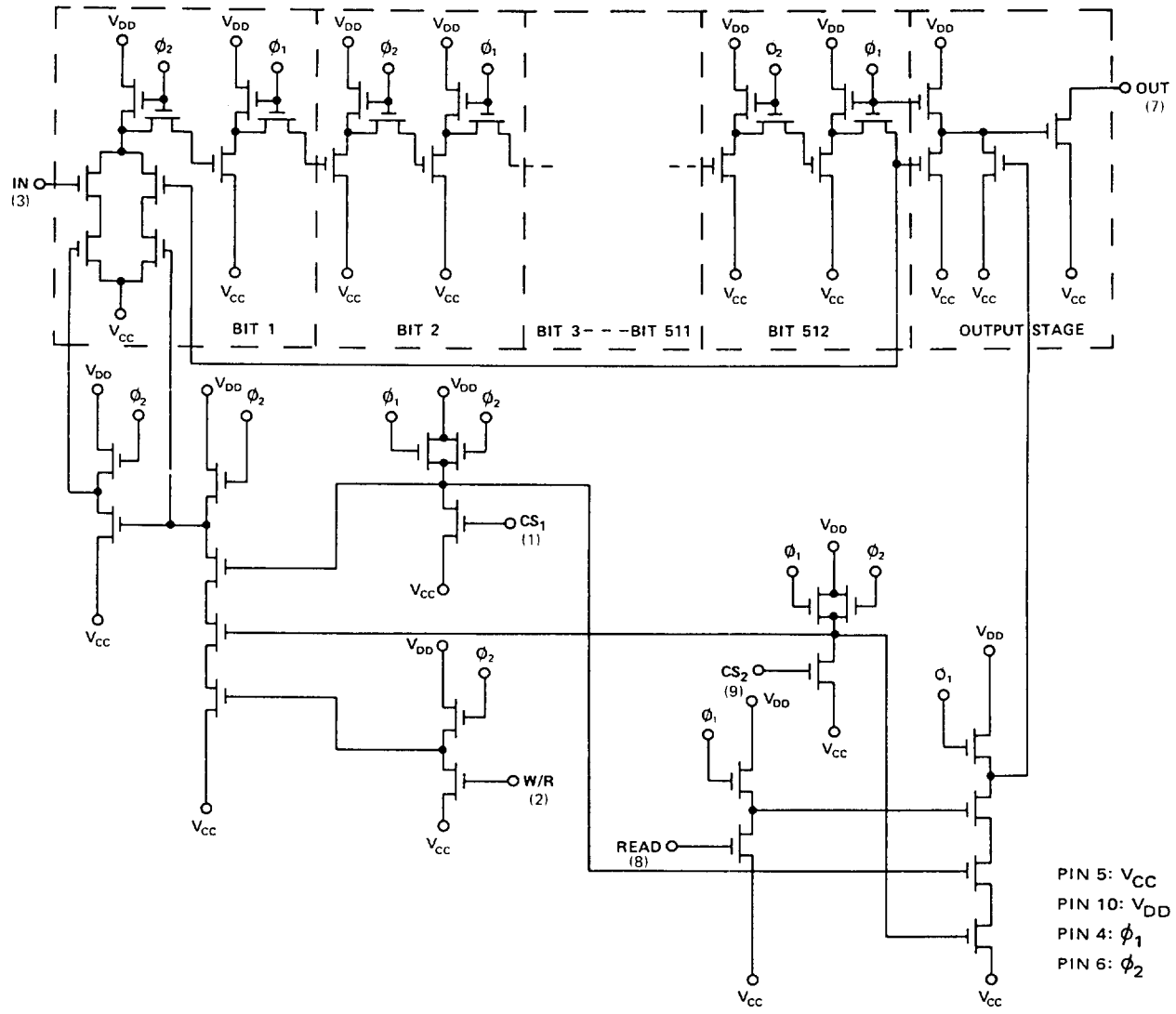
MINIMUM OPERATING DATA RATE
OR MAXIMUM CLOCK PULSE DELAY
VS. TEMPERATURE



MAXIMUM DATA RATE
VS. CLOCK AMPLITUDE



Circuit Schematic



A.C. Characteristics T_{CASE} = 0°C to +85° C; V_{CC} = +5 ± 5%; C_L = 20 pF; 1 TTL Load

SYMBOL	TEST	V_{DD} = −5V ± 5% V_{ILC}=V_{CC}−14.5 to V_{CC}−17 R_L = 3 K		V_{DD} = −9V ± 5% V_{ILC}=V_{CC}−12.6 to V_{CC}−14.7 R_L = 5.6 K		UNIT
		MIN.	MAX.	MIN.	MAX.	
Frequency	CLOCK DATA REP RATE	200 Hz @ 25°C(1)	2	200Hz @ 25°C(1)	1.5	MHz
$t_{\phi PW}$	CLOCK PULSE WIDTH	0.200	10	.240	10	μsec
$t_{\phi D}$	CLOCK PULSE DELAY	30	Note 1	30	Note 1	nsec
Duty Cycle(2)	CLOCK DUTY CYCLE		40		36	%
t_R;t_F	CLOCK PULSE TRANSITION		1		1	μsec
t_{DW}	DATA WRITE (SETUP) TIME	100		100		nsec
t_{DH}	DATA TO CLOCK HOLD TIME	20		20		nsec
t_{A+}; t_{A-}	CLOCK TO DATA OUT DELAY		250		250	nsec
t_{R-}; t_{CS-}; t_{WR-}	CLOCK TO "READ" OR "CHIP SELECT" OR "WRITE/ RECIRCULATE" TIMING	0		0		nsec
t_{R+}; t_{CS+}; t_{WR+}	CLOCK TO "READ" OR "CHIP SELECT" OR "WRITE/ RECIRCULATE" TIMING	0		0		nsec

CAPACITANCE(3) V_{CC} = 5V ± 5%, V_{DD} = −5V ± 5% or −9V ± 5%, T_A = 25°C

SYMBOL	TEST	TYP.	MAX.	CONDITIONS	
C_{IN}	INPUT CAPACITANCE	3	5 pF	V_{IN} = V_{CC}	f = 1 MHz
C_{OUT}	OUTPUT CAPACITANCE	2	5 pF	V_{OUT} = V_{CC}	
C_ϕ	CLOCK CAPACITANCE	75	85 pF	V_ϕ = V_{CC}	
$C_{\phi_1\text{-}\phi_2}$	CLOCK TO CLOCK CAPACITANCE	6	10 pF	V_ϕ = V_{CC}	

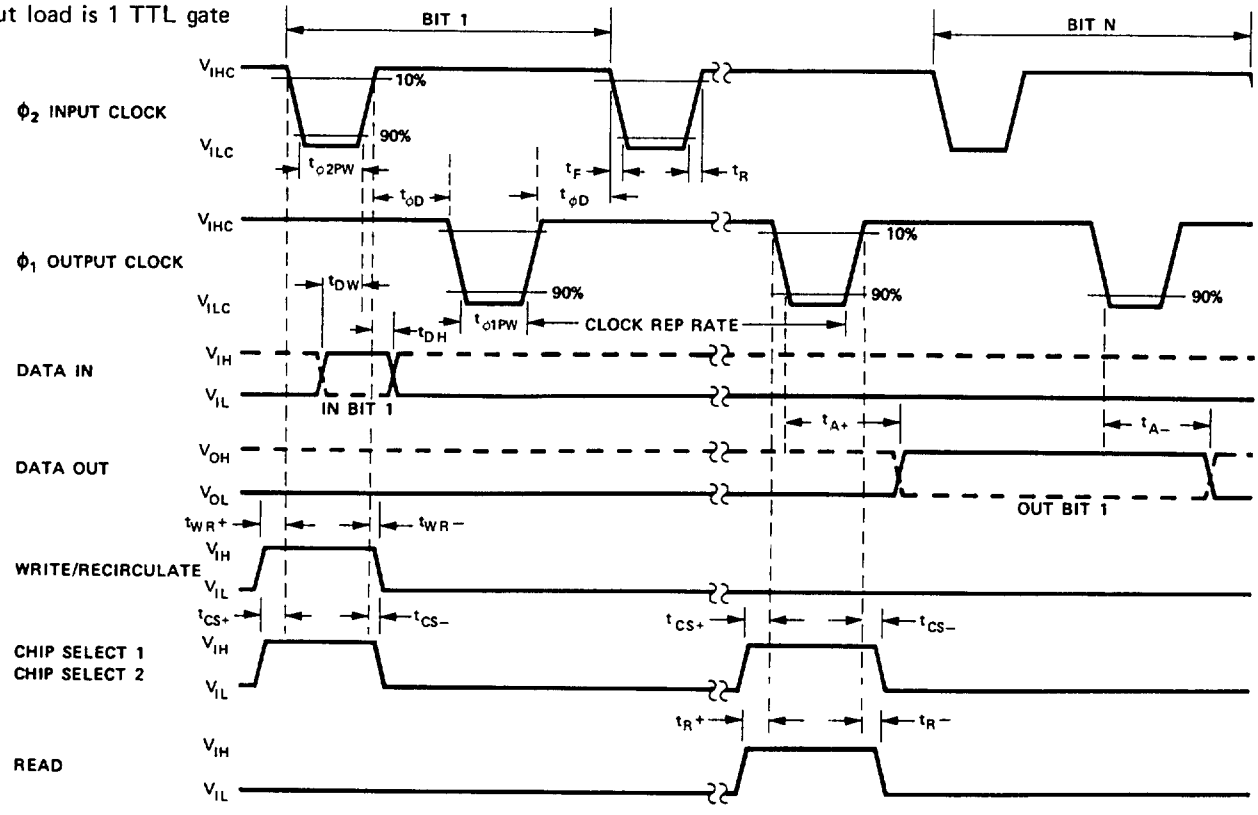
Note 1: See curve of Min Data Rate, and Max Clock Delay vs. Temp. on page 5. Note 2: Duty Cycle = $[t_{\phi PW} + \frac{1}{2}(t_R + t_F)]$ x clock rate.
Note 3: This parameter is periodically sampled and is not 100% tested.

Switching Characteristics

Conditions of Test

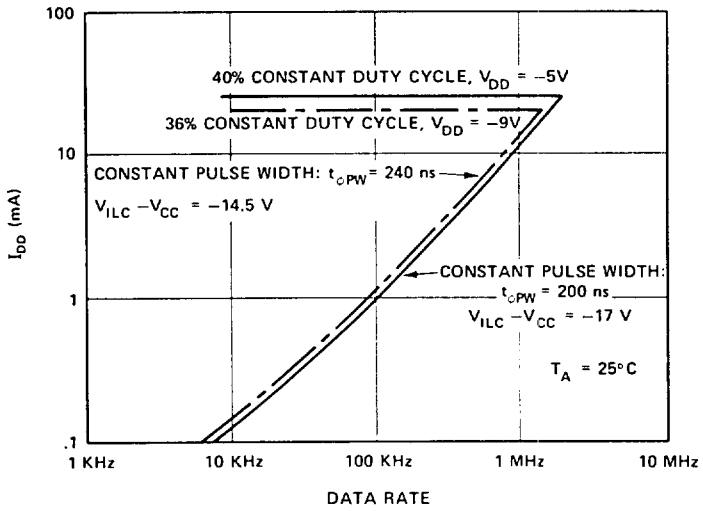
Input rise and fall times: 10 nsec
Output load is 1 TTL gate

Timing Diagram

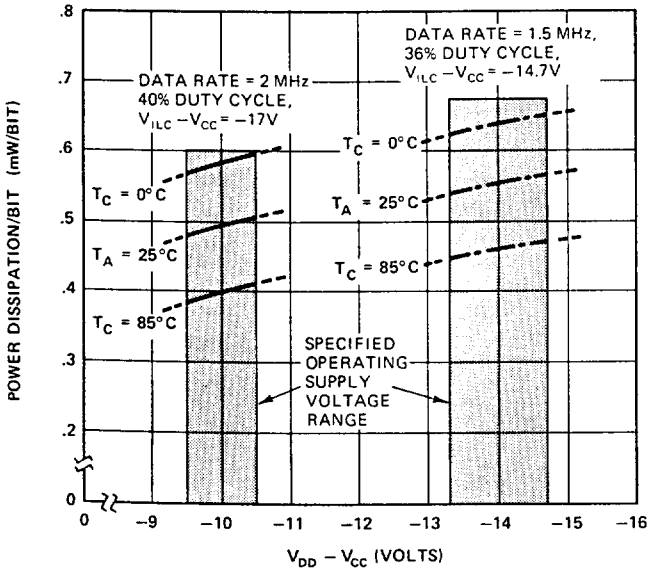


Typical Characteristics

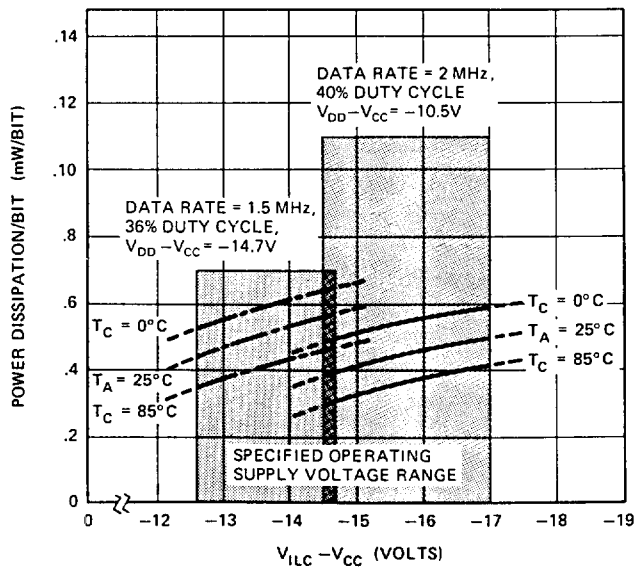
I_{DD} CURRENT VS. DATA RATE



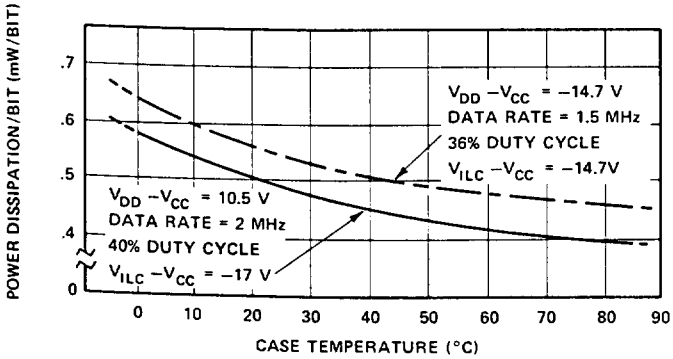
POWER DISSIPATION/BIT VS. SUPPLY VOLTAGE



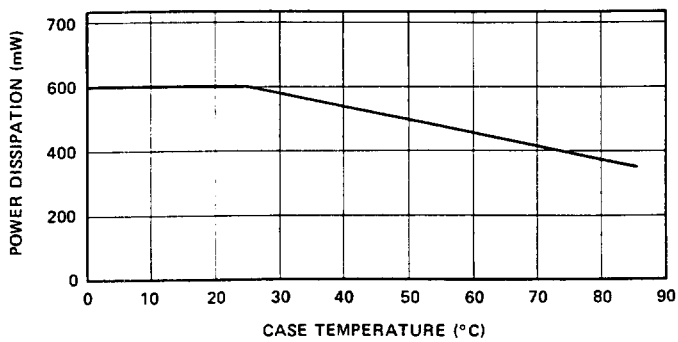
POWER DISSIPATION/BIT VS. CLOCK AMPLITUDE



POWER DISSIPATION/BIT VS. TEMPERATURE



MAXIMUM PACKAGE POWER DISSIPATION



Maximum Guaranteed Ratings *

Case Temperature Under Bias	0°C to +85°C
Storage Temperature	−65°C to +160°C
Power Dissipation(1)	600 mW
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+.3V to −20V

* COMMENT:

Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics T_{CASE} = 0°C to +85°C, V_{CC} = +5V ±5%, unless otherwise specified

V_{DD} = −5V ± 5%

SYMBOL	TEST	MIN.	TYP.(2)	MAX.	UNIT	CONDITIONS
I_{LI}	INPUT LOAD CURRENT		10	1000	nA	$V_{IN} = V_{IH}$ to V_{IL}
I_{LO}	OUTPUT LEAKAGE CURRENT		10	1000	nA	V_{OUT} = 0.0V
I_{LC}	CLOCK LEAKAGE CURRENT		10	1000	nA	$V_{ILC}=V_{CC}-17V$
I_{DD1}	POWER SUPPLY CURRENT		25	40	mA	T_A=25°C, Output at Logic "0", 2 MHz Data Rate, 40% Duty Cycle, Continuous Operation,
I_{DD2}	POWER SUPPLY CURRENT			45	mA	T_C=0°C, $V_{ILC}=V_{CC}-17V$
V_{ILC1}	CLOCK INPUT LOW VOLTAGE	$V_{CC}-17$		$V_{CC}-14.5$	V	
V_{IHC}	CLOCK INPUT HIGH VOLTAGE	$V_{CC}-1$		$V_{CC}+.3$	V	
V_{IL}	INPUT "LOW" VOLTAGE	$V_{CC}-10$		$V_{CC}-4.2$	V	
V_{IH1}	INPUT "HIGH" VOLTAGE	$V_{CC}-2$		$V_{CC}+.3$	V	
V_{OL}	OUTPUT LOW VOLTAGE		−.3	0.5	V	R_{L1}=3K to V_{DD}, I_{OL}= 1.6 mA
V_{OH}	OUTPUT HIGH VOLTAGE DRIVING TTL	2.4	3.5		V	R_{L1}=3K to V_{DD}, I_{OH}= −100 μA
V_{OH1}	OUTPUT HIGH VOLTAGE DRIVING MOS	$V_{CC}-1.5$	$V_{CC}-1$		V	R_{L2}=5.6K to V_{DD} (see p. 6 for connection)

V_{DD} = −9V ± 5%

I_{LI}	INPUT LOAD CURRENT		10	1000	nA	$V_{IN} = V_{IH}$ to V_{IL}
I_{LO}	OUTPUT LEAKAGE CURRENT		10	1000	nA	V_{OUT} = 0.0V
I_{LC}	CLOCK LEAKAGE CURRENT		10	1000	nA	$V_{ILC}=V_{CC}-14.7V$
I_{DD3}	POWER SUPPLY CURRENT		20	31	mA	T_A =25°C, Output at Logic "0", 1.5 MHz Data Rate, 36% Duty Cycle, Continuous Operation,
I_{DD4}	POWER SUPPLY CURRENT			36	mA	T_C =0°C, $V_{ILC}=V_{CC}-14.7V$
V_{ILC2}	CLOCK INPUT LOW VOLTAGE	$V_{CC}-14.7$		$V_{CC}-12.6$	V	
V_{IHC}	CLOCK INPUT HIGH VOLTAGE	$V_{CC}-1$		$V_{CC}+.3$	V	
V_{IL}	INPUT "LOW" VOLTAGE	$V_{CC}-10$		$V_{CC}-4.2$	V	
V_{IH2}	INPUT "HIGH" VOLTAGE	$V_{CC}-1.8$		$V_{CC}+.3$	V	
V_{OL}	OUTPUT LOW VOLTAGE		−.3	0.5	V	R_{L1}=5.6K to V_{DD} I_{OL}= 1.6 mA
V_{OH}	OUTPUT HIGH VOLTAGE DRIVING TTL	2.4	3.5		V	R_{L1}=5.6K to V_{DD}, I_{OH}=−100 μA
V_{OH1}	OUTPUT HIGH VOLTAGE DRIVING MOS	$V_{CC}-1.6$	$V_{CC}-1$		V	R_{L2}=6.2K to V_{DD} (See p. 6 for R_{L3}=3.9K to V_{CC} connection)

Note 1: For operating at elevated temperatures the device must be derated based as shown on page 3. In typical applications a case temperature of 85°C corresponds to 70°C for the low profile TO-99. In applications the duty cycle should be a minimum to reduce power dissipation. Duty cycle = $[t_{\phi PW} + \frac{1}{2}(t_R + t_F)]$ x clock rate.

Note 2: Typical values are at T_A = 25°C and at nominal voltages.

intel

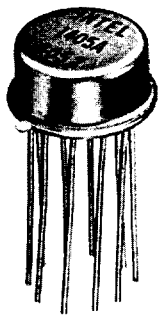
Silicon Gate MOS LSI Shift Register **1405A**

INTEL CORP. 3065 Bowers Avenue, Santa Clara, California 95051 • (408) 246-7501

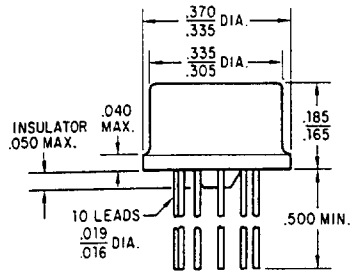
JUNE 1971

512 BIT DYNAMIC RECIRCULATING SHIFT REGISTER

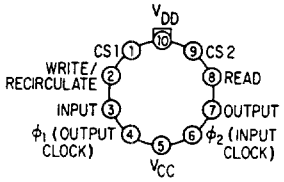
- **High Frequency Operation -- 2 MHz Guaranteed over Temperature.**
- **DTL, TTL Compatible**
- **Write/Recirculate and Read Controls Incorporated on the Chip**
- **Low Power Dissipation--.3 mW/bit at 1 MHz**
- **Low Clock Capacitance--85 pF**
- **Low Clock Leakage -- ≤1 uA at –17 V**
- **Simple Two Dimensional Memory Matrix Organization -- 2 Chip Select Controls**
- **Inputs Protected Against Static Charge**
- **Standard Packaging--10 Lead Low Profile TO-99**



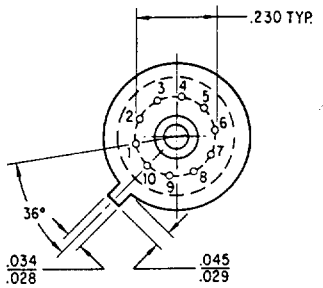
PACKAGE OUTLINE



PIN CONFIGURATION

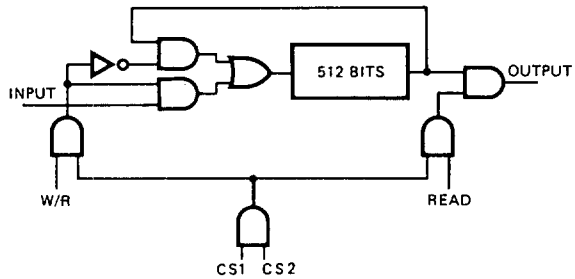


Top View



Bottom View

LOGIC DIAGRAM



MODE \ PIN	W/R (2)	CS1 (1)	CS2 (9)	READ (8)
WRITE	1	1	1	1 or 0
RECIRCULATE(1)	1 or 0	1 or 0	1 or 0	1 or 0
READ	1 or 0	1	1	1

Note 1: Either W/R, CS1, or CS2 must be a "0" during Recirculation.
A logic 1 is defined as a high input and a logic 0 as a low input.

The 1405A is a 512 bit dynamic recirculating shift register and is a direct pin replacement for the 1405. The 1405A is capable of operating at power supply voltages of +5V, –9V as well as +5V, –5V. A high speed recirculating data rate of 2 MHz over the temperature is easily obtained at the +5, –5 power supplies.

Write/recirculate and read controls eliminate the need for external logic elements when recirculating data. In addition, any number of devices can be combined to form a multi-dimensional memory array. For this purpose two chip select controls have been provided.

These registers can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.) or by MOS circuits. The design of the output stage provides driving capability for both MOS and bipolar IC's as well as OR-tieing of shift registers. The 1405A is ideally suited for usage in low cost memories or delay line applications.

Use of low threshold **silicon gate technology** allows high speed (2 MHz guaranteed) while reducing power dissipation by a factor of **two** and clock input capacitance by a factor of **three** over equivalent products manufactured by conventional technologies.