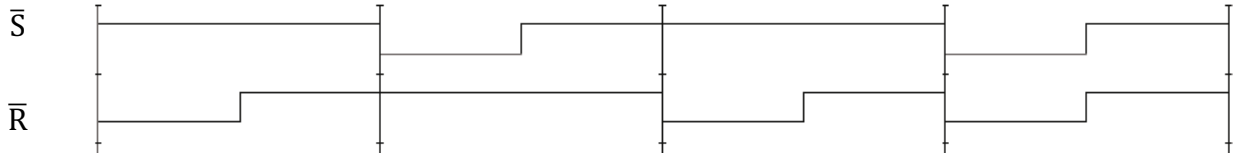
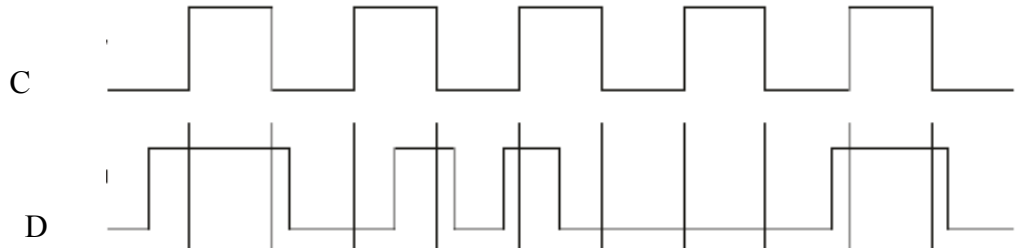
14:332:231-Digital Logic Design
Assignment 6
Due Date: 2:00 pm, 04/19/2023

1. The signals to the $\overline{S}$ and $\overline{R}$ inputs of a $\overline{S} - \overline{R}$ latch are shown below. Sketch the waveforms for the outputs Q and QN of this latch. Ignore the propagation delays.



2.

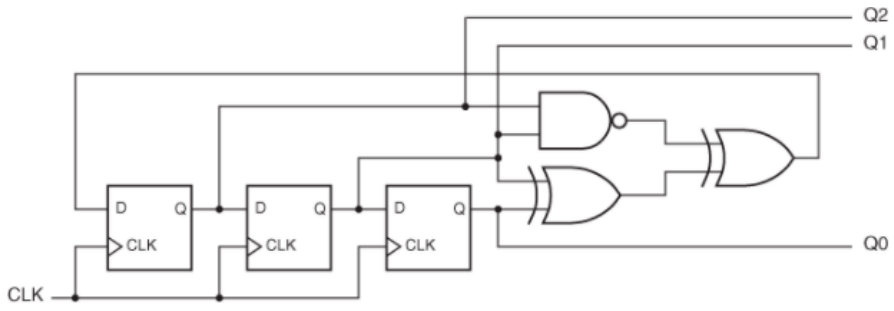
a) The signals for the C and D inputs for a D latch are shown below. Sketch the waveforms for the output Q for the D latch. Ignore the propagation delays. Assume the initial state for Q is 0.



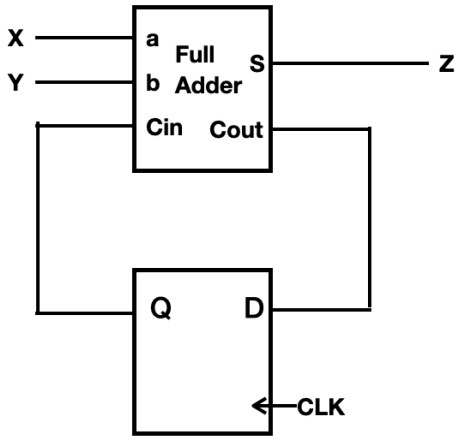
b) The C and D signals above were applied to the clock and D inputs of an edge-triggered D flip-flop. Sketch the waveforms for the output Q for the D flip-flop. Ignore the propagation delays. Assume the initial state for Q is 0.

3. For the state machines shown below
i) derive the state/output table,
ii) derive the state diagram.

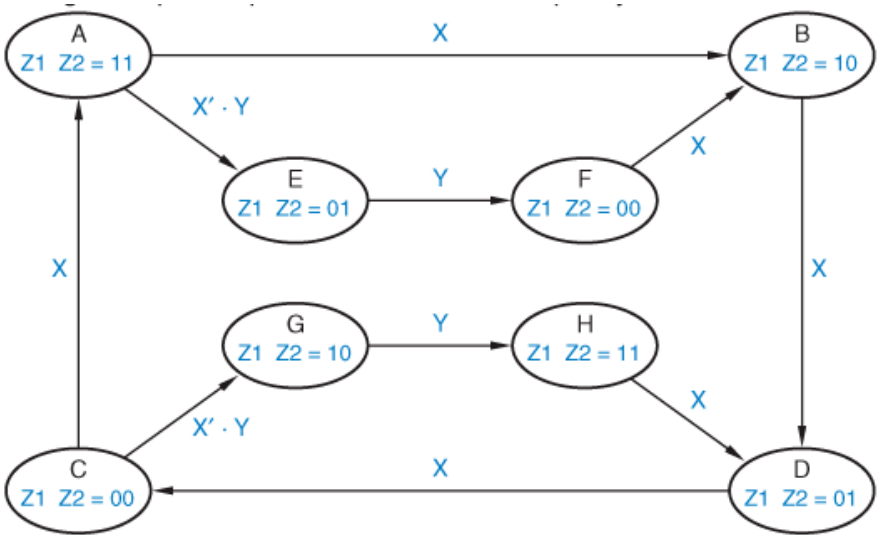
a)



b)



4. For the state diagram shown, derive the state/output table.



5. Draw a state machine diagram for a traffic light controller that works as follows: A timing signal T is the input to the controller. T defines the yellow light interval, as well as the changes of the red and green lights. The outputs to the signals are defined below:

GN: Green Light, (North/South signal);
YN: Yellow Light (North/South signal);
RN: Red Light (North/South signal);

GE: Green Light (East/West signal)
YE: Yellow Light (East/West signal)
RE: Red Light (East/West signal)

While T=0, the green light is on for one signal and the red light for the other. With T=1, the yellow light is on for the signal that was previously green, and the signal that was previously red remains red. When T becomes 0, the signal that was previously yellow becomes red, and the signal that was previously red becomes green. This pattern of alternating changes in color continues. Assume that the controller is synchronous with a clock that changes much more frequently than input T.