Laboratory 4: A Simple 4-bit Arithmetic Logic Unit (ALU)

Learning Objectives

- Learn how a basic ALU works
- Analyze 2's complement's arithmetic
- Synthesize a simple 4-bit ALU

In this lab, you will design, simulate and build a circuit performing addition/subtraction/increment /decrement of 4-bit words in two's-complement representation. The 2's complement representation for 4-bit words is presented below. Make sure that you are familiar with this representation .

Decimal Representation	Two's complement Representation
-8	1000
-7	1001
-6	1010
-5	1011
-4	1100
-3	1101
-2	1110
-1	1111
0	0000
+1	0001
+2	0010
+3	0011
+4	0100
+5	0101
+6	0110
+7	0111

Your ALU will be built around a 4-bit binary adder. To perform other operations beside addition you will have to use a multiplexer for each bit as well as a few additional gates. The nature of the operation is controlled by the inputs S0 and S1.

Code S1S0	Operation
00	Addition
01	Subtraction
10	Increment
11	Decrement

After you have designed the complete unit, you will predict the result of several operations and then implement it in hardware. In the final report you will be asked to explain the results of the computations.

The theoretical background required for this lab are:

- two's-complement representation
- arithmetic operations with two's-complement representation
- 4-bit binary adder (the IC used in this lab is 74LS283, please read the datasheet: https://www.ti.com/lit/gpn/sn74s283)

List of ICs used in this lab:

IC Number	Operation	Qty
74LS04	Hex inverter	1
74LS86A	Quad 2-input XOR	1
74LS153	4-input, 2-bit (dual 4-to-1) MUX	2
74LS283	4-bit Binary Adder	1

1. Pre-Lab

For the prelab, you have two tasks. You are asked to design the Arithmetic Logic Unit using the available hardware, which is a 4-bit Binary Adder (74LS283), 4-to-1 multiplexers, and logic gates.

1.1 Design of the 4-bit Arithmetic Logic Unit (ALU)

Since all four bits are processed the same way, you have to design only the handling of one bit. Let the two binary words used in addition or subtraction be X3X2XlXO (X[3:0]) and Y3Y2Y1YO (Y[3:0]) . The structure of your circuit (for one bit) should be like in Figure 1.

The first addend X is applied directly to the adder. To perform all four desired operations with the adder, the second addend must be chosen with the help of the two control variables S1S0.

However, to know how to wire the four inputs of the 4-to-1 multiplexer to either of the signals: a bit of Y, the complement of the same bit, logic '0', logic 'l', you must decide first about the carry-in generation circuit. **The order of MUX inputs in Figure 1 is not correct! To design the circuit, you need to determine the correct order and include in your pre-lab report.**

Recall that in the two's-complement subtraction you need to have the CIN signal asserted to logic 'l'. You can implement the increment operation as setting Y [3:0] to 0000 but providing an asserted CIN signal. Similarly, the decrement operation can be implemented as an addition with -1.

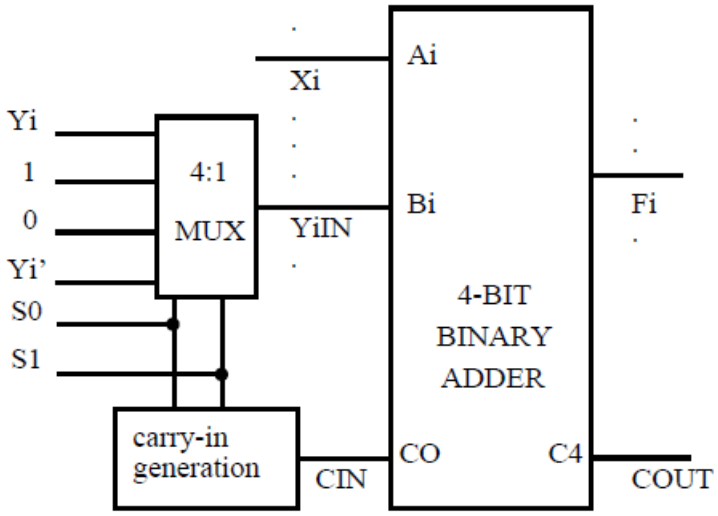

Figure 1: Structure of the 4-bit Arithmetic Logic Unit (ALU)

Why should the increment /decrement be done this way? Examine the control codes for subtraction and increment, the two operations when CIN is asserted to one. You should be able to see how simple the carry-in generation circuit is. The multiplexer inputs should be easy to derive now from the way the operations were defined.

1.2 Simulation using Xilinx Vivado (Optional)

1. Write the code for synthesizing the 4-bit ALU. Include this code in your prelab report.

2. Open the elaborated design under the RTL analysis tab. Submit the Elaborated design schematic diagram with your prelab report. This diagram will contain the schematic for the ALU.

3. Create a simulation file in Vivado and write the code for running the simulation for each possible combinations of the selection bits S1S0 for X [3:0] = +6 and Y[3:0] = -1.

4. Simulate the testbench and obtain the timing diagram which demonstrates each of the possible input combinations along with the corresponding output.

1.3 Pre-lab Report

Your pre-lab report should contain the following
- Discussion of how you arrived at your design.
- The logic diagram of the circuit implementing the 4-bit arithmetic unit.
- The truth table of the investigated case.
- Your code for the synthesis of the circuit (optional)
- Schematic for the Elaborated Design obtained under the RTL Analysis tab of Vivado (optional)
- The timing diagram obtained from the simulation using Vivado (optional)

2.Experiments

2.1 Experiment A

1. Build the ICOD that you used in Lab1 with 4 switches and 4 LED's. Check that the ICOD on your breadboard is working properly, by toggling each of the input pins from logic '0' (GND) to logic '1' (5V), and from logic '1' (5V) to logic '0' (GND).

2. There are ten input signals. Use two switches of the ICOD unit to have access to the control signals SO and Sl. The other two switches should be connected to X3 and Y3, i.e. the sign bit s of the two operands. Connect the four LEDs to the output bits of the adder, FO to F3. The COUT signal should be checked with the logic probe. **This arrangement will remain the same for all the experiments performed in this lab.**

3. Using the switches set both sign bits to logic '0'.

4. Connect with wires the bits X2, X1 and XO to logic '0' or logic '1' so that X[3:0] represents +2.

5. Similarly, connect Y2, Yl and YO so that Y [3:0] represents +5.

6. Using the 2 switches for control bits S1 and S0, verify that all the operations are being successfully performed and fill the following truth table.

Decimal X Y	Operation	Result		
		Binary	Decimal	COUT
	Addition			
	Subtraction			
	Increment			
	Decrement			

2.2 Experiment B

1. Change Y3 to logic ' 1' with the switch. What is the number represented now by Y[3:0]?

2. Using the 2 switches for control bits S1 and S0, verify that all the operations are being successfully performed and fill the following truth table.

Decimal X Y	Operation	Result		
		Binary	Decimal	COUT
	Addition			
	Subtraction			
	Increment			
	Decrement			

2.3 Experiment C

1. Change X3 also to logic ' 1' with the switch. What is the number represented now by X[3:0]?

2. Using the 2 switches for control bits S1 and S0, verify that all the operations are being successfully performed and fill the following truth table.

Decimal X Y	Operation	Result		
		Binary	Decimal	COUT
	Addition			
	Subtraction			
	Increment			
	Decrement			

2.4 Experiment D

1. Set the sign bit X3 to logic '0' and let the sign bit Y3 to be logic ' l'.

2. Change X [3:0] from +2 to +3 by moving the X0 wire from logic '0' to logic '1'. Execute addition and record the result as well as the value of COUT.

3. Lab 4 Report

Your report for Lab 3 should include the following:

- Your prelab report with all the materials requested

- Completed tables from Experiments A, B and C with discussion of the results, and discussion of the results obtained in Experiment D

- Images of the circuits that you implemented to realize the ALU