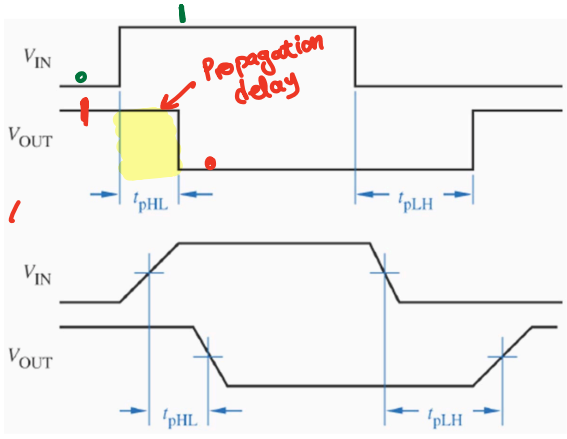
Timing Hazards

Propagation Delay: In real circuits, when the input to a logic gate changes, the output does NOT change immediately.

This is because switching elements in the gate take time to react.

As a result, the change in the output is *delayed* with respect to the time that the input was changed.

This delay is referred to as the "*propagation delay*".



Some Definitions:

Steady-State Behavior: output of logic circuit as a function of its inputs under the assumption that the *inputs have been stable* for a *long time*. "Long" here is relative to the delays in the circuit.

Transient Behavior: due to gate delays, logic circuits exhibit transient behavior. The transient behavior of a combinational logic circuit may *differ* from what is predicted by a steady-state analysis.

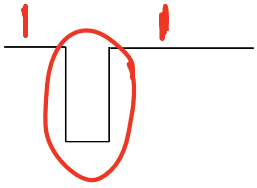
Glitch: is an *unwanted pulse* at the output of a combinational logic circuit (a momentary change in an output that should not have changed).

Hazard: A *circuit* with the *potential for a glitch* is said to *have a hazard*. A hazard is something intrinsic about a circuit; a circuit with hazard may or may not have a glitch depending on input patterns and the electric characteristics of the circuit.

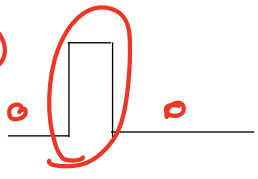
Hazards occur in the output when *different paths from input to output* have *different propagation delays*.

Static Hazard: The *output* undergoes a *momentary transition* when it is *expected to remain unchanged*.

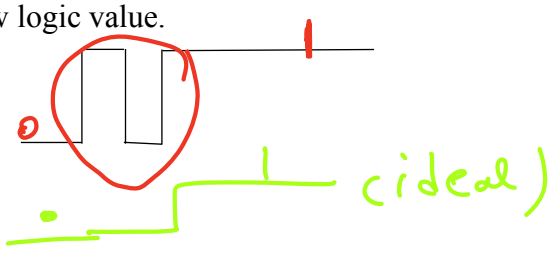
Static-1 Hazard:



Static-0 Hazard:

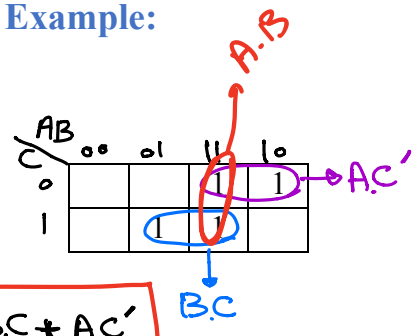


Dynamic Hazard: The *output is supposed to change*, but it *changes multiple times in between*, before it settles to its new logic value.

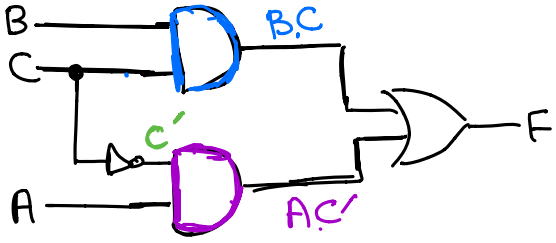


Detection of Static Hazards & Designing Hazard-Free Circuits

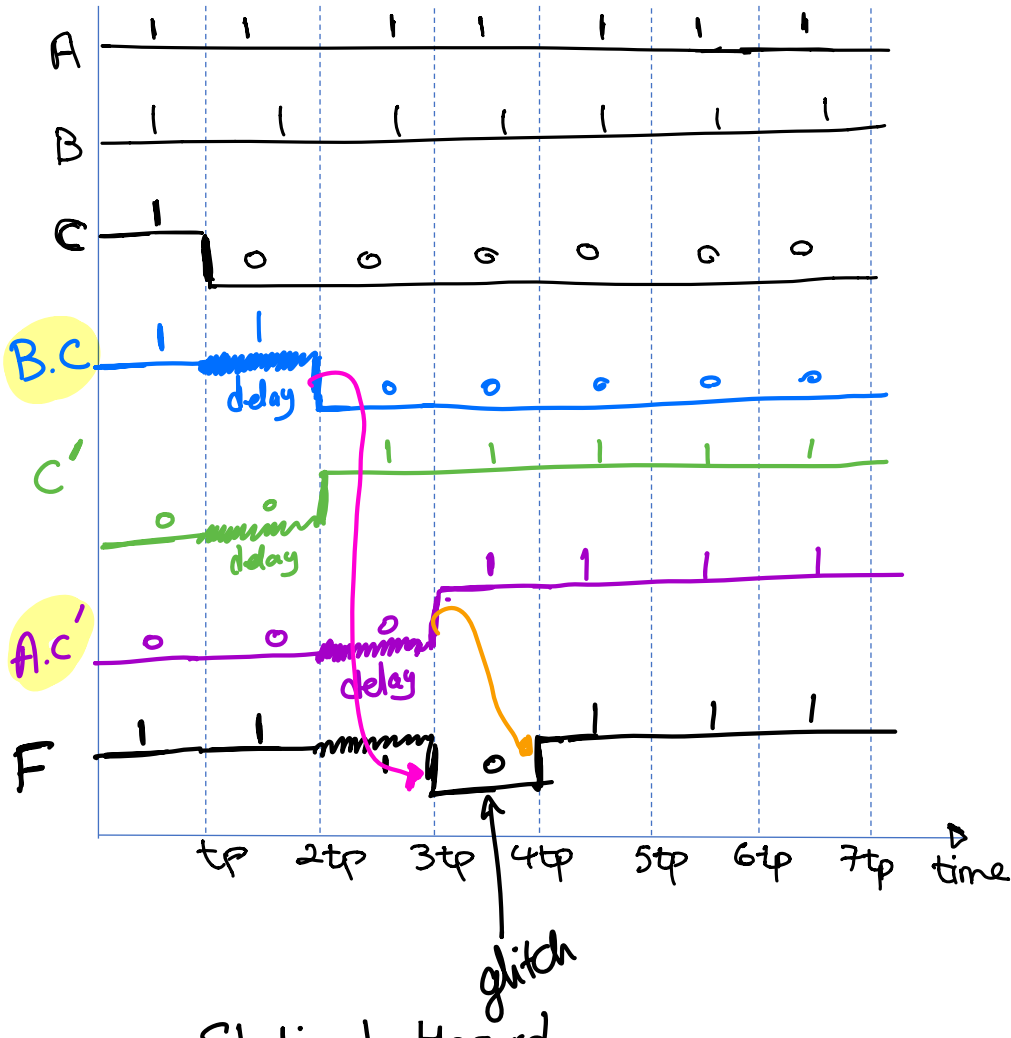
Example:



$F = B.C + A.C'$



Assume each gate has propagation delay of tp.



A=1, B=1, C=1 → f=1

A=1, B=1, C=0 → f=1

Static-1 Hazard

Observations:

- When representing a function as a Sum-of-Products (AND-OR) circuit, the AND gates correspond to the prime implicants of the K-Map.
- Change in the input "C" (from 1->0) propagates to the output F along two paths with different delays. This difference has caused the glitch in the output.
- A hazard happened when there is a *transition* between *prime implicants* (i.e. between the AND gates).

Detection of Static-1 Hazards:

- A potential hazard exists when two *adjacent 1-cells* in a K-Map are NOT covered by a single product term (prime implicant) in the circuit.

- Note that *two-level OR-AND* circuits (based on POS) *have no static-1 hazard*.

Detection of Static-0 Hazards:

- A potential hazard exists when two *adjacent 0-cells* in a K-Map are NOT covered by a single sum term in the circuit.

- Note that *two-level AND-OR* circuits (based on SOP) *have no static-0 hazard*.

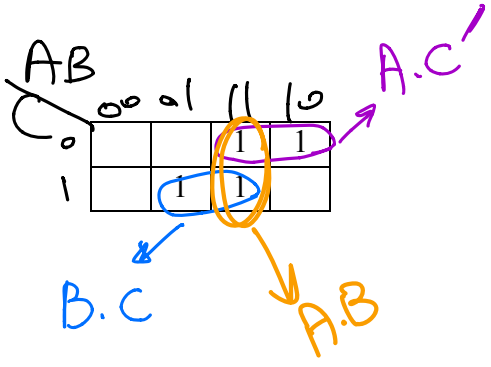
Approaches for Eliminating Hazards:

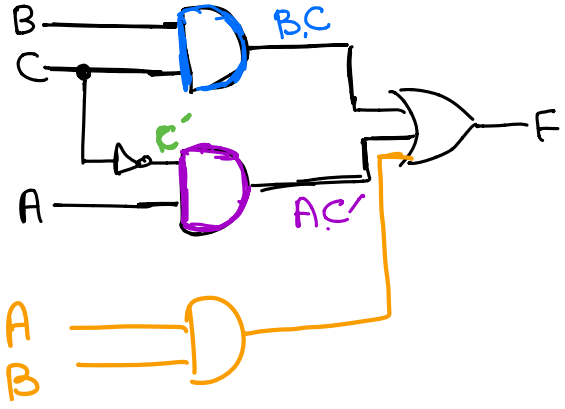
1. Wait! Evaluate the output at intervals that are longer than the maximum propagation delay in the circuit.

2. Match propagation delays: make sure propagation delays from input to output for different paths in the circuit are the same. In the example above, you could add a buffer in the top row. In practice, matching the propagation delays in different paths is difficult to achieve. e.g. you could add a buffer gate before the top AND gate

3. Add redundant prime implicants: find the prime implicant that covers all adjacent 1-cells, and add it as an extra product term to the function.

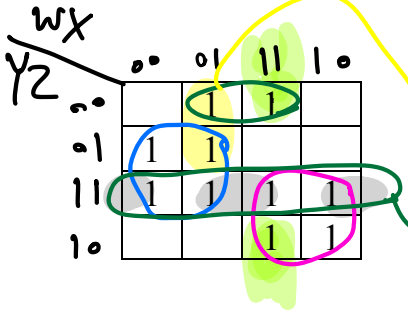
Example:





SoP

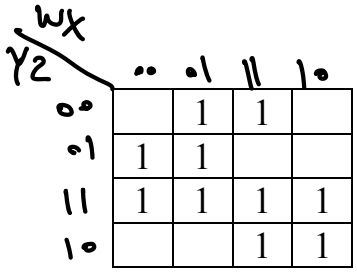
Example (Static-1 Hazard):



$F(YZWX) = Z.W' + Y.W + Y'.Z'.X$

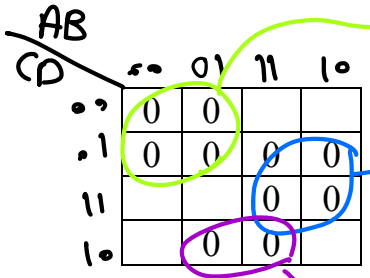
$Y'.W'.X$
$Y.Z$
$Z'.W.X$

Redundant Prime implicants that need to be added so the circuit stay static Hazard-free.



POS

Example (Static-0 Hazard):

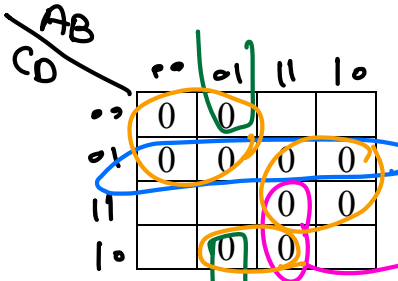


$(A+C)$

$(A'+D')$

$(B'+C'+D)$

$F(A,B,C,D) = (A+C).(A'+D').(B'+C'+D)$



$(C+D')$

$(A'+B'+C')$

$(A+B'+D)$

Need to add $(C+D')$, $(A'+B'+C')$ $(A+B'+D)$ to $F(A,B,C,D)$ to eliminate Static-0 Hazard.

Example (Dynamic Hazard):

If there are multiple paths from an input (or its complement) to the output, the circuit has a potential for a dynamic hazard. Analysis and elimination of dynamic hazards is a complicated process, and usually solved by computer programs.