14:332:231-Digital Logic Design

Assignment 3

Due Date: 2:00 pm, 02/22/2023

1. Optimize the following expressions in the form of sum-of-products using an appropriate K-map. Identify essential prime implicants.

a. F(X, Y, Z) = $\sum_{X,Y,Z}(0, 2, 4, 6, 7)$

b. F(X, Y, Z) = X′Y′+XZ′+Y′Z+X′YZ′

c. F(X, Y, Z,W) = $\sum_{X,Y,Z,W}(0, 2, 4, 5, 8, 10, 11, 15)$

d. F(X, Y, Z,W) = $\sum_{X,Y,Z,W}(1, 4, 5, 6, 10, 11, 12, 13, 15)$

e. F(X, Y, Z,W) = $\sum_{X,Y,Z,W}(1, 5, 6, 7, 11, 12, 13, 15)$

2. Optimize the following expressions in the form of product-of-sums using an appropriate K-map.

a. F(X, Y, Z,W) = $\sum_{X,Y,Z,W}(0, 1, 2, 8, 10, 12, 14, 15)$

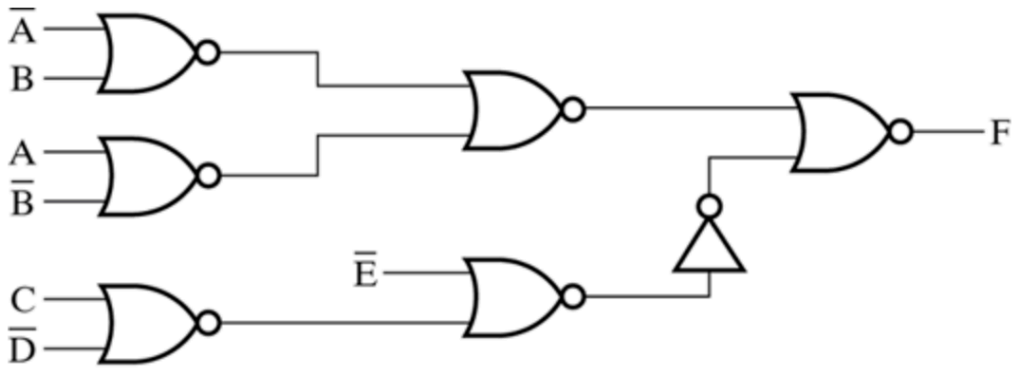
b. F(X, Y, Z,W) = $\prod_{X,Y,Z,W}(0, 2, 6, 7, 8, 9, 10, 12, 14, 15)$

3. Optimize the following expressions in the forms of sum-of-products and product-of-sums using an appropriate K-map.

a. F(X, Y, Z,W) = $\sum_{X,Y,Z,W}(5, 6, \ 11\ , 12)$, d(X, Y, Z,W) = $\sum_{X,Y,Z,W}(0, 1, 2, 9, 10, 14, 15)$

b. F(X, Y, Z,W) = $\prod_{X,Y,Z,W}(3, 4, 6, 11, 12, 14)$, d(X, Y, Z,W) = $\sum_{X,Y,Z,W}(0, 1, 2, 7, 8, 9, 10)$

4. In the following circuit, the NOR gates have propagation delay of $t = 0.073$ ns and the inverter has a propagation delay of $t = 0.048$ ns. Find the propagation delay of the longest path through the circuit.



5. For the following logic expressions, find all of the static hazards in the corresponding two-level AND-OR circuit using a K-Map, and design a hazard-free circuit that realizes the same logic function:

a. F(X,Y,Z)= X.Y+X′Z′

b. F(W,X,Y,Z)= W′X+Y′Z+W′XYZ+WXYZ′

6. Using a truth table, find the expression of the sum-of-products and the AND-OR circuit realization for a) a 2-input XOR gate, and b) a 2-input XNOR gate.

7. Using K-Maps design a logic circuit that accepts the binary input $a_4a_3a_2a_1a_0$, and generates an output in the form of b_1b_0. In this circuit if the input is "1" (that is $a_4a_3a_2a_1a_0=00001$) or if it is a prime number other than 2, the output should be $b_1b_0=01$. If the input is an even number, the output should be $b_1b_0=10$. In other cases the output can be $b_1b_0=00$ or $b_1b_0=11$. Realize this circuit using only NAND gates.