Digital Logic Design

Dov Kruger

Department of Electrical and Computer Engineering
Rutgers University

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Welcome to DLD!

Syllabus: `github.com/RU-ECE/ECE231-DigitalLogicDesign/main/syllabus.md`

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Course Topics

- Background: basic electricity and electronics
- Practical skills to design digital circuits and debug them in lab
- Digital Logic
- Number systems
- Analysis and synthesis of combinational circuits
- Decoders/encoders, multiplexers/demultiplexers
- Arithmetic systems, comparators, adders, multipliers
- Sequential circuits, latches, flip-flops
- Registers, shift registers, counters, LFSRs
- Finite state machines, analysis and synthesis
- Verilog programming to implement these circuits

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Textbook Information

- Text: J. F. Wakerly, *Digital Design Principles and Practices*, 5/e, Pearson, 2018

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Expectations

- No electronics is assumed (but you should be taking PE1)
- No programming experience is assumed
- Learn to draw schematics in a CAD package
- Learn to program in Verilog but not for full demonstration

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Primary Expectations

- Come to class regularly
- Do not email me when you are sick, unless you are out multiple times
- Attendance not taken, but attendance quizzes given out in class
- No excuses for missing attendance inclass work, but at least two absences ignored
- If test results are great, attendance will be ignored
- If test results not good, curving applied only if attendance is good
- If $> 90\%$ of class fills out reviews, $+1$ on final.
- Map to letter grade depends on class average, please do not ask

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Primary Expectations, Labs

- Prepare for each lab by reading the lab in advance
- Submit pre-lab questions before the lab
- Pre-labs are *individual work*
- Submit lab report within 1 week of completion of the lab
- Late lab reports will not be accepted
- For serious illness, contact your TA. They will contact me

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Grading Policies

- syllabus on the home page of the course
- `https://rutgers.instructure.com/courses/293365`

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Why Cover Basic Electricity?

- This course does not cover circuits.
- We focus on digital logic: 1 and 0, true and false.
- But in order to do the labs, you have to:
  - Build circuits.
  - Debug circuits.
- We will do a quick circuits overview complementary to PE1
- We will review common errors observed in labs

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Getting Help

- I have office hours (definitely try, historically few use them)
- Link on home page of course:
  `https://rutgers.instructure.com/courses/293365`
- I am outnumbered: 262+ students this semester!
- TAs also have office hours
- Get help immediately if you do not understand something

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Attendance

Attendance exercises will be given out every week during class.
Purpose:

- Encourage active learning.
- Practice what I am teaching immediately
- Email your TA in advance if you will be missing class
- Do not email me about attendance unless you have a longterm problem
- Take any attendance classes in makeup sessions conducted by a TA
- Scores are 1 (attended) 0 (missed) 0.5 (made up)
- DO NOT EMAIL ME if you miss one. Missing one or two is not an issue
- If you do A work as shown on your tests, you will still get an A
- Curving is contingent on good attendance

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Academic Honesty and Your Skills

- Your goal should be to learn and become skilled in computer engineering
- Cheating just means you are not learning
- Any work found not to be your own will be scored as zero and reported to the department chair

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Preparation: Installing Software

- CAD: Fritzing, tinkercad (online), KiCAD, others
- Compiler: iverilog
  - Install on your computer if possible
  - If not, run online or use the computer lab
- Optional software available
  - Xilinx Vivado (65GB, complicated but eventually needed)
  - msys2 (Windows) Linux command line
  - vscode (programming editor and IDE)

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Preparation: CAD

- All circuits must be drawn in CAD
- Easiest: Fritzing, tinkercad (online)
- CircuitLab `https://www.circuitlab.com/`
- Optional: More complex KiCAD, Eagle, LTSpice

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Optional Software

- Installing a linux-like command line on Windows (msys2)
- Installing a programming editor (vscode)

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