

VM & ISA

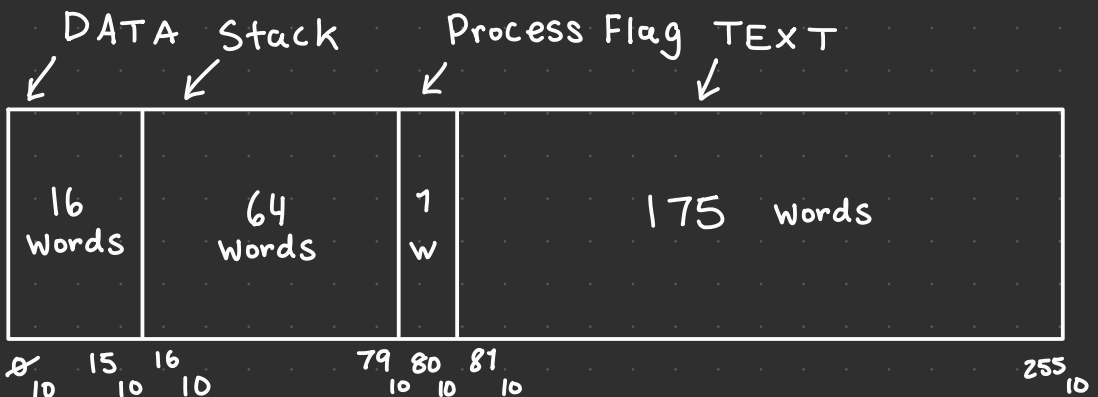
Documentation
& user manual

Virtual Hardware

The hardware's smallest (and largest) unit of memory is a **word**. A word is **8 bits** long.

There consists **4 Registers** all **1 word** in size. Of these registers there are **2 General Purpose ($R0, R1$)**, **1 Stack Pointer (SP)**, and **1 Program counter (PC)**.

The **memory** is **256 words** long. It is laid out below:



Instructions

| Name | Args | C-Like Effect |
|------|------|---------------|
|------|------|---------------|

| | | |
|-----|-------|-----------|
| Mov | Ra Rb | $Ra = Rb$ |
|-----|-------|-----------|

| | | |
|-----|-------|---------------------|
| Cmp | Ra Rb | $Mem(80) = Ra - Rb$ |
|-----|-------|---------------------|

| | | |
|-----|-------|------------------|
| Shl | Ra Rb | $Ra = Ra \ll Rb$ |
|-----|-------|------------------|

| | | |
|-----|-------|------------------|
| Shr | Ra Rb | $Ra = Ra \gg Rb$ |
|-----|-------|------------------|

| | | |
|-----|-------|----------------|
| Add | Ra Rb | $Ra = Ra + Rb$ |
|-----|-------|----------------|

| | | |
|-----|-------|----------------|
| Sub | Ra Rb | $Ra = Ra - Rb$ |
|-----|-------|----------------|

| | | |
|-----|-------|-----------------|
| And | Ra Rb | $Ra = Ra \& Rb$ |
|-----|-------|-----------------|

| | | |
|-----|-------|----------------|
| OrR | Ra Rb | $Ra = Ra Rb$ |
|-----|-------|----------------|

| | | |
|-----|----|----------------|
| Not | Ra | $Ra = \sim Ra$ |
|-----|----|----------------|

| | | |
|-----|----|----------------------|
| Psh | Ra | $Mem[SP] = Ra, SP++$ |
|-----|----|----------------------|

| | | |
|-----|----|----------------------|
| Pop | Ra | $SP--, Ra = Mem[SP]$ |
|-----|----|----------------------|

| | | |
|-----|----|---|
| Sys | Ra | $Syscall(Ra, \text{argc}, \text{argv})$ |
|-----|----|---|

JMP is Special

| | | |
|-----|-----------|--|
| Jmp | mask Addr | if $Mem(80) \& \text{mask} : PC = \text{Addr}$ |
|-----|-----------|--|

| | | |
|------|---------|------------|
| Ld ± | Ra, Imm | $Ra = Imm$ |
|------|---------|------------|

| | | |
|-----|---------|---------------------|
| LDA | Ra, Imm | $Ra = Mem(\pm Imm)$ |
|-----|---------|---------------------|

| | | |
|-----|---------|---------------------|
| STA | Ra, Imm | $Mem(\pm Imm) = Ra$ |
|-----|---------|---------------------|

See prev page ↗

LT EQ GT
100 010 001

↖ ↗

$Ra = Ra \ll Rb$

$Ra = Ra \gg Rb$

$Ra = Ra + Rb$

$Ra = Ra - Rb$

$Ra = Ra \& Rb$

$Ra = Ra | Rb$

$Ra = \sim Ra$

$Mem[SP] = Ra, SP++$

$SP--, Ra = Mem[SP]$

$N = Mem[SP] \quad Mem[SP+1 \dots N]$

$Syscall(Ra, \text{argc}, \text{argv})$

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if $Mem(80) \& \text{mask} : PC = \text{Addr}$

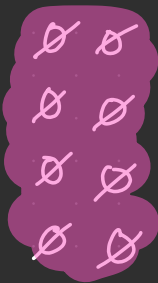




$Ra = Imm$

$Ra = Mem(\pm Imm)$

$Mem(\pm Imm) = Ra$

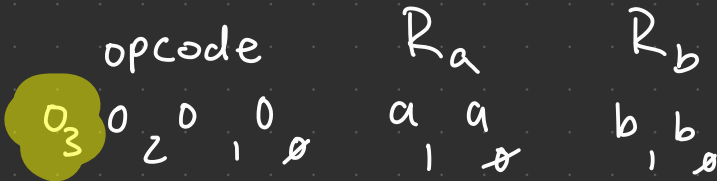
Note: Ra, Rb, mask, Imm serve as placeholders

Instruction Groupings

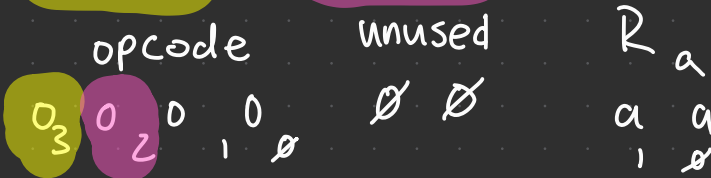
| <u>Type</u> | <u>Op Code</u> | <u>name</u> |
|------------------|---|-------------|
| X |  0 0 0 0 | Mov |
| | 0 0 0 1 | Cmp |
| | 0 0 1 0 | SHL |
| | 0 0 1 1 | SHR |
| X |  0 1 0 0 | ADD |
| | 0 1 0 1 | Sub |
| | 0 1 1 0 | AND |
| | 0 1 1 1 | ORR |
| Y |  1 0 0 0 | NOT |
| | 1 0 0 1 | PSH |
| | 1 0 1 0 | POP |
| | 1 0 1 1 | SYS |
| Z _J → |  1 1 0 0 | Jmp |
| Z |  1 1 0 1 | LDI |
| | 1 1 1 0 | LDA |
| | 1 1 1 1 | STA |

Instruction Types

X: O_3 is \emptyset



Y: O_3 is 1 & O_2 is \emptyset

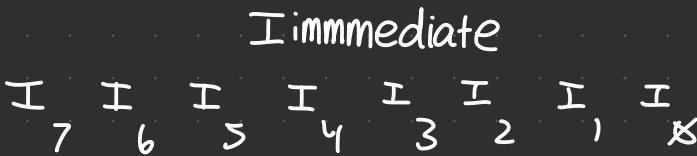


Z: O_3 is 1 & O_2 is 1 BUT: Z_J : Z & $O_1 = O_{\emptyset}$ is \emptyset

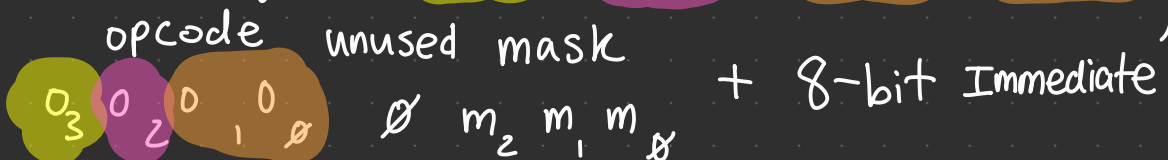


$\emptyset \emptyset R_a$ becomes:

mask
 $\emptyset m_2 m_1 m_{\emptyset}$



more explicitly Z_J : O_3 is 1 & O_2 is 1 & O_1 is \emptyset & O_{\emptyset} is \emptyset



Assembler Syntax

asm \rightarrow data text \$

data \rightarrow ".data" dataList
| λ

dataList \rightarrow dataItem dataList
| λ

dataItem \rightarrow [ident] "=" [immediate]

text \rightarrow ".text" textList

textList \rightarrow [ident] ":" textList
| Xinstruction textList
| Yinstruction textList
| Zinstruction textList
| λ

Xinstruction \rightarrow [Xcmd][Reg][Reg]

Yinstruction \rightarrow [Ycmd][Reg]

Zinstruction \rightarrow [Zcmd][Reg] ", " Zitem
| ZJinstruction

ZJinstruction \rightarrow [ZJcmd][Mask] ", " Zitem

Zitem \rightarrow [immediate]

| [ident]

System Calls

0₁₆ sys_Exit

1₁₆ sys_sleep

Note about sys_Exit & sys_sleep:

2₁₆ sys_Rand

3₁₆ sys_out_int

4₁₆ sys_out

System Calls Examples

Sys-Exit .

LDI R0, 0₁₀ } argv[0] = 0₁₀
PSH R0

LDI R0, 0₁₀ ← Sys-Exit
Sys R0 ← Syscall(R0, ~~argc~~, argv)
Sys-Exit(ExitCode)

Don't need to set since exit takes const Argc of 1

Sys-SLEEP :

LDI R0, 50₁₀ } argv[0] = 50₁₀
PSH R0

LDI R0, 1₁₀ ← Sys-sleep
Sys R0 ← Syscall(R0, ~~argc~~, argv)
Sys-sleep(TimeMS)

System Calls Examples Pt. 2

Sys_out:

LDI R0, 21₁₀ } argV[2] = 21₁₀ (l)
PSH R0

LDI R0, 105₁₀ } argV[1] = 105₁₀ (i)
PSH R0

LDI R0, 72₁₀ } argV[0] = 72₁₀ (H)
PSH R0

LDI R0, 3₁₀ } argC = 3₁₀
PSH R0

LDI R0, 2₁₀ ← Sys_out
Sys R0 ← syscall(R0, argC, argV)

Sys_out(Len, STR) ↑

Sys_Rand:

LDI R0, 3₁₀ ← Sys_Rand
Sys R0 ← syscall(R0, ~~argC~~, ~~argV~~) Sys_Rand(void) ↓
POP R0 ← move Return into R0