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# Introduction (*Heading 1*)

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# Hardware Design

## Registers use the D flipflop design discussed in class, specifically using the controlled variant to only write when given the write signal. This results in each register needing 20 flipflops and a shared Write Enable signal, for a total of 21 input bits. Only the Q output bits are kept, so there are 20 output bits as well, with 20 discarded notQ bits.

## The control unit takes advantage of a number of multiplexers, demultiplexers, and decoders in order to correctly route data. Multiplexers are used for incoming data, like values taken from registers, while demultiplexers are used for outgoing data, like data sent to write to a register. A decoder is additionally needed to enable writing on the correct register.

# Instruction Set

Every instruction is a 20-bit word divided evenly into four sections: a 5-bit opcode, two 5-bit input addresses, and a 5-bit write address in that order. As is, this allows for more than the required number of unique opcodes for our three person group, as well as the ability to index through our entire 32-bit register array. Access to the 64-bit memory is not directly possible with this convention, and would rely on passing an address already stored in a register.

The following instructions are implemented at a high level at time of writing: no operation: NOP, the logical functions: NOT, AND, OR, XOR, mathematical functions: INC, DEC, ADD, SUB, and comparisons: EQ, GT, LT. A complete list of planned opcodes can be found in opCodes.txt.

The following an example programs one might write for this architecture (commas added for readability):

01000,00000,00000,00000

#NOT x0, x0, x0 / x0 = NOT(x0)

01000,00001,00000,00001

#NOT x1, x0, x1 / x1 = NOT(x1)

01100,00000,00000,00000

#SHFTR x0, x0, x0 / x0 = SHFTR(x0)

01101,00001,00000,00001

#SHFTL x1, x0, x1 / x1 = SHFTL(x1)

01001,00000,00001,00010

#AND x0, x1, x2 / x2 = AND(x0, x1)

10101,00001,00010,00011

#SUB x1, x2, x3 / x3 = x1 - x2

# Implimentation

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##### Conclusion

Of the many challenges we ran into with this project, a lot of them were related to the limitations brought about by using verilog, in addition to simply getting used to its syntax and conventions. One major example of this can be found in the mux/demux/encode/decode attempts made in ProgramFlow.v. The challenge here was differentiating the wires and identifying which was which. In conventional programming, this could be achieved by comparing a value to the iterator used in a for loop, but this is not the case for verilog’s generate blocks, which do not give you access to a genvar (its iterator) during runtime. In the mux implementation, we see that you can simply index the input based on the selector, but this is not possible when indexing the output in the demux circuit.

##### References

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