# OCHUKO ADIOTOMRE

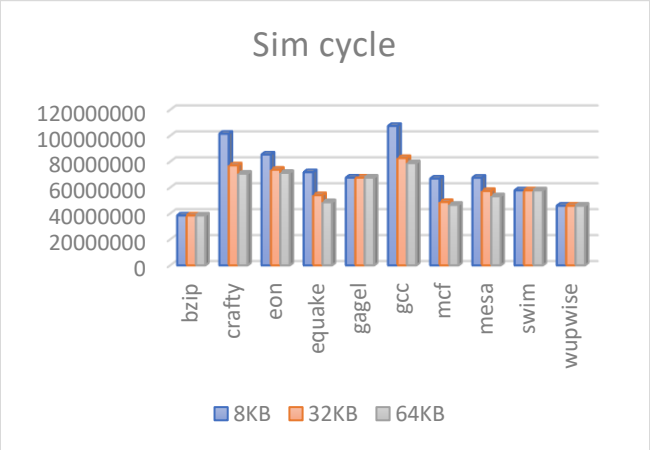
INTRODUCTION

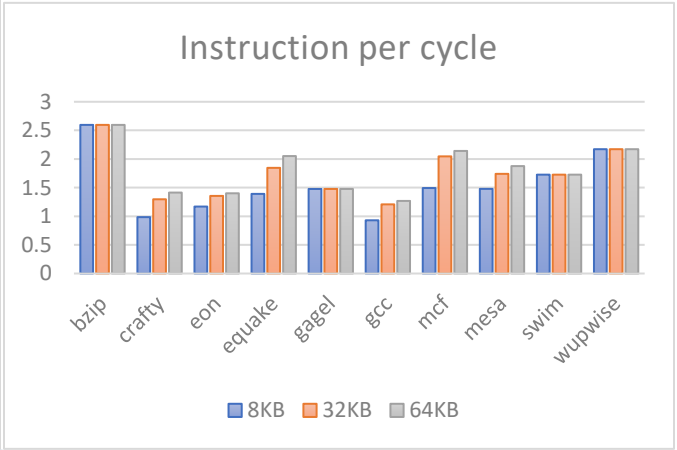
This project makes use of an open source tool called SimpleScalar. The SimpleScalar is used to simulate real program to obtain and analyze performance information of simulated architecture. The performance information being analyzed are the Miss Rate, Write Back, Instruction per Cycle, Loads executed, Stores Executed, Simulation time in cycles.

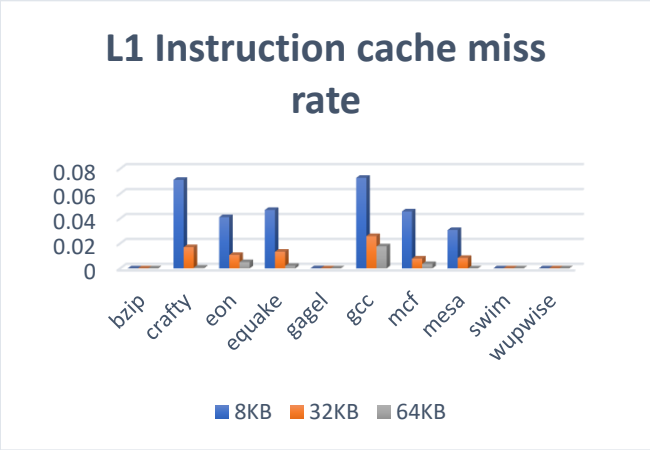
ANALYSIS

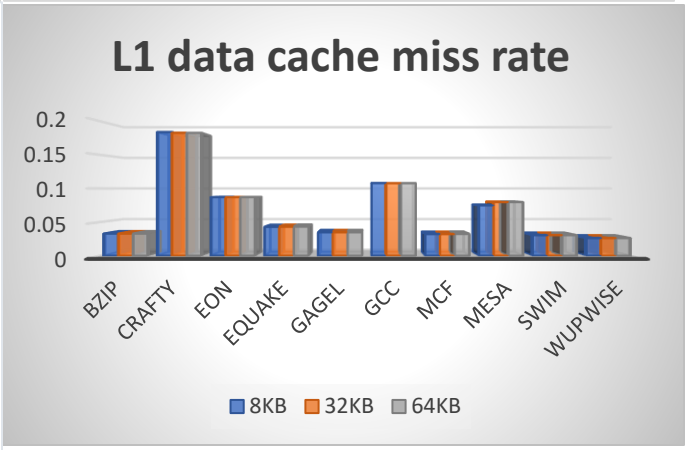
1. **Comparing 8KB, 32KB, 64KB instruction cache size. Since I had to make the block and associativity at the default size I had to just change the number of sets to achieve this.**

**The number of sets used is 256, 1024 and 2048 simultaneously for the 8KB, 32KB and 64KB.**



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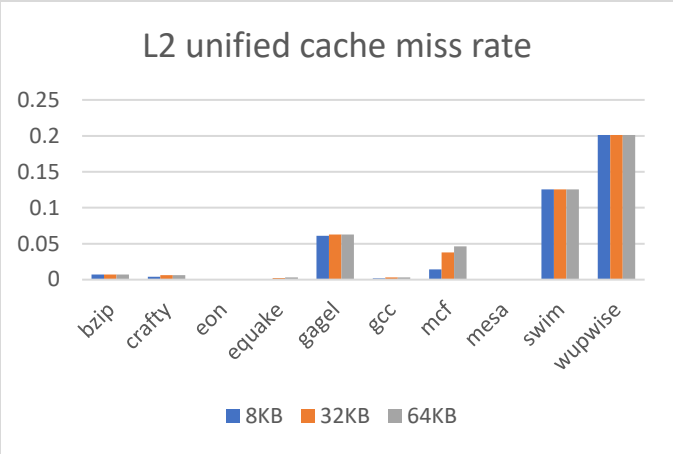
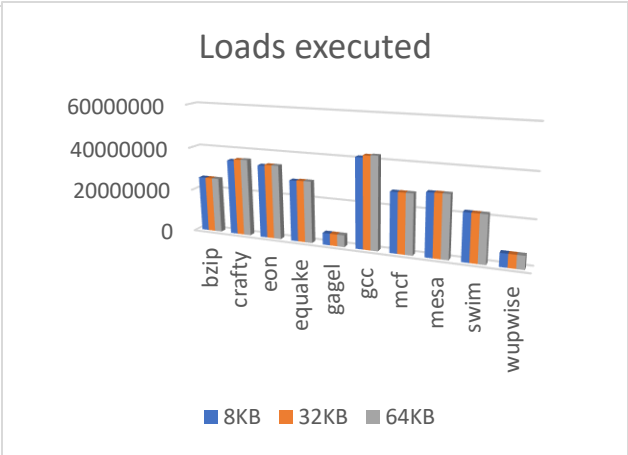
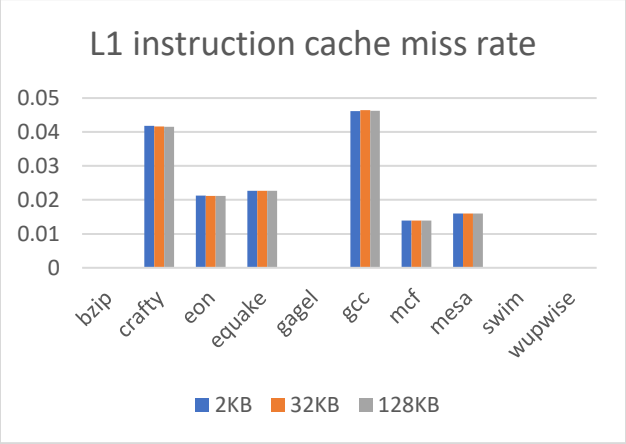


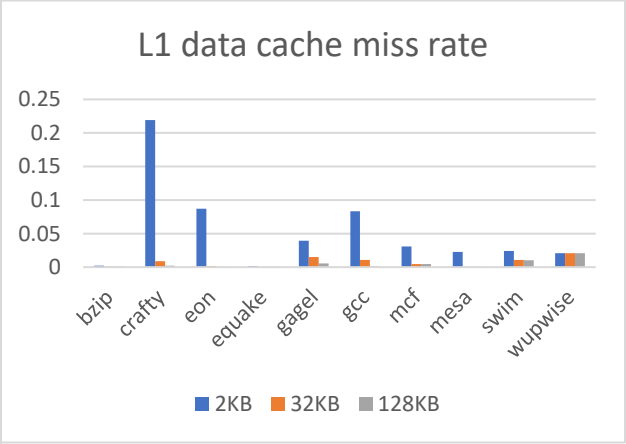




- As L1 instruction cache size increase total simulation time cycle increase
- As L1 instruction cache size increase instruction per cycle (IPC) increase
- As L1 instruction cache size increase, L1 instruction cache miss rate reduce
- As L1 instruction cache size increase, L1 data cache miss rate stays constant
- As L1 instruction cache size increase, L2 cache miss rate stays constant
- As L1 instruction cache size increase, loads executed increase by a negligible size

2. **Comparing 2KB, 32KB, 132KB L1 data cache size of all 4 way associativity. Since I had to make the block at the default size I had to just change the number of sets to achieve this.**

**The number of sets used is 16, 256 and 1024 simultaneously for the 2KB, 32KB and 132KB.**



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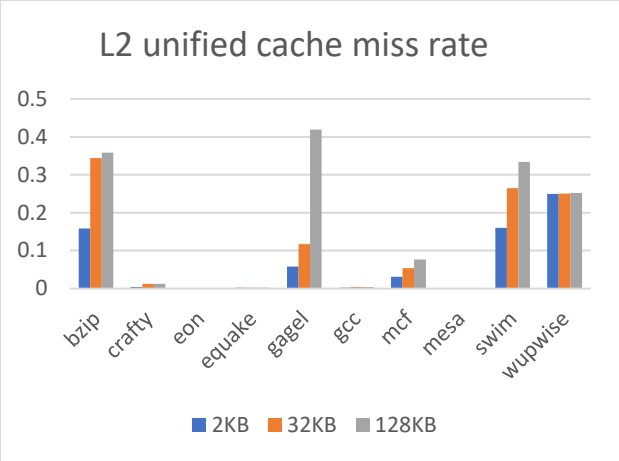


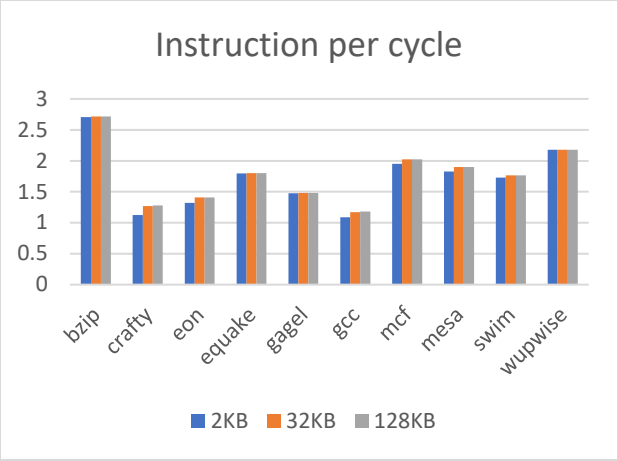


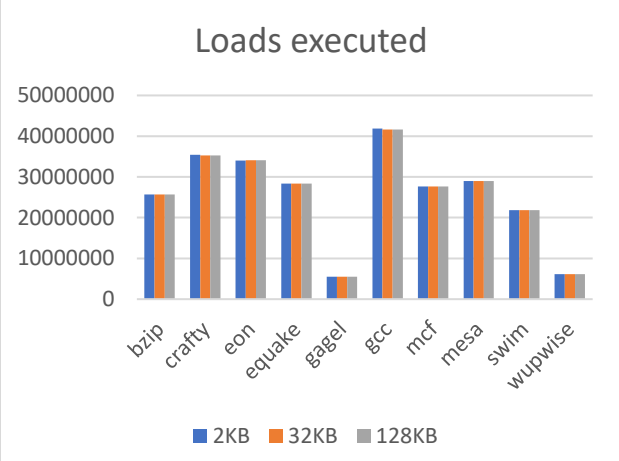


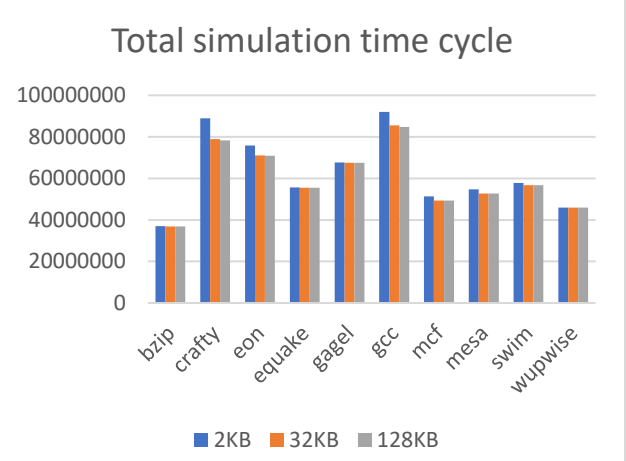


- As L1 data cache size increase, L1 instruction cache miss rate stays constant
- As L1 data cache size increase, L1 data cache miss rate reduce
- As L1 data cache size increase, L2 cache stays increase in few benchmarks
- As L1 data cache size increase, IPC increases negligibly
- As L1 data cache size increase, load executed stays constant
- As L1 data cache size increase, total simulation time cycle reduce

3. **Comparing 32KB L1 data cache size of all 1 way, 2 ways and 8 way associativity. Since I had to make the block the default size I had to just change the number of sets to achieve this. The number of sets was 1024, 512, 128 for 1 way, 2way and 8 ways respectively**

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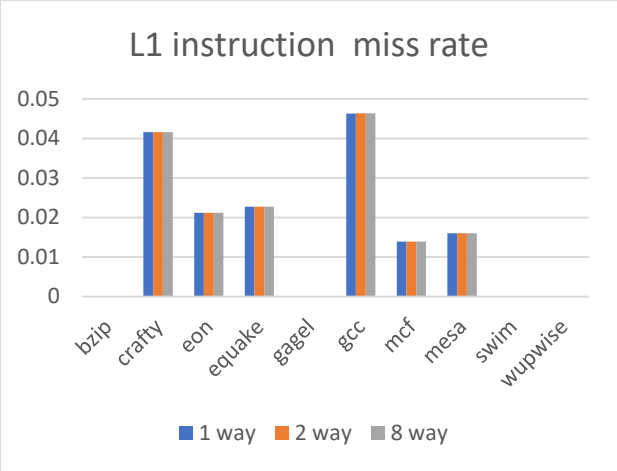


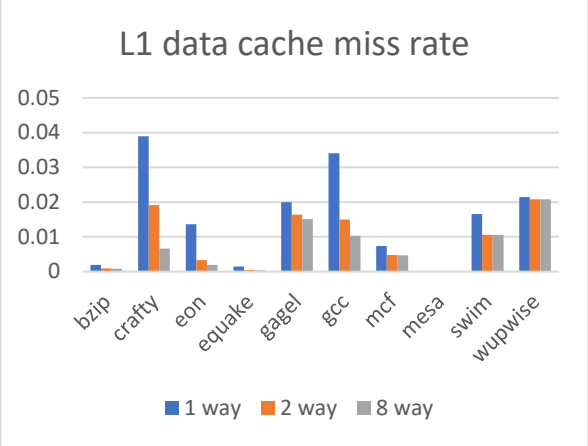


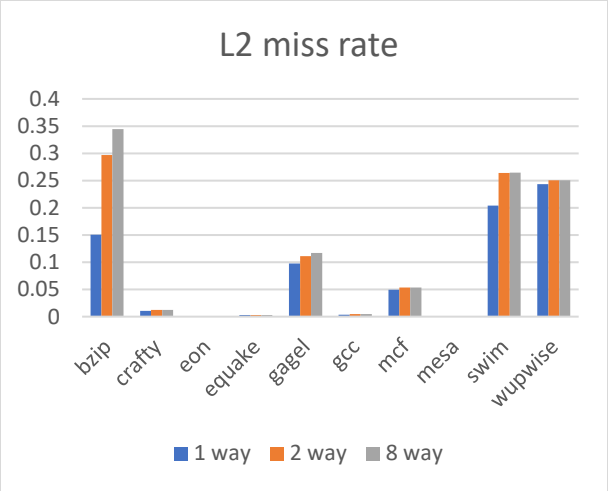


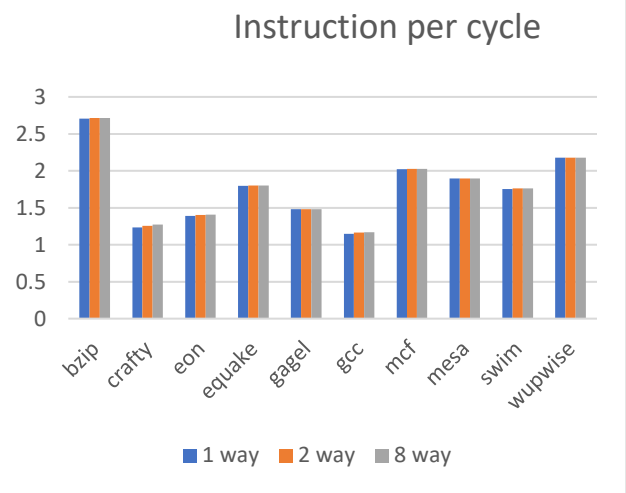


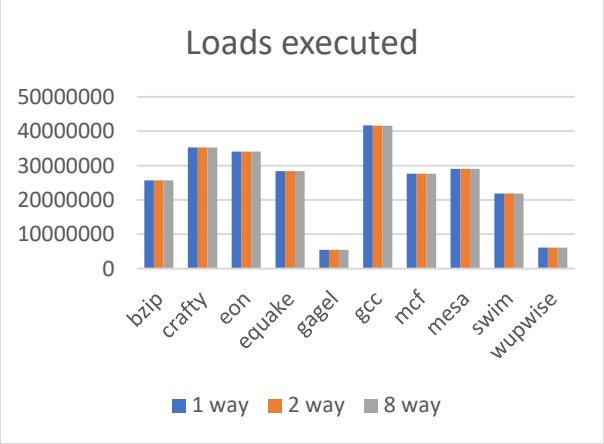


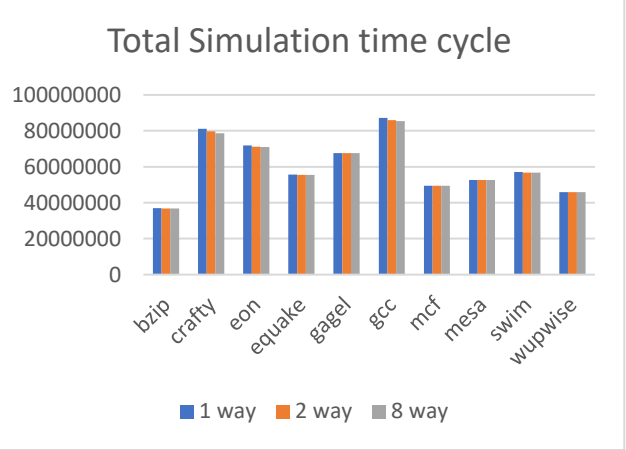


- As L1 data cache associativity increases, L1 instruction cache miss rate stays constant
- As L1 data cache associativity increases, L1 data cache miss rate stays reduce
- As L1 data cache associativity increases, L2 miss rate increases
- As L1 data cache associativity increases, instruction per cycle stays constant
- As L1 data cache associativity increases, Loads executed remains constant
- As L1 data cache associativity increases, total simulation time cycle reduces insignificantly

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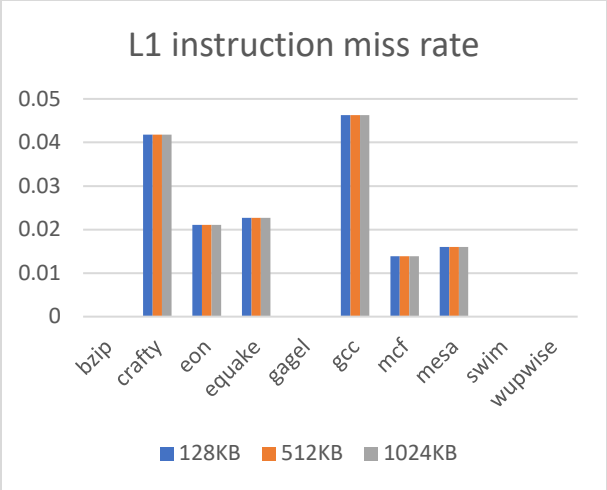
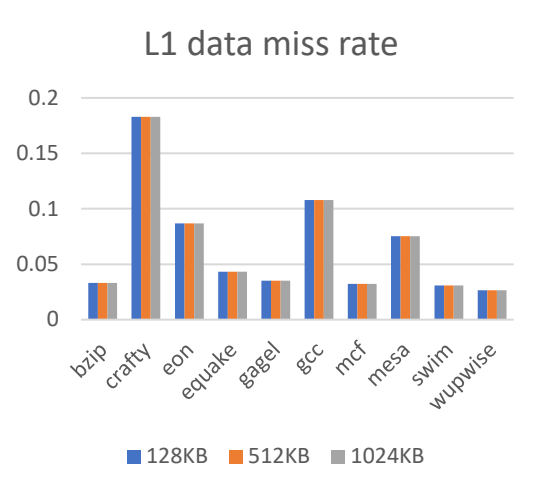
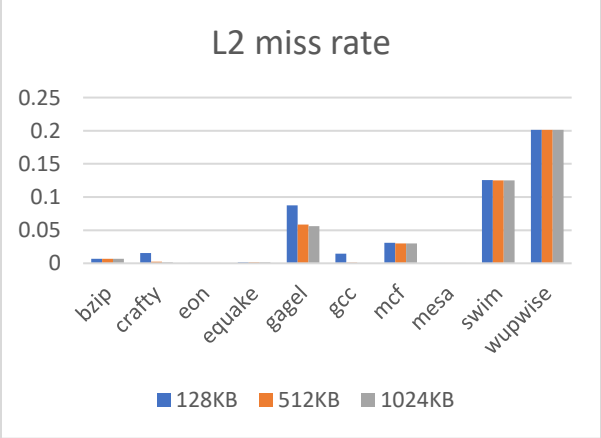
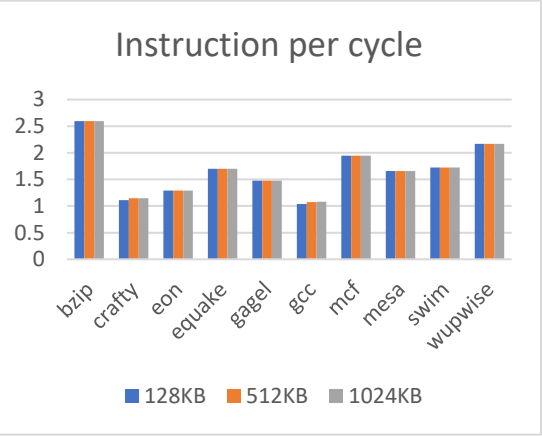
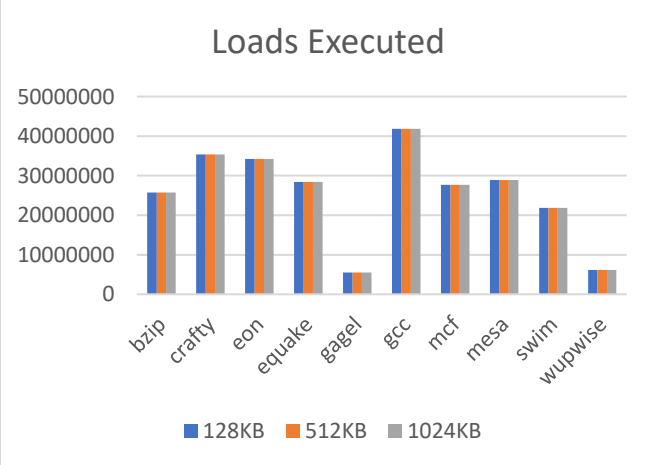
4. **Comparing 128KB, 512KB, 1024KB L2 unified cache size. Since I had to make the block and associativity the default size I had to just change the number of sets to achieve this. The number of sets was 512, 2048, 4096 for 128KB, 512KB and 1024KB respectively**

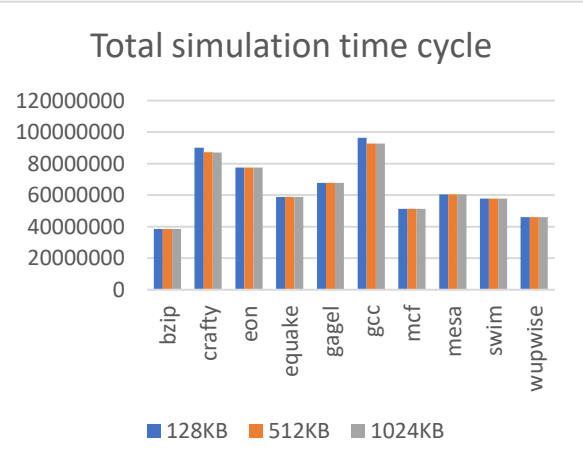



- As L2 data cache size increases, L1 instruction miss rate stays constant
- As L2 data cache size increases, L1 data miss rate stays constant

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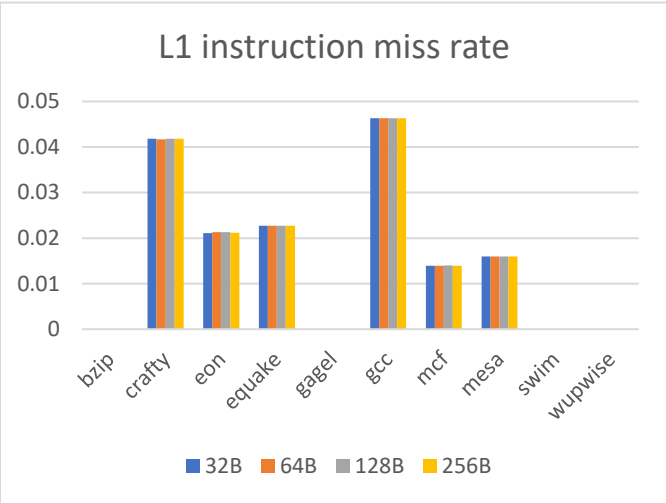
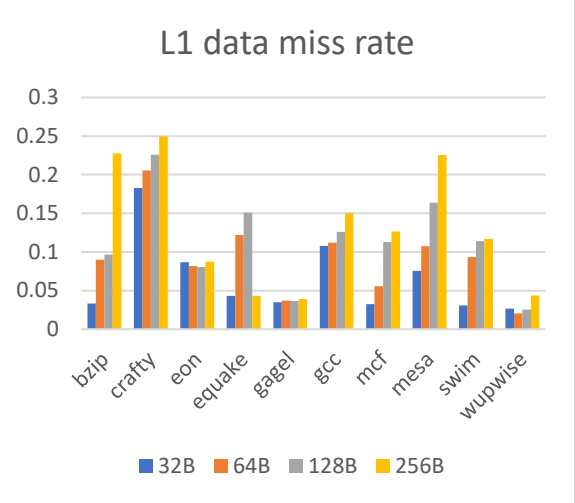
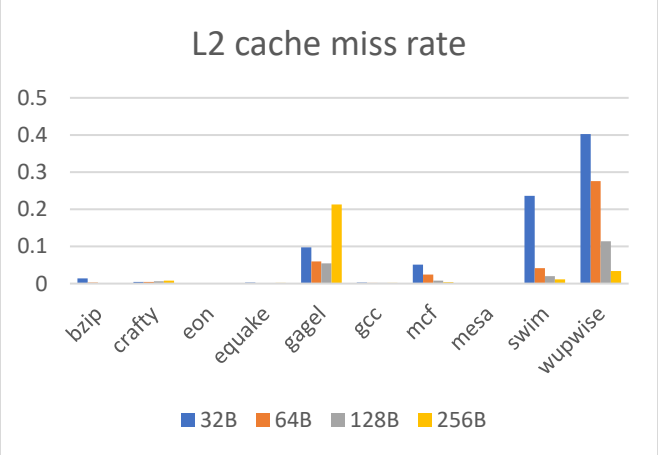
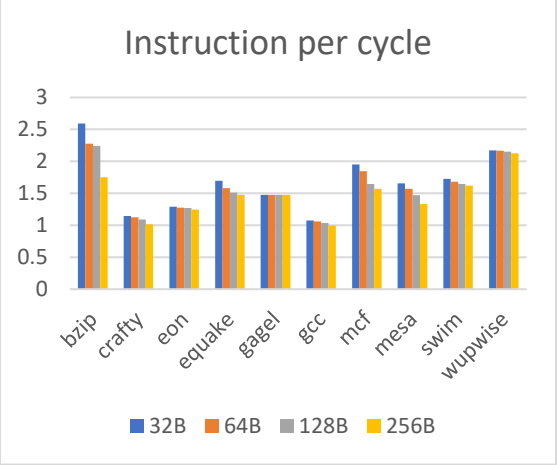
- As L2 data cache size increases, L2 miss rate decreases slightly
- As L2 data cache size increases, instruction per cycle
- As L2 data cache size increases, load executed remain constant
- As L2 data cache size increases, total simulation time cycle increases by a little

5. **Comparing default cache size of L1 data cache and L2 unified cache, having block size of 32B, 64B, 128B and 256B. Since I had to make the associativity the default size I had to just change the number of sets of both L1 data cache and L2 cache.**
   **To achieve this, For 32B the number of sets was 128 for L1 and 2048 for L2, for 64B the number of sets was 64 for L1 and 1024, for 128B the number of sets was 32 for L1 and 512 for L2, for 256B the number of sets was 16 for L1 and 256 for L2.**



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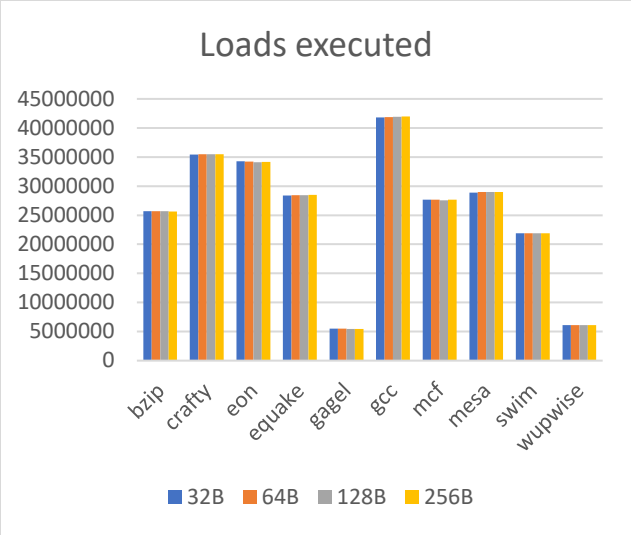
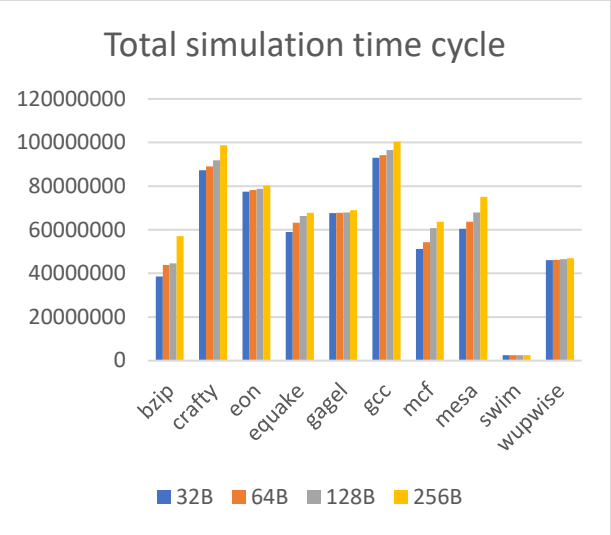
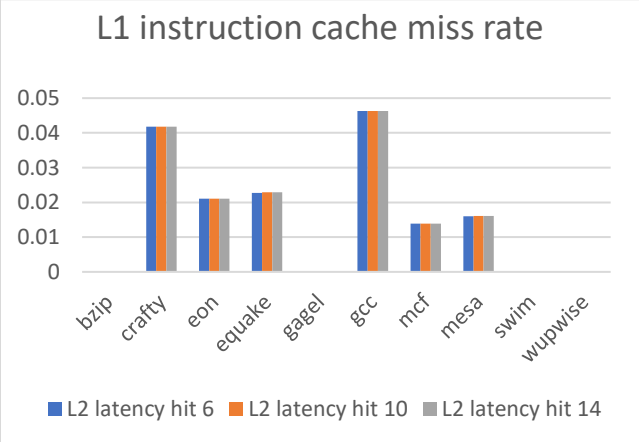
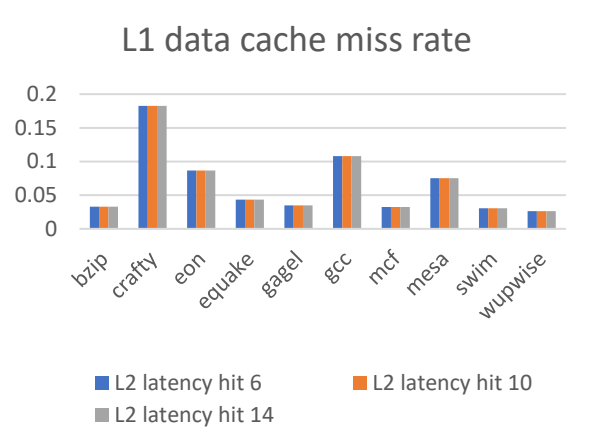


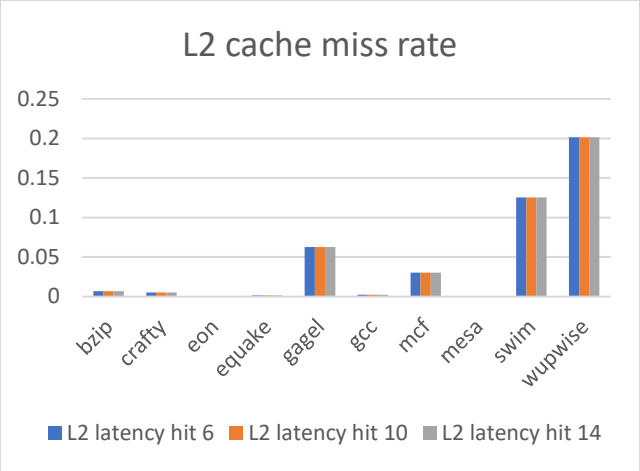



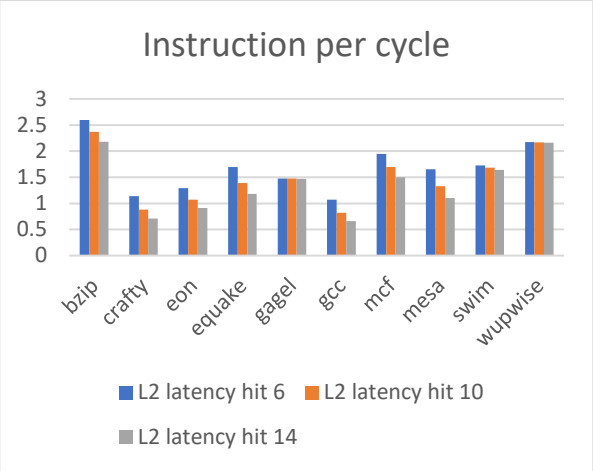

- As block size increase, L1 instruction miss rate stays constant
- As block size increase, L1 data miss rate increases
- As block size increase, L2 miss rate reduces
- As block size increase, instruction per cycle reduce
- As block size increase, loads executed remains constant
- As block size increase, total simulation time cycle increases

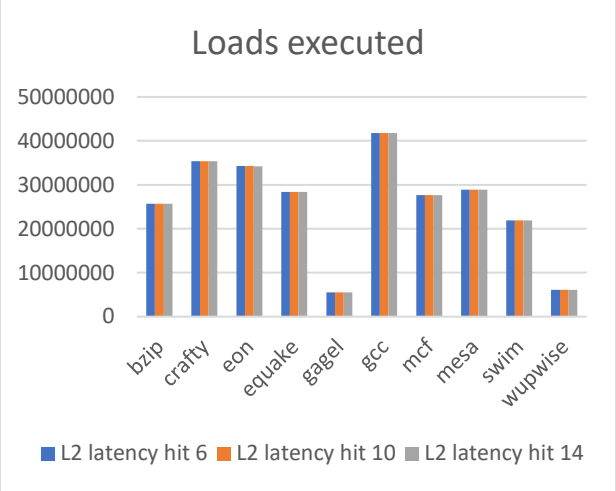
6. **Comparing default cache size, block, set and associativity with different L2 latency hit time of 6, 10 and 14.**

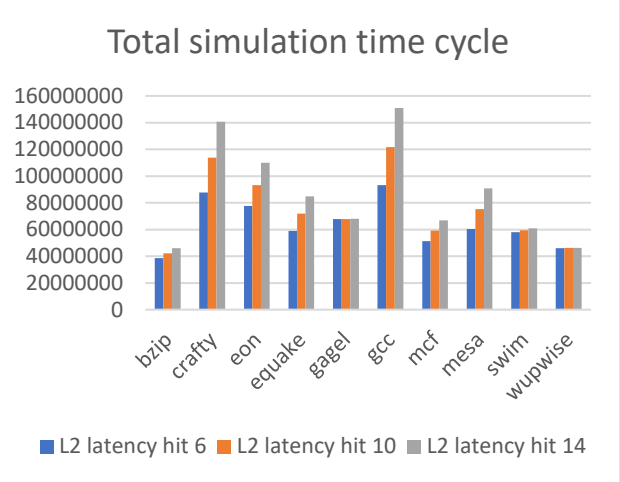





- As L2 latency hit increases, L1 instruction cache miss rate remains constant
- As L2 latency hit increases, L1 data cache miss rate remains constant
- As L2 latency hit increases, L2 cache miss rate remains constant
- As L2 latency hit increases, instruction per cycle reduces
- As L2 latency hit increases, loads executed is constant
- As L2 latency hit increases, total simulation time cycle increases

7. **Comparing default cache size, block, set and associativity with different L1 latency hit time of 1, 2 and 4.**

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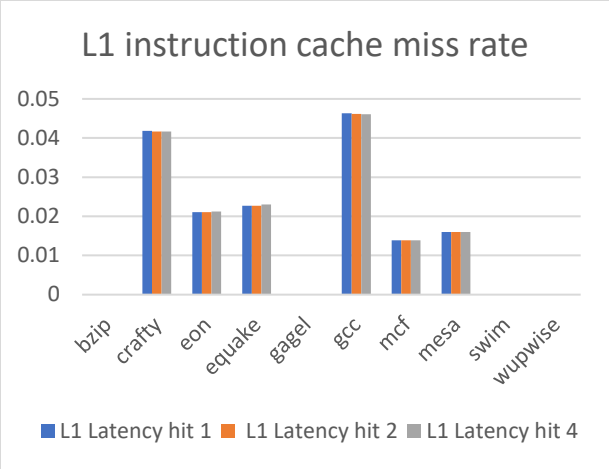


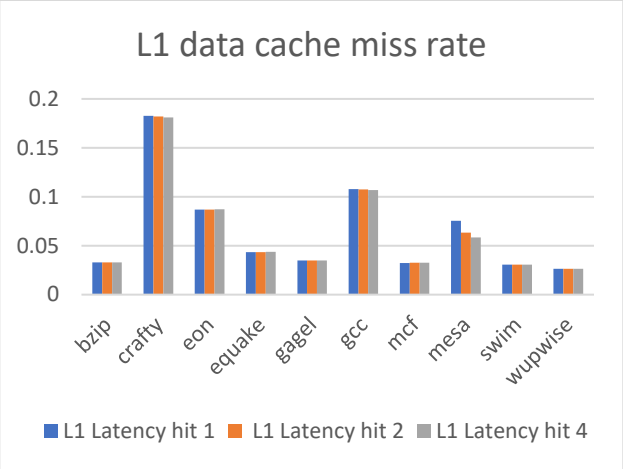


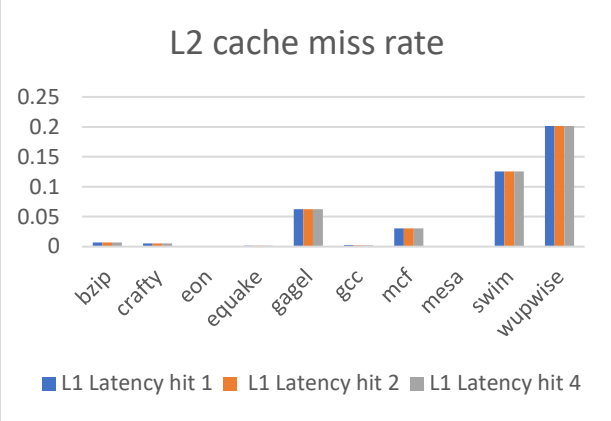


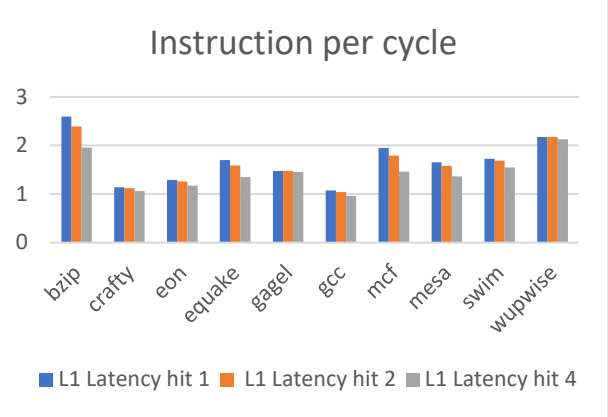


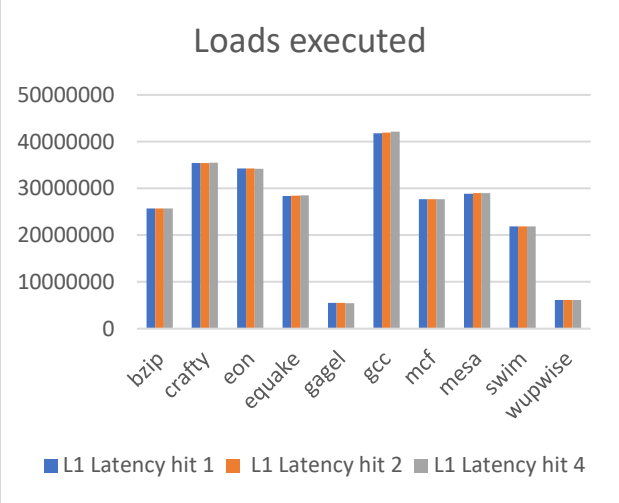


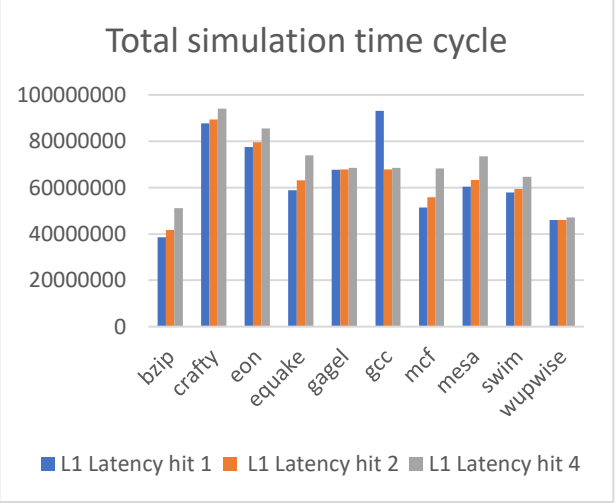


- As L1 latency hit increases, L1 instruction cache miss rate remains constant
- As L1 latency hit increases, L1 data cache miss rate remains constant
- As L1 latency hit increases, L2 miss rate remains constant
- As L1 latency hit increases, instruction per cycle reduces
- As L1 latency hit increases, loads executed remains constant
- As L1 latency hit increases, total simulation time cycle