AsciiDoctor demo for HDL designers

v1.0

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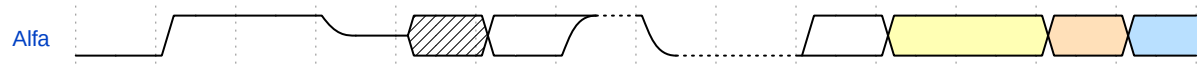
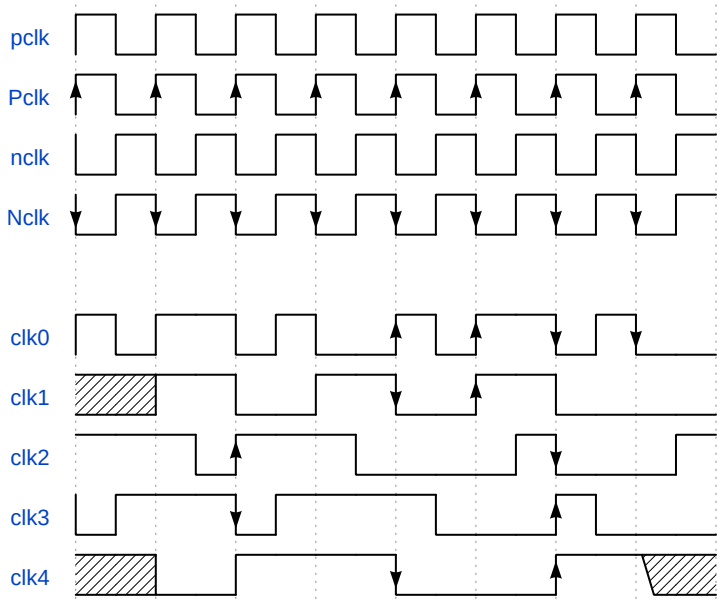
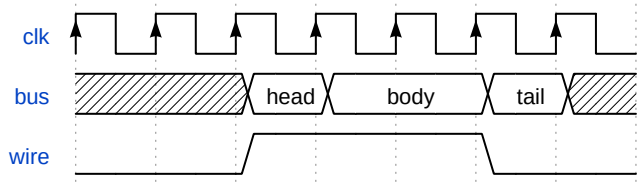
1.1. Test #0



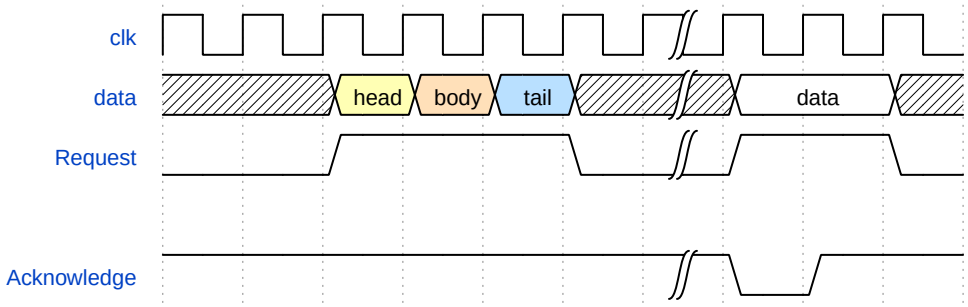
1.2. Test #1



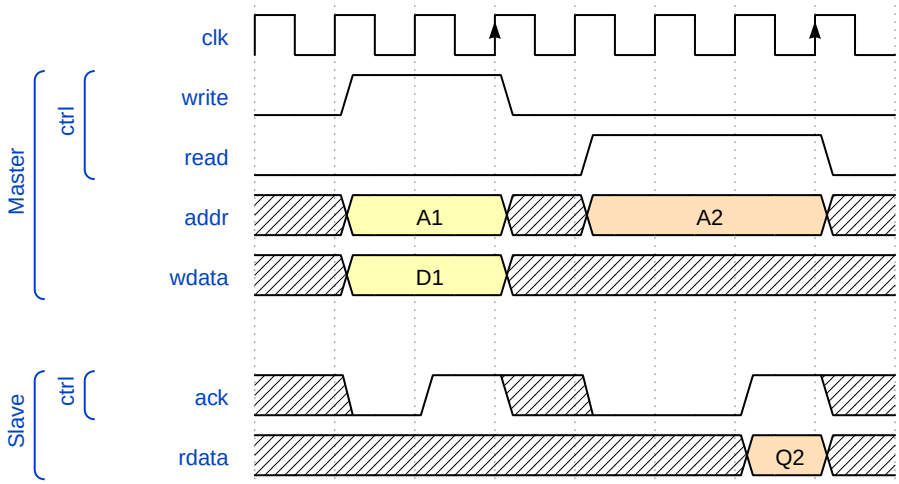
1.3. Test #2



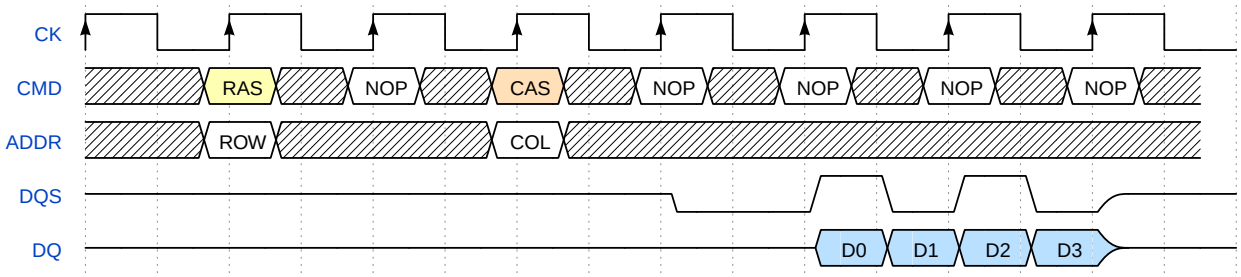
1.4. Test #3



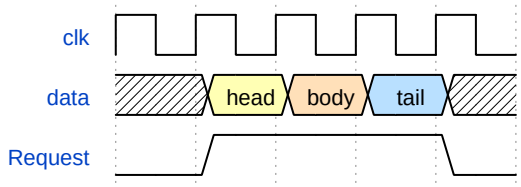
1.5. Test #4



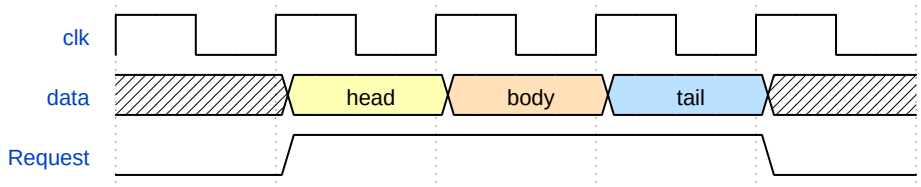
1.6. Test #5



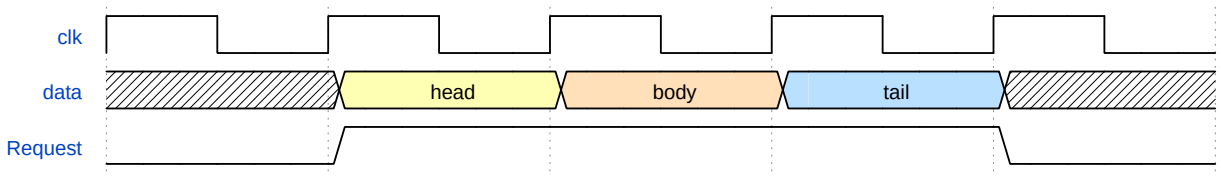
1.7. Test #6



1.8. Test #7

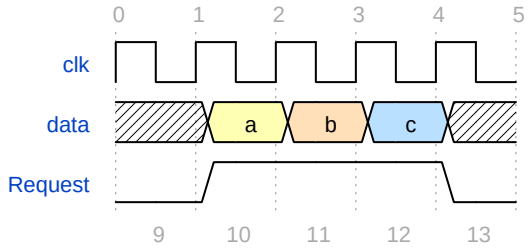


1.9. Test #8



1.10. Test #9

WaveDrom example



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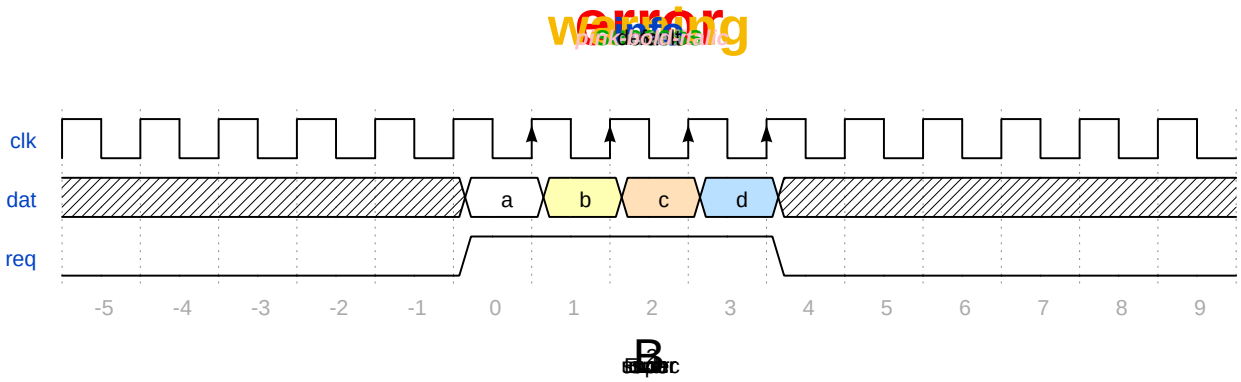
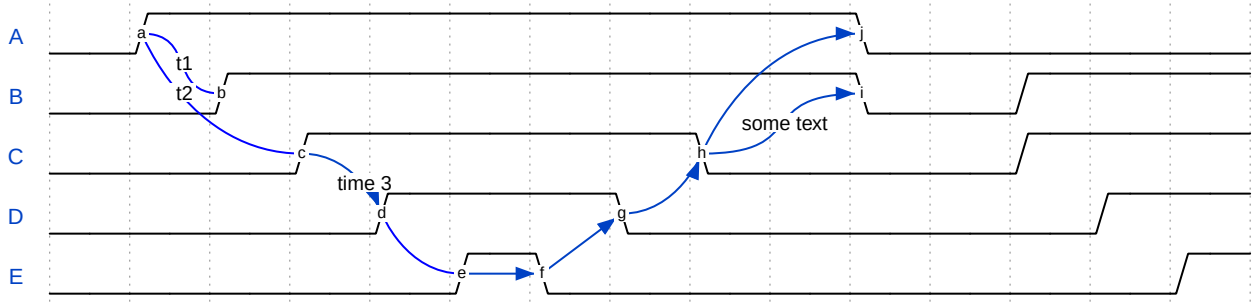
1.11. Test #10



1.12. Test #11



Chapter 2. Port description example

Signal name	Type	Description
clk	in	Clk input
reset	in	Reset
address	in	Address bus
read	in	Read signal
readdata	out	Read data bus
readvalid	out	Read valid signal
write	in	Write signal
writedata	in	Write data bus

Chapter 3. Register description example

Address	Bits	Field Name	Access	Description
0x00000000	31:24	NU	RO	Not used.
	23:16	VMAJ	RO	Version major.
	15:8	VMIN	RO	Version minor.
	7:0	VPATCH	RO	Version patch.
0x00000004	31:16	STATUS	RO	Status bits.
	15	PLL_LOCKED	RO	PLL locked.
	14	DDR_INIT_DONE	RO	DDR Init_done.
	13:12	NU	RO	Not used.
	11:8	GROUP_0_INTR	R/W	Group #0 interrupt requests.
	7:4	GROUP_1_INTR	R/W	Group #1 interrupt requests.
	3:0	GROUP_2_INTR	R/W	Group #2 interrupt requests.

Chapter 4. VHDL syntax coloring example

```
proc_column_counter : process ( reset, clk )
  begin
    if reset = '1' then
      col <= 0;
    elsif rising_edge( clk ) then
      if enable then
        if sink_endofpacket = '1' then
          col <= 0;
        elsif col = g_width - g_data_size / c_pixel_size then
          col <= 0;
        else
          col <= col + g_data_size / c_pixel_size;
        end if;
      end if;
    end if;
  end process proc_column_counter;
```