



# Altium Designer

## Essentials Training with Altium 365

### Module 13: Schematic Electrical Rules Validation

**Altium**  
TRAINING





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# Module 13: Schematic Electrical Rules Validation

## 1 Purpose

In this exercise, you will learn how to validate a PCB Project and learn how to review and resolve any reported messages after validating, such as warnings and errors.

Validation is an important step that should not be overlooked. Validating builds a netlist for each schematic sheet, creates sheet-to-sheet connectivity and builds the Unified Data Model. Validating the project analyzes the complete design to check for drafting and electrical errors.

## 2 Shortcuts


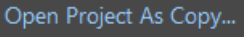

Shortcuts used when working with Module 13: Schematic Electrical Rules Validation

C » O	Project Options
C » C	Validate PCB Project





## 3 Preparation

1. Close all existing projects and documents.
2. Next, create a Copy / Clone of the Training Project Module Project Module 13 Schematic Electrical Rules Validation.
3. Select **File » Open Project...** to open the *Open Project* dialog.
4. Enable the folder view button .
5. Navigate to the predefined Training Project Module 13 Schematic Electrical Rules Validation (Top\Projects\Altium Designer Essentials Training Course\...).
6. Select **Open Project as Copy...** .
7. At the new dialog, *Create Project Copy*:
  - a) Add your name to the project: to Module 13 Schematic Electrical Rules Validation - [Your Name].
  - b) Add a description: Altium Essential Training - Module 13 - [Your Name].
  - c) Open the *Advanced* section.
  - d) Select the Ellipsis Button  from the **Folder** configuration to open the *Choose Folder* Dialog.
    - i) Select the folder with your name: Project\For Attendees\[Your Name]
    - ii) Select **OK**.
  - e) Change the Local Storage path if needed.
  - f) Select **OK** to create the copy.
8. Wait until Altium Designer creates the copy of the project and opens the project in the *Projects* panel; this can take up to 1 minute.

Hint: For details how to Copy / Clone the predefined training project see Module 9 Making the Connection, Step 3 Preparation.





## 4 Project Options

Before validating the project, you should first check the *Error Reporting* settings to be sure they are defined properly for what you are designing.

### 4.1 Error Reporting Tab

9. Right-click the *Module 13 Schematic Electrical Rules Validation* project from the *Projects* panel, and select **Project Options...**, **C » O**.
10. Click on the *Error Reporting* tab as shown in Figure 1.

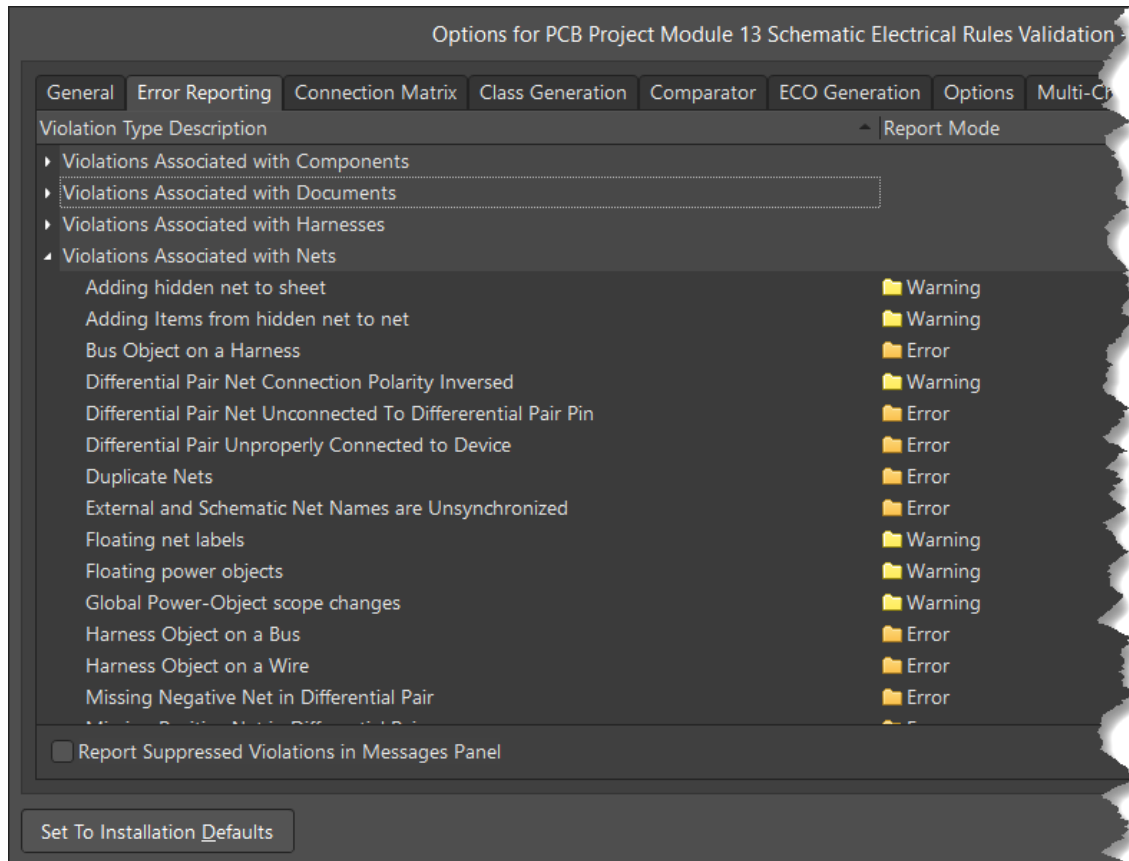


Figure 1. Project Options Error Reporting Tab

11. Scroll down to view the different categories of violation checks that the validation performs. Error reporting for these violations can be changed at any time from the *Report Mode* column and will only apply to the specific project.





## 4.2 Connection Matrix Tab

12. Select the **Connection Matrix** tab. You can set the reporting mode for connections between different pins, ports and sheet entry types as shown in Figure 2.
13. Set all Unconnected options to Warning as shown in Figure 2.

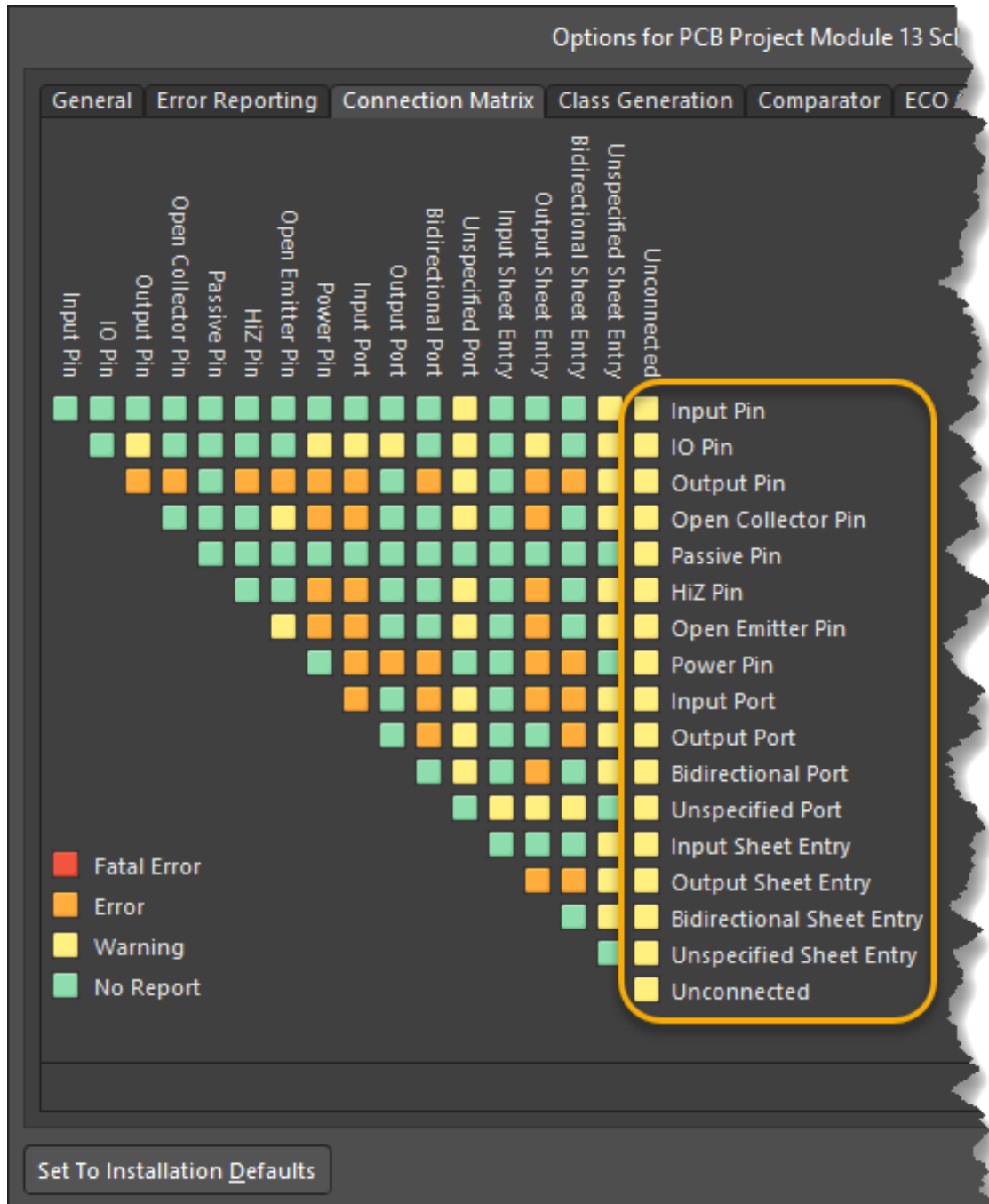


Figure 2. Connection Matrix Tab

Hint: A common setting that is used for the default ERC matrix setting, is to set the Unconnected information to Warning instead of No Report to report all open Pins, Ports, and Sheet Entries.

14. Click **OK** to save and close Project Options.





## 4.3 Preferences - Navigation

16. Go to Preferences » System » Navigation.

17. In the *Highlight Methods* section, set the **Far-Close** slider to mid-range as shown in Figure 3.

18. Click **OK** to save and close *Preferences*.

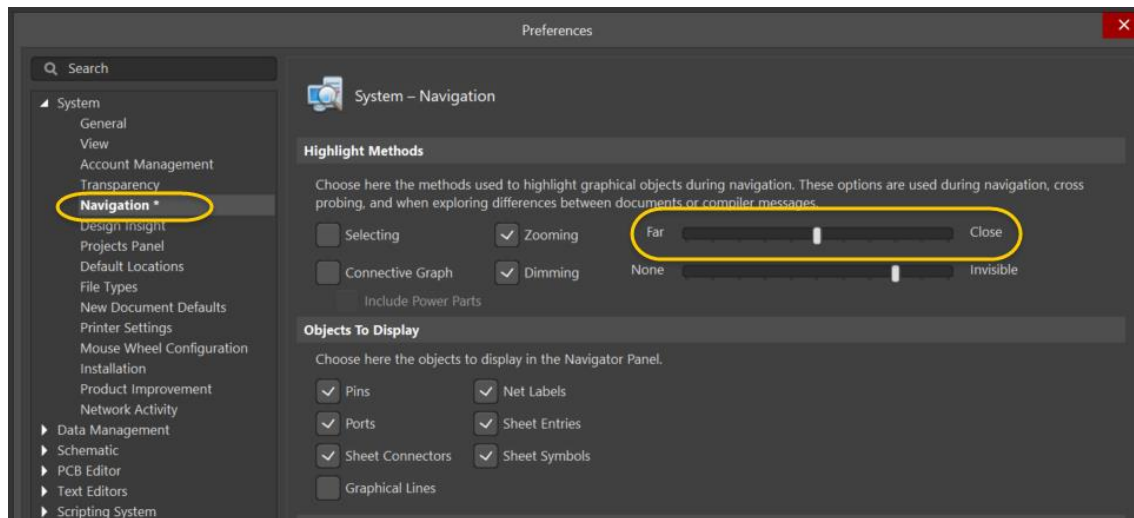


Figure 3. Highlight Preference







## 5 Validating the Project

19. Validate the `WCTopping` design by going to **Project » Validate PCB Project [Project Name]** or by right-clicking on the project in the *Projects* panel and selecting **Validate PCB Project [Project Name]**.
20. After you validate the design, the *Messages* panel will appear. If it does not, the project has either passed the Electrical Rules Check (ERC), or there are only *Warnings* and no *Errors* or *Fatal Errors*.

Hint: If you cannot find the *Messages* Panel, click on the **Panels** button  in the bottom right corner of Altium Designer and select **Messages** from the popup menu.

### 5.1 Correcting Errors and Warnings

21. Upon validation, you should see many Errors and Warnings in the *Messages Panel*. Double-clicking any warning or error message in the *Messages Panel* will navigate to the location where the warning or error occurs. It will display the affected elements in the *Details* section of the *Messages* panel.
22. If not already done, sort the listings in the *Messages* panel to group the *Warnings*, *Fatal Errors* and *Errors* by clicking the **Class** column header until the *Fatal Error* are brought to the top of the list as shown in Figure 4. Feel free to enlarge the *Messages* panel to see all of the details.
23. You should see 3 “Net GPIOXX has only one pin” Errors in the *Messages* panel as shown in Figure 4 below.
24. Double-clicking on each of these 3 errors (“Net <GPIO##> has only one pin”) will highlight the affected pins associated to that error. In this case, it’s Pin 11, Pin 13 and Pin 15 of component `J1`.

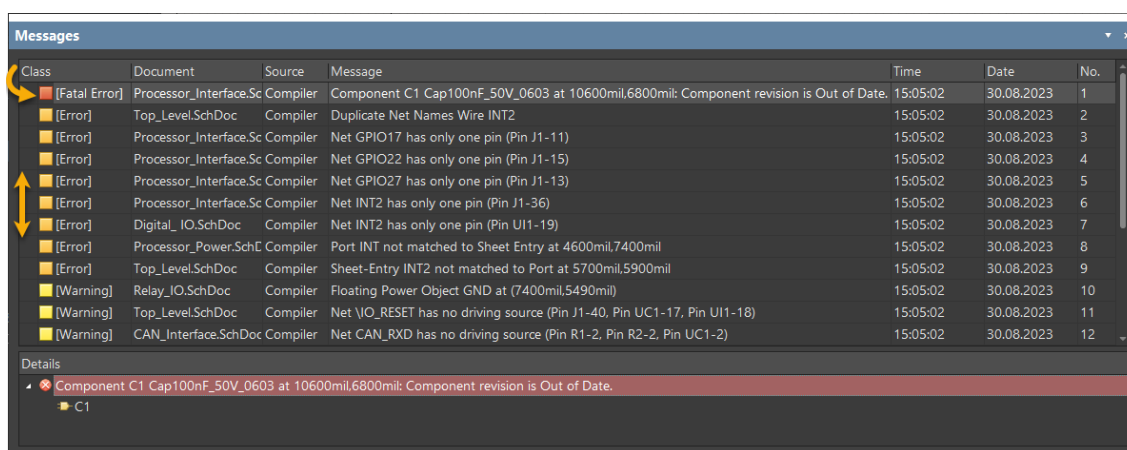


Figure 4. Net <name> only has one Pin error in the Messages panel

### 5.2 Fatal Error - Revision Out of date

25. Double click the Fatal Error message, Figure 4.
  - a) Altium opens the page `Processor_Interface.SchDoc`.
  - b) Altium will jump and show the capacitor `C1`.



26. Select C1 and check the status information at the *Properties* panel, the component status shows it is *Out of date* and does not match the component in the library, Figure 5.

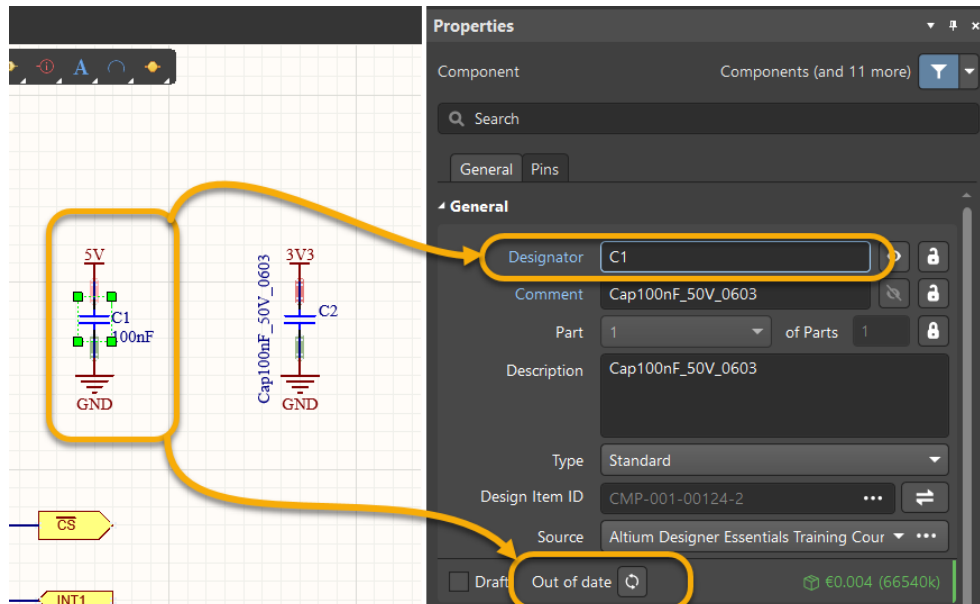



Figure 5. Component is Out of Date

27. To update the component to the latest revision, and to fix the ERC error, select the refresh button .
28. Refreshing the component will pull the latest revision from the database and update the component, Figure 6.

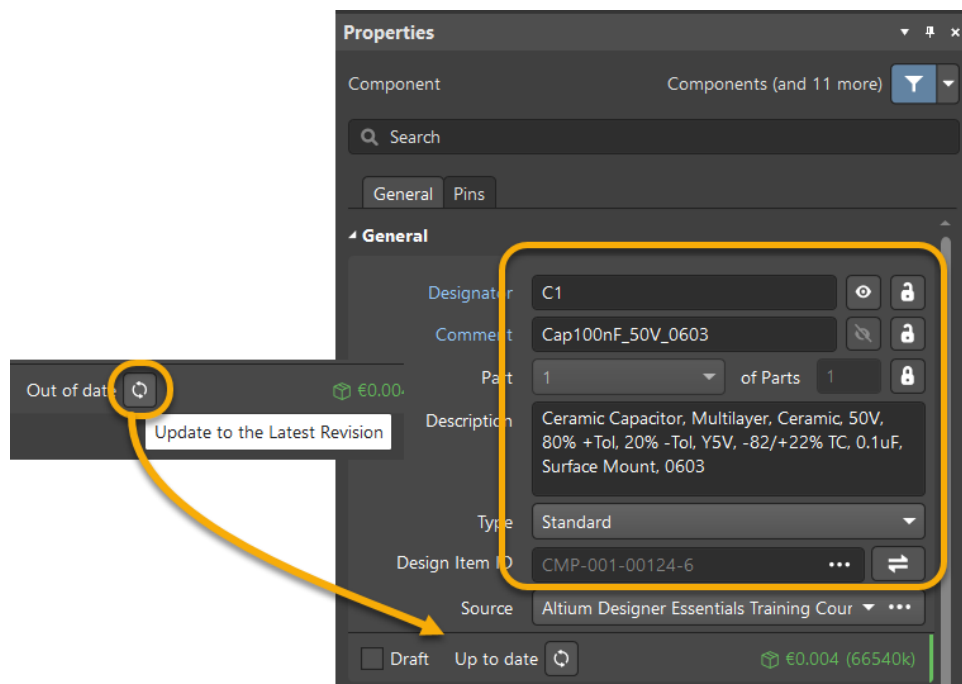


Figure 6. Now Component is Up to Date

Hint: To check the revision status of the components it is not necessary to run the validation. With the command **Tools » Item Manager** you can open the *Item Manager*. The *Item Manager* allows you to see all components, the revision status of all components and you can update and replace components within the *Item Manager*.



### 5.3 Error - Net has Only one Pin

29. Double-click on the message *Net GPIO17 has only one pin (Pin J1-11)* to jump to the error. You see a wire that is connected just to one pin.
30. Right-click on the error in the Messages panel called *Net GPIO17 has only one pin (Pin J1-11)*.
31. For suppressing warning and errors, we will assign a **Specific No ERC directive** as follows:
  - a) Right-click on the error in the Messages panel called *Net GPIO17 has only one pin (Pin J1-11)*
  - b) Select **Place Specific No ERC for this Violation...** from the menu as shown in Figure 7

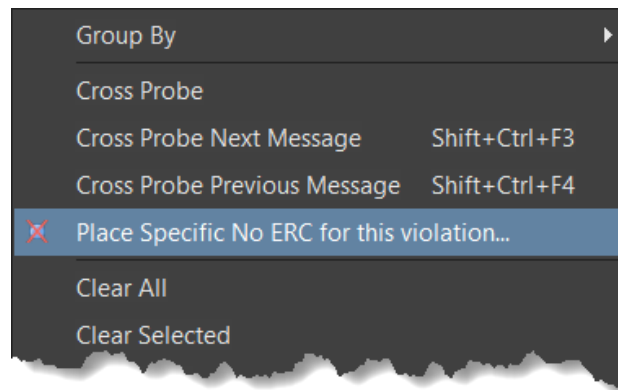


Figure 7. Place No ERC Directive directly from the Messages panel

- c) The appropriate schematic will open, and the **Specific No ERC** directive will be on your cursor. Place the directive at the end of the wire for that pin (*GPIO17*).
- d) Continue to place **Specific No ERC directives** to the 2nd & 3rd errors as shown in Figure 8 below.

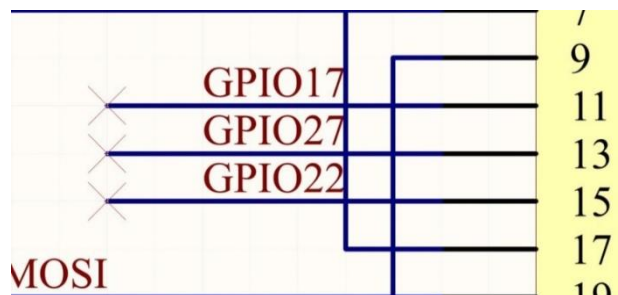


Figure 8. Placed No ERC directives

32. Validate the project again by going to **Project » Validate PCB Project WCTopping.PrjPcb**.
33. Verify the list of messages no longer reports the "Net <GPIO##> has only one pin (Pin J1-##)" errors. You'll notice that there are still other Errors and Warnings that need to be addressed.

Note: Placing a "Specific No ERC" will mask the Error or Warning associated with that object. This directive should only be used if you want to purposely disregard that Error or Warning (for example, pin not connected or being used). It is best practice to resolve the Warning or Error correctly, instead of placing a "Specific No ERC" directive. Be cautious when using them.



## 5.4 Error - Port INT not matched to Sheet Entry / Sheet-Entry INT2 not matched to Port

There are many related errors, this is a consequence of a Port name not matching a Sheet Entry in the *Processor\_Power.SchDoc*. The main reason for these errors is due to a break or discontinuity in the connection of net INT2.

Class	Document	Source	Message
[Error]	Digital_IO.SchDoc	Compiler	Net INT2 has only one pin (Pin U11-19)
[Error]	Processor_Interface.SchDoc	Compiler	Net GPIO17 has only one pin (Pin J1-11)
[Error]	Processor_Interface.SchDoc	Compiler	Net GPIO22 has only one pin (Pin J1-15)
[Error]	Processor_Interface.SchDoc	Compiler	Net GPIO27 has only one pin (Pin J1-13)
[Error]	Processor_Interface.SchDoc	Compiler	Net INT2 has only one pin (Pin J1-36)
[Error]	Processor_Power.SchDoc	Compiler	Port INT not matched to Sheet Entry at 4600mil,7400mil
[Error]	Top_Level.SchDoc	Compiler	Duplicate Net Names Wire INT2
[Error]	Top_Level.SchDoc	Compiler	Sheet-Entry INT2 not matched to Port at 5700mil,5900mil
[Warning]	CAN_Interface.SchDoc	Compiler	Net CAN_RXD has no driving source (Pin R1-2, Pin R2-2, Pin UC1-2)
[Warning]	CAN_Interface.SchDoc	Compiler	Net NetRCAN1_2 has no driving source (Pin RCAN1-2, Pin UC2-8)
[Warning]	CAN_Interface.SchDoc	Compiler	Net OSC1 has no driving source (Pin CO1-2, Pin UC1-8, Pin X1-1)
[Warning]	Relay_IO.SchDoc	Compiler	Floating Power Object GND at (7400mil,5490mil)
[Warning]	Relay_IO.SchDoc	Compiler	Unconnected Pin U1-12 at 7400mil,5600mil
[Warning]	Relay_IO.SchDoc	Compiler	Unconnected Pin U1-8 at 7400mil,5500mil
[Warning]	Top_Level.SchDoc	Compiler	Net IOexpand_CS has no driving source (Pin J1-7, Pin UC1-16, Pin UI1-11)
[Warning]	Top_Level.SchDoc	Compiler	Net RELAY1 has no driving source (Pin J1-29, Pin U1-3)
[Warning]	Top_Level.SchDoc	Compiler	Net RELAY2 has no driving source (Pin J1-31, Pin U1-6)
[Warning]	Top_Level.SchDoc	Compiler	Net SPI_MOSI has no driving source (Pin J1-19, Pin UC1-14)
[Warning]	Top_Level.SchDoc	Compiler	Net SPI_SCLK has no driving source (Pin J1-23, Pin UC1-13, Pin UI1-12)
[Warning]	Top_Level.SchDoc	Compiler	Net VO_RESET has no driving source (Pin J1-40, Pin UC1-17, Pin UI1-18)

Figure 9. Port Related Errors

34. In the messages panel double-click on the message Port INT not matched to Sheet Entry, to jump to the schematic with the violation, as highlighted in Figure 10.

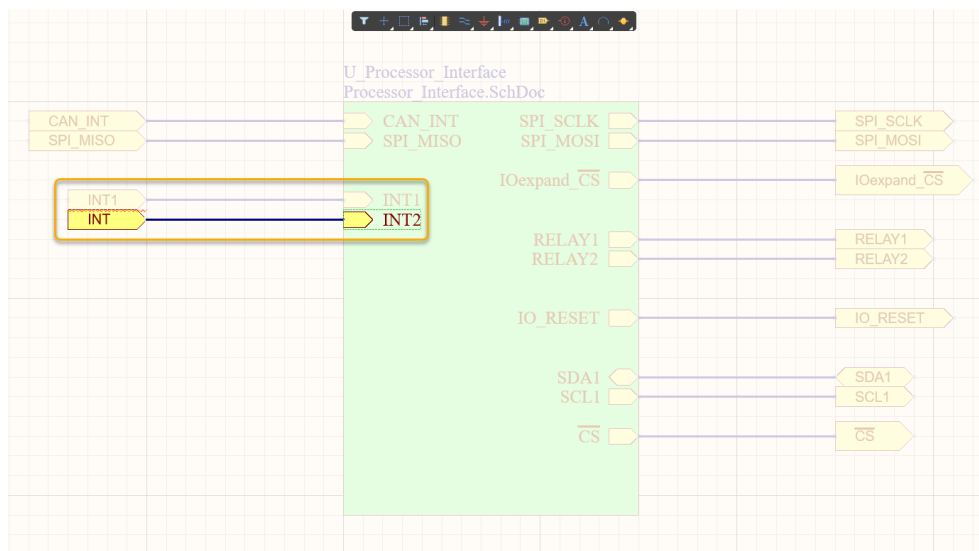


Figure 10. Port INT not matched to Sheet Entry

35. Change the Port from INT to INT2.

36. Validate the project again.

Following the validation process, all the errors associated with unmatched ports have been successfully resolved.

Hint: It is possible to check Port and Sheet Entry synchronization by running the command: **Design » Synchronize Sheet Entries and Ports.**

## 5.5 Warnings - No driving source

37. The next group of errors for Net <Net ##> has no driving source occurs when an input of an IC is connected to a passive component, as shown in Figure 11 below. (Net NetRCAN1\_2 has no driving source (Pin RCAN1-2, Pin UC2-8)).

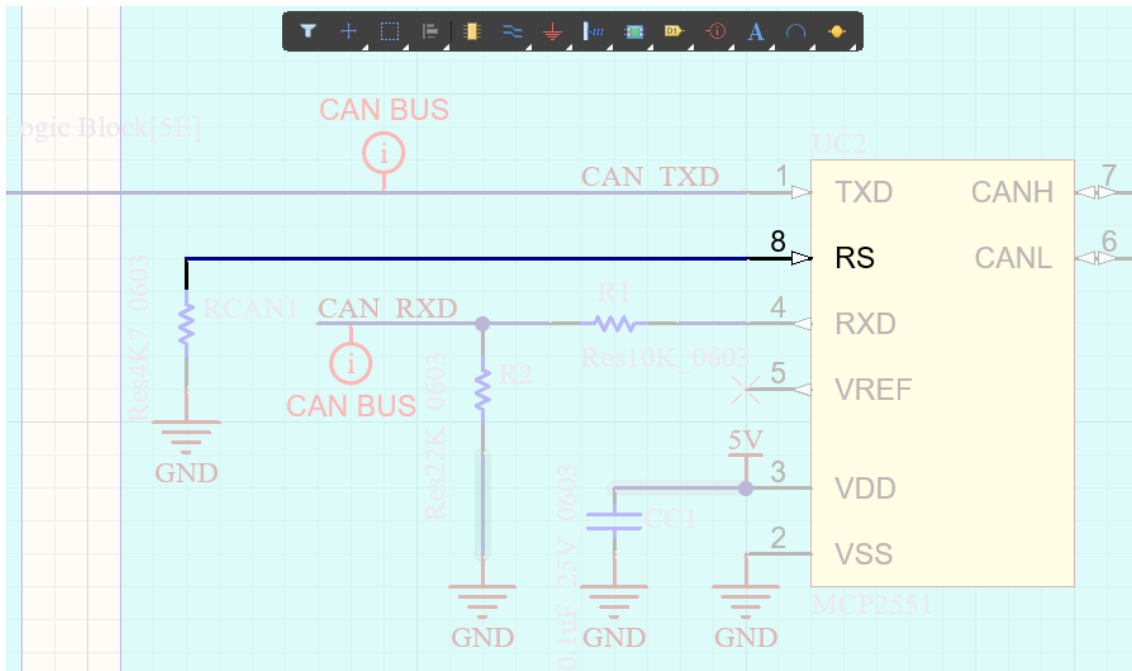


Figure 11. Input of an IC with no driving source

38. Open the Project Options using the **Project » Project Options...** menu.

39. In the *Error Reporting* tab, find the *Violations Associated with Nets* section, Figure 12.

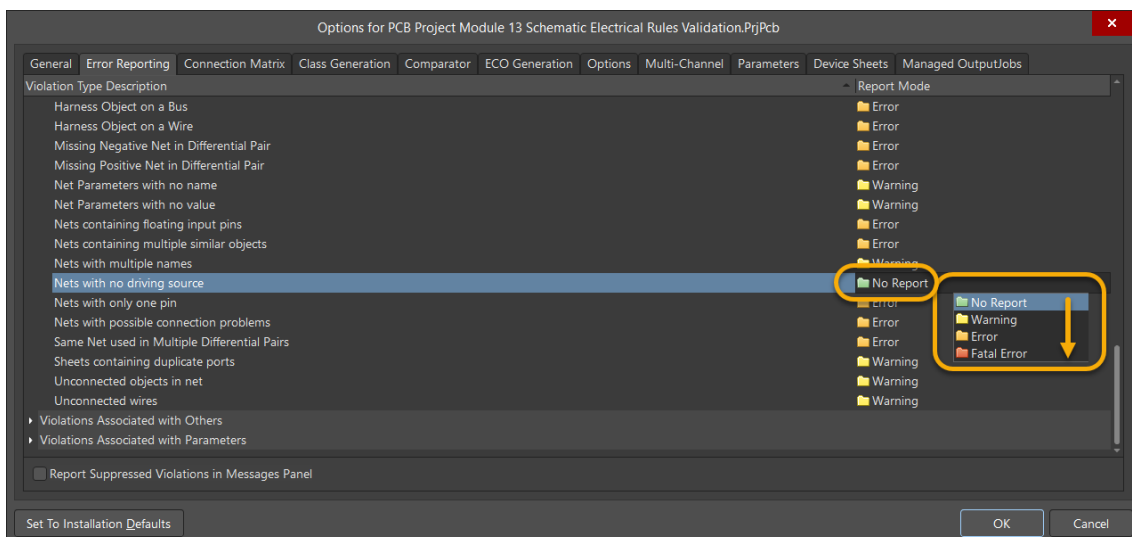


Figure 12. Net Violation Setting

- Locate the *Nets with no driving source* error listing.
  - Set this to **No Report** in the *Report Mode* column.
  - Press the **OK** button to exit the dialog.
40. Validate the project again to verify there are no more *Nets with no driving source* warnings.



## 5.6 Remaining errors - Unconnected Pin / Floating Power Object

41. To resolve the following remaining errors, place a no ERC Directive and connect the floating GND port to the VSS on U1.

- Unconnected Pin
- Floating Power Object

## 5.7 Final Validation

42. Run validation one more time.

Once you have addressed the remaining warnings, you should see the message, as shown in Figure 13 below. A clean validation means there should be no remaining Errors or Warnings. This confirms all identified issues and potential problems have been successfully resolved, ensuring the overall integrity of the schematic design.

43. Close the *Messages* panel, for now.

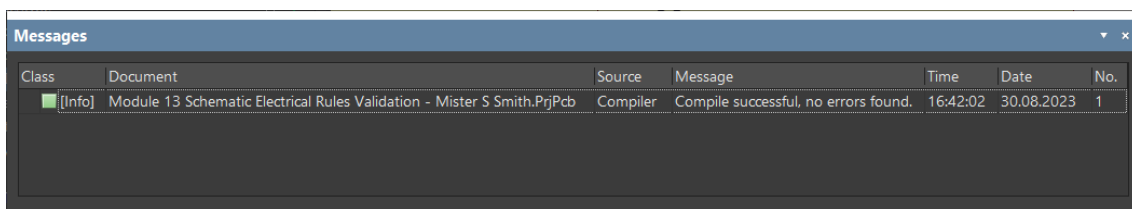
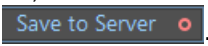


Figure 13. Messages panel with no errors or warnings

44. Select **File » Save All** to save all modifications.

45. Save the modifications to the server:

- At the *Project* panel, next to the Project name you find the command **Save to Server** .
- Select **Save to Server**.
- At the dialog *Save [Project Name]:*
  - Add the comment `Module 13: Schematic Electrical Rules Validation - [Add Your Name]- Finished.`
  - Click on **OK**.

46. When ready, close the project and any open documents.







**Congratulations on completing the Module!**

Module 13: Schematic Electrical Rules  
Validation

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