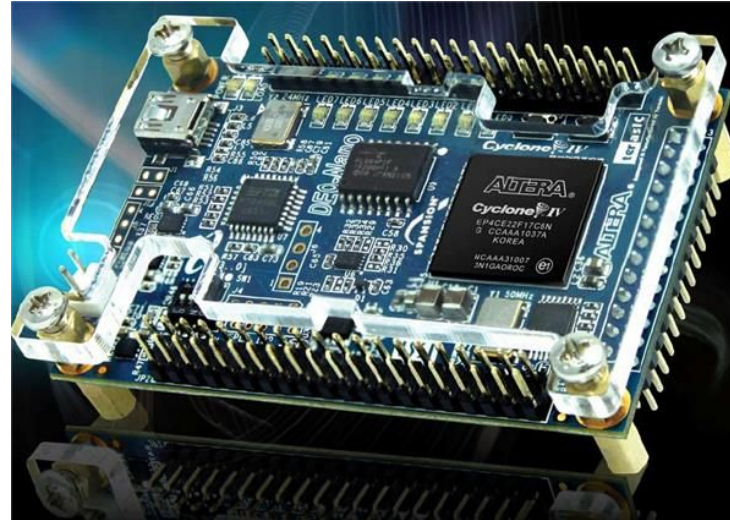
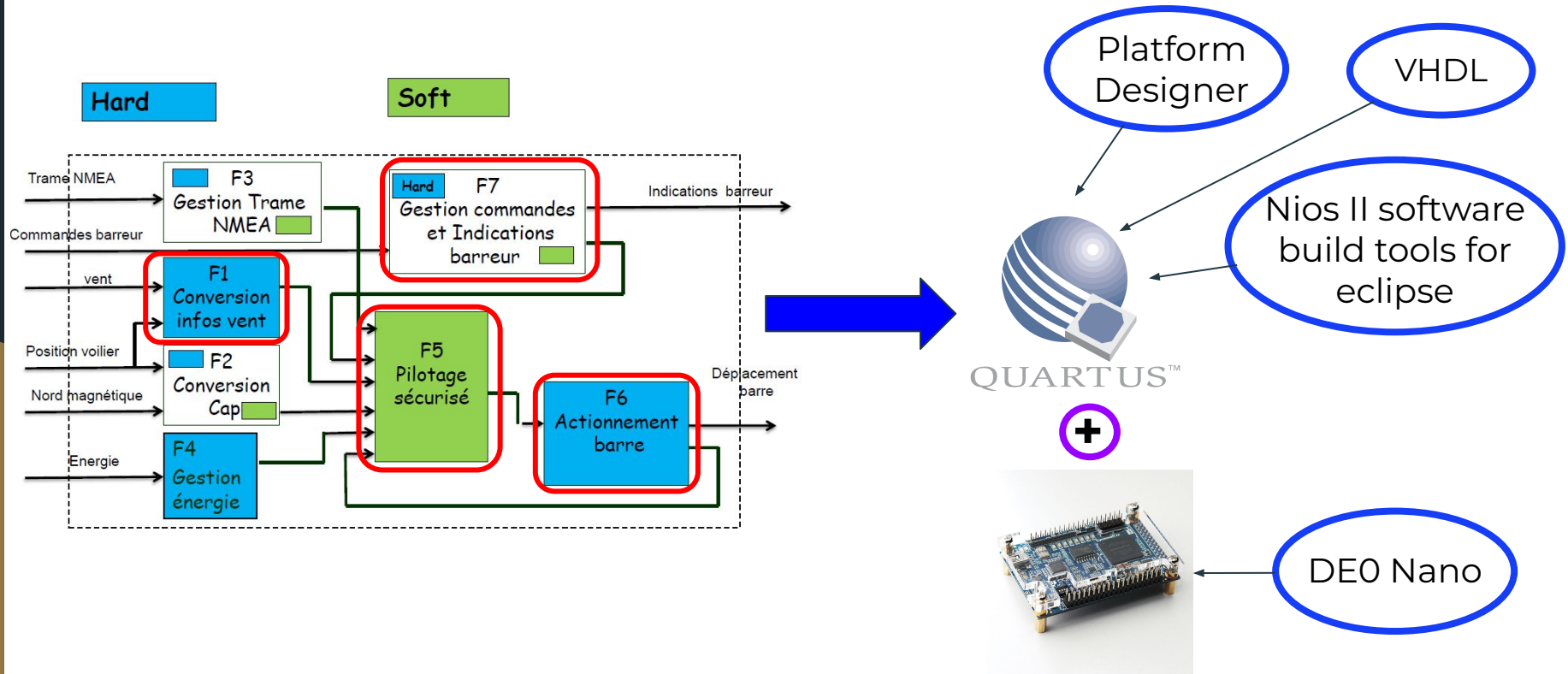


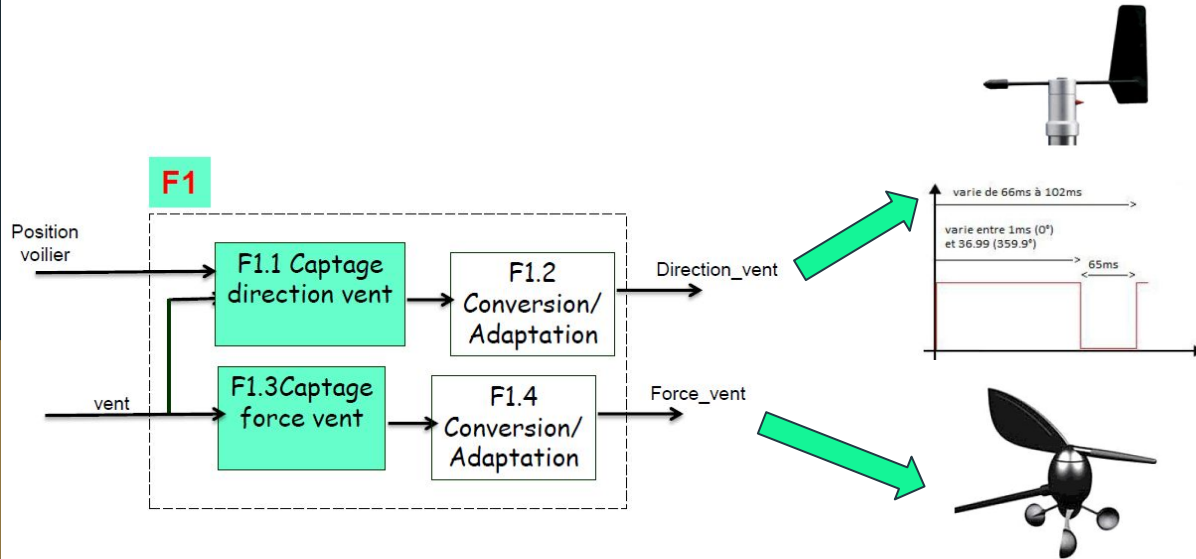
Bureau d'étude VHDL



Présentation du Sujet



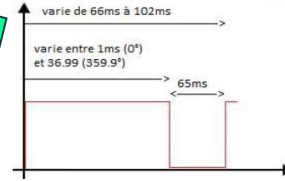
Fonction 1 : Mesure vitesse et direction du vent



Girouette

Mesure Direction du vent :

- ❖ PWM variable
- ❖ Temps état haut : 1 - 36.99 ms
- ❖ Plage angle : 0° - 359°

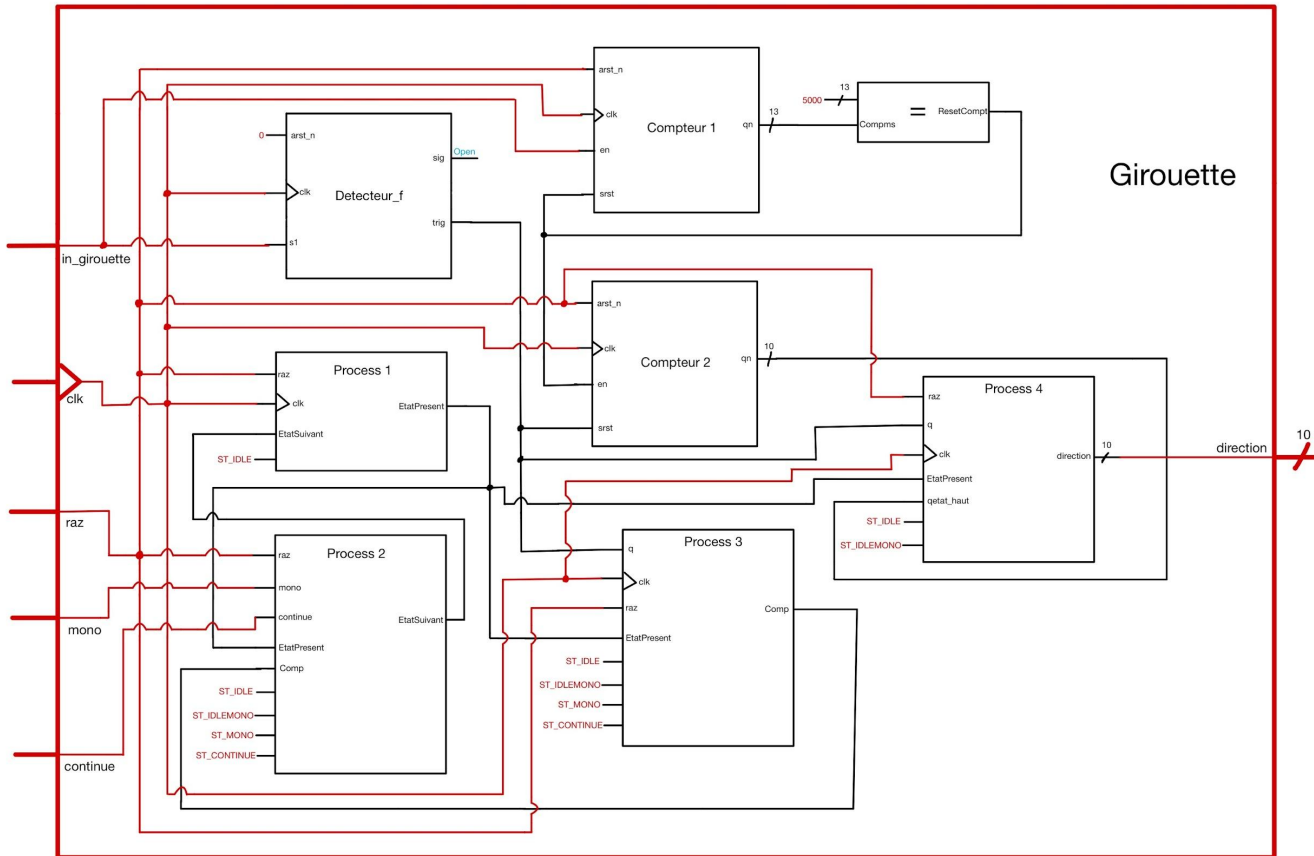


Anémomètre

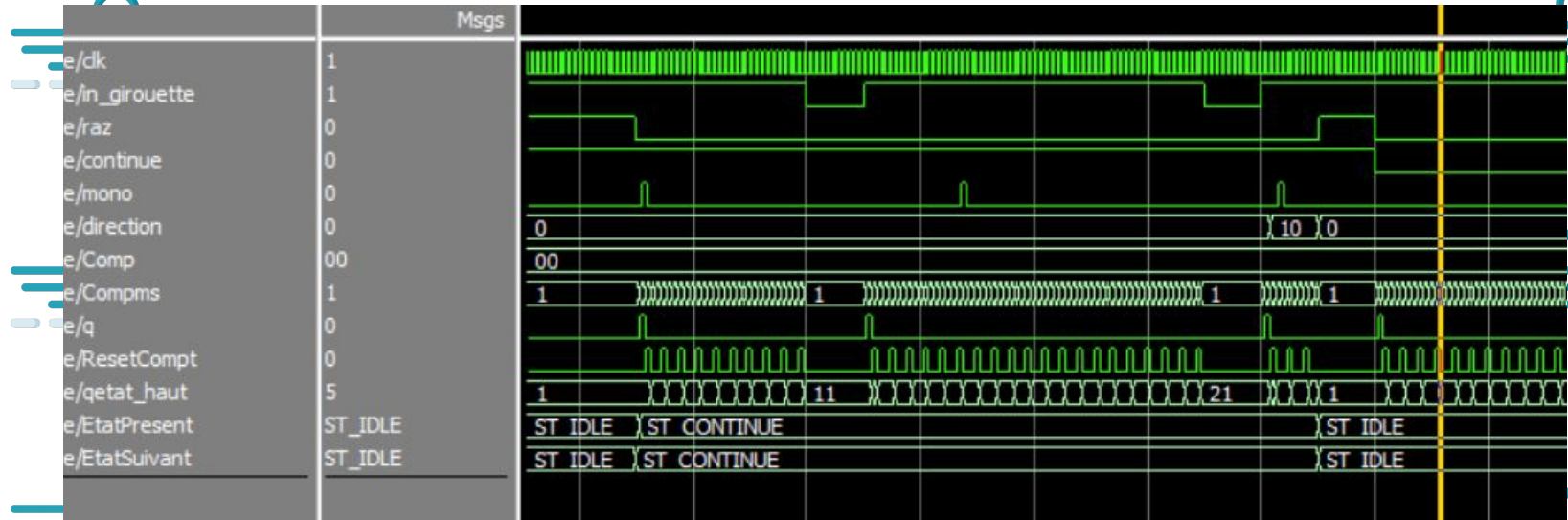
Mesure vitesse du vent :

- ❖ fréquence variable 0 à 250 Hz
- ❖ Vitesse mesurable 0 à 250 km/h

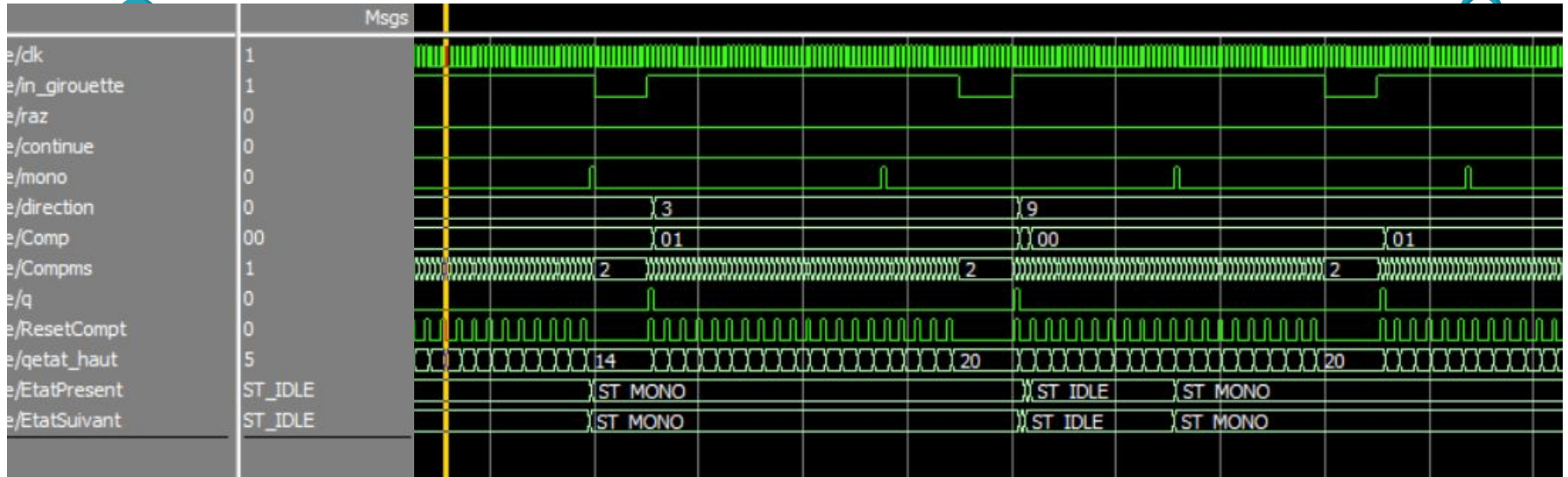
Girouette : Mesure direction du vent



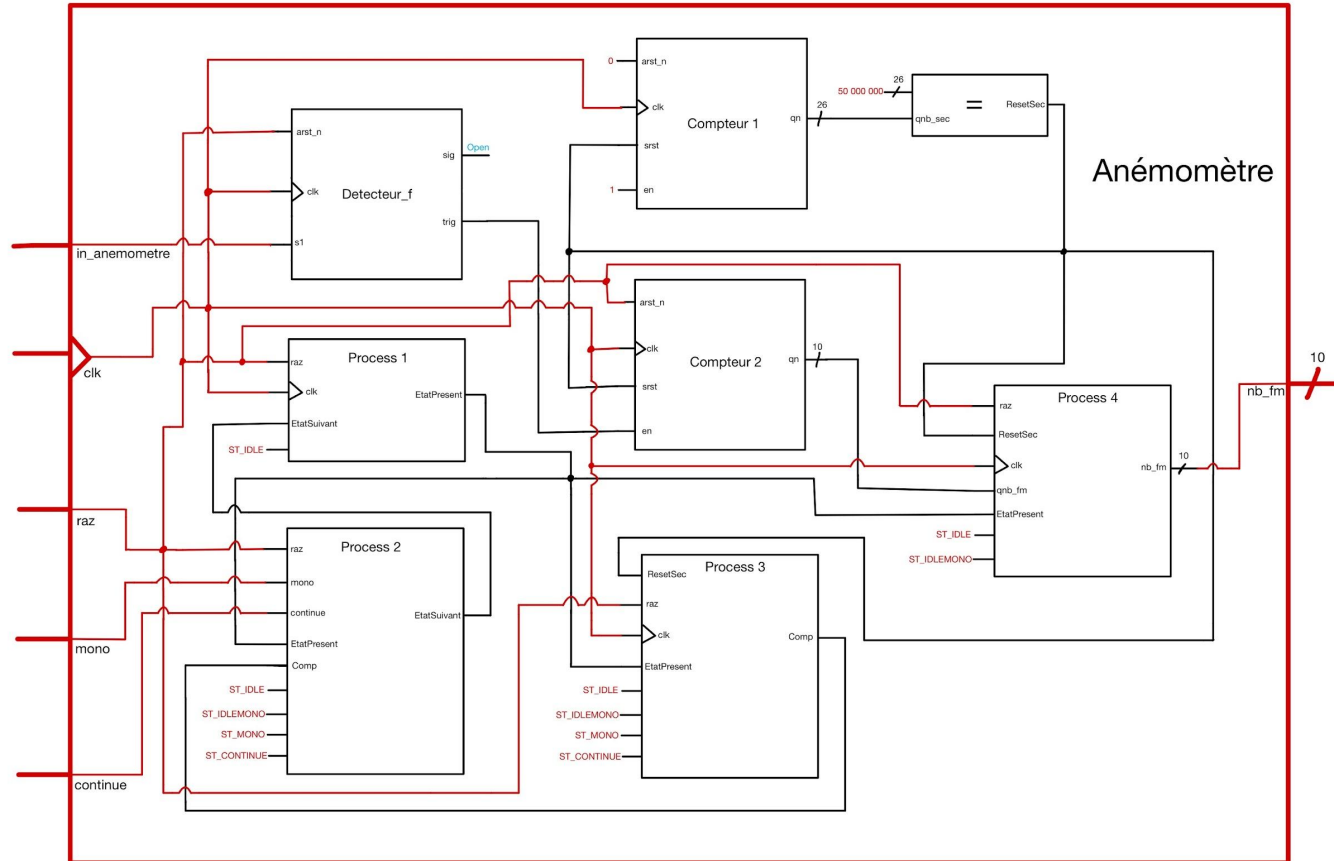
Girouette : Mesure direction du vent



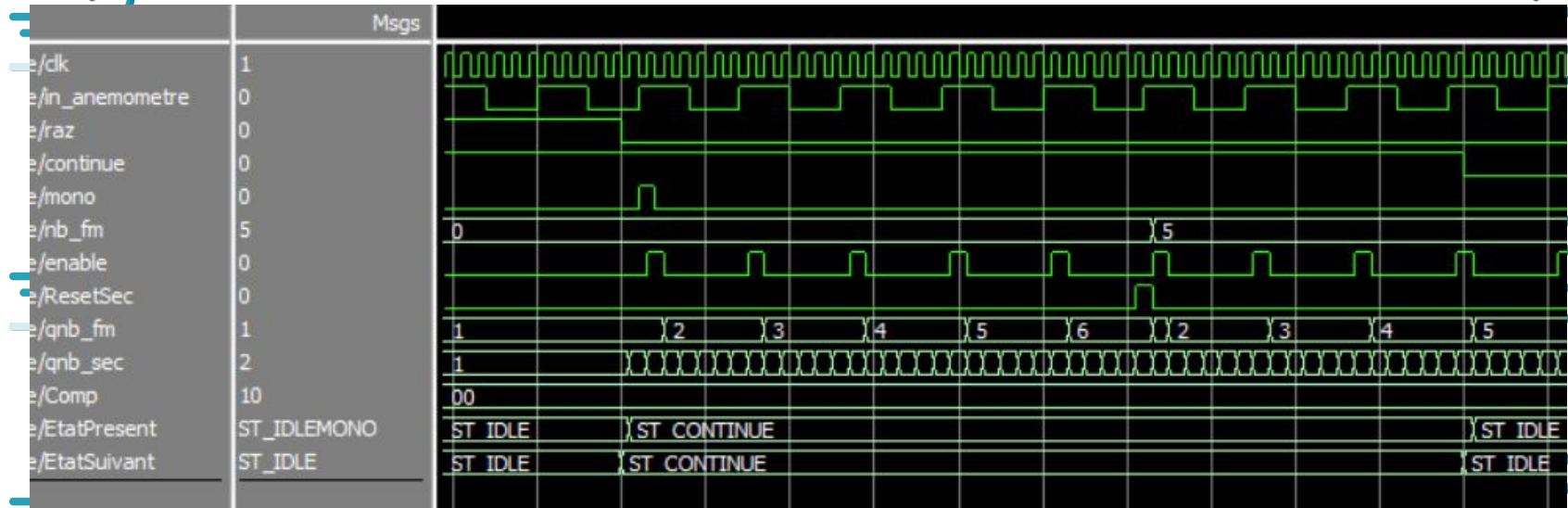
Girouette : Mesure direction du vent



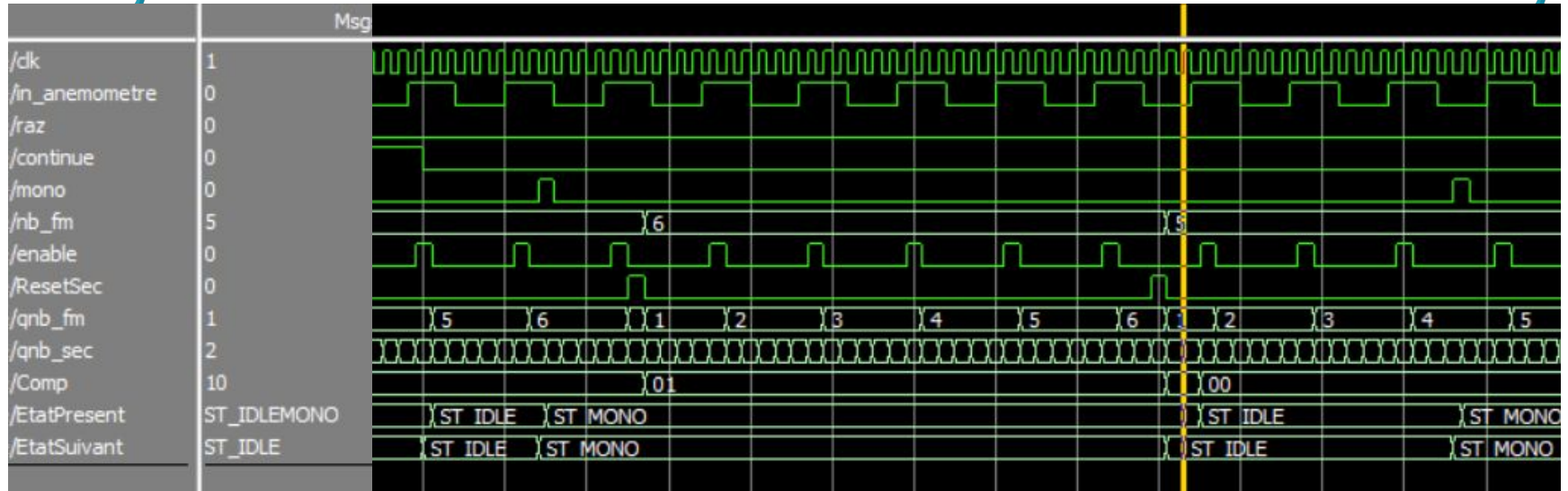
Anémomètre : Mesure vitesse du vent



Anémomètre : Mesure vitesse du vent



Anémomètre : Mesure vitesse du vent



Bus Avalon : Communication avec CPU

Use	Connections	Name	Description	Export	Clock	Base	End	IRQ
✓		clk_0	Clock Source					
		clk_in	Clock Input	clk	exported			
		clk_in_reset	Reset Input	reset				
		clk	Clock Output	Double-click to export	clk_0			
		clk_reset	Reset Output	Double-click to export				
✓		cpu	Nios II Processor					
		clk	Clock Input	Double-click to export	clk_0			
		reset	Reset Input	Double-click to export	[clk]			
		data_master	Avalon Memory Mapped Master	Double-click to export	[clk]			
		instruction_master	Avalon Memory Mapped Master	Double-click to export	[clk]			
		irq	Interrupt Receiver	Double-click to export	[clk]			IRQ 0
		debug_reset_req...	Reset Output	Double-click to export	[clk]			
		debug_mem_slave	Avalon Memory Mapped Slave	Double-click to export	[clk]	# 0x8800	0x8fff	
		custom_instructio...	Custom Instruction Master	Double-click to export	[clk]			
✓		mem	On-Chip Memory (RAM or ROM)...					
		s1	Avalon Memory Mapped Slave	Double-click to export	[clk1]	# 0x0000	0x7fff	
		s2	Avalon Memory Mapped Slave	Double-click to export	[clk1]	# 0x0000	0x7fff	
		clk1	Clock Input	Double-click to export	[clk]			
		reset1	Reset Input	Double-click to export	[clk1]			
✓		uart	JTAG UART Intel FPGA IP					
		clk	Clock Input	Double-click to export	clk_0			
		reset	Reset Input	Double-click to export	[clk]			
		avalon_jtag_slave	Avalon Memory Mapped Slave	Double-click to export	[clk]	# 0x9088	0x908f	
		irq	Interrupt Sender	Double-click to export	[clk]			
✓		avalon_f1_0	Avalon Memory Mapped Slave					
		avalon_slave_0	Conduit	Double-click to export	[clock_sink]	# 0x9080	0x908f	
		avalon_f1_0_condu...	Conduit	Double-click to export	[clock_sink]			
		clock_sink	Clock Input	Double-click to export	clk_0			
✓		avalon_f6_0	Avalon Memory Mapped Slave					
		avalon_slave_0	Conduit	Double-click to export	clk_0	# 0x9040	0x907f	
		avalon_f6_0_condu...	Conduit	Double-click to export	[clock]			
		clock	Clock Input	Double-click to export	[clock]			
✓		avalon_f7_0	Avalon Memory Mapped Slave					
		avalon_slave_0	Conduit	Double-click to export	[clock_sink]	# 0x9000	0x903f	
		avalon_f7_0_condu...	Conduit	Double-click to export	[clock_sink]			
		reset_sink	Reset Input	Double-click to export	[clock]			
		clock_sink	Clock Input	Double-click to export	clk_0			

Platform Designer

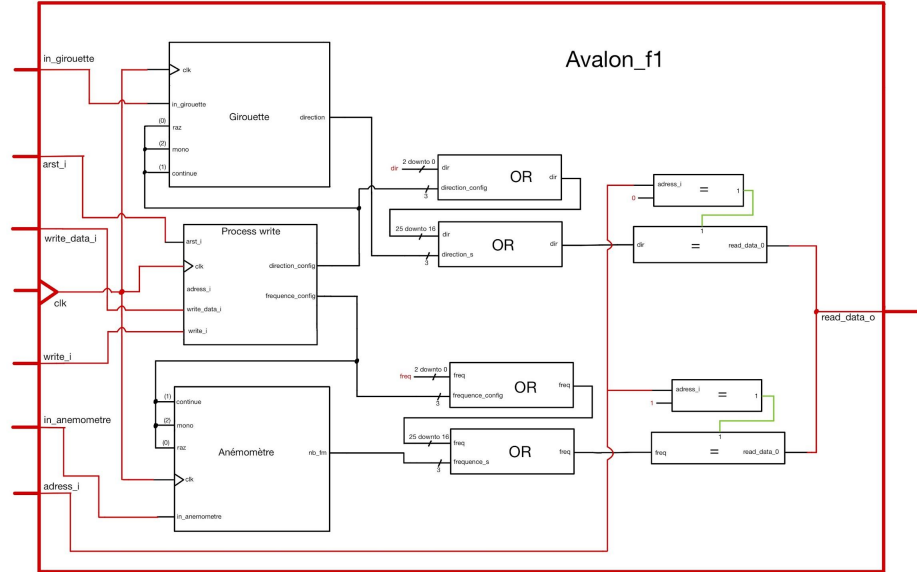
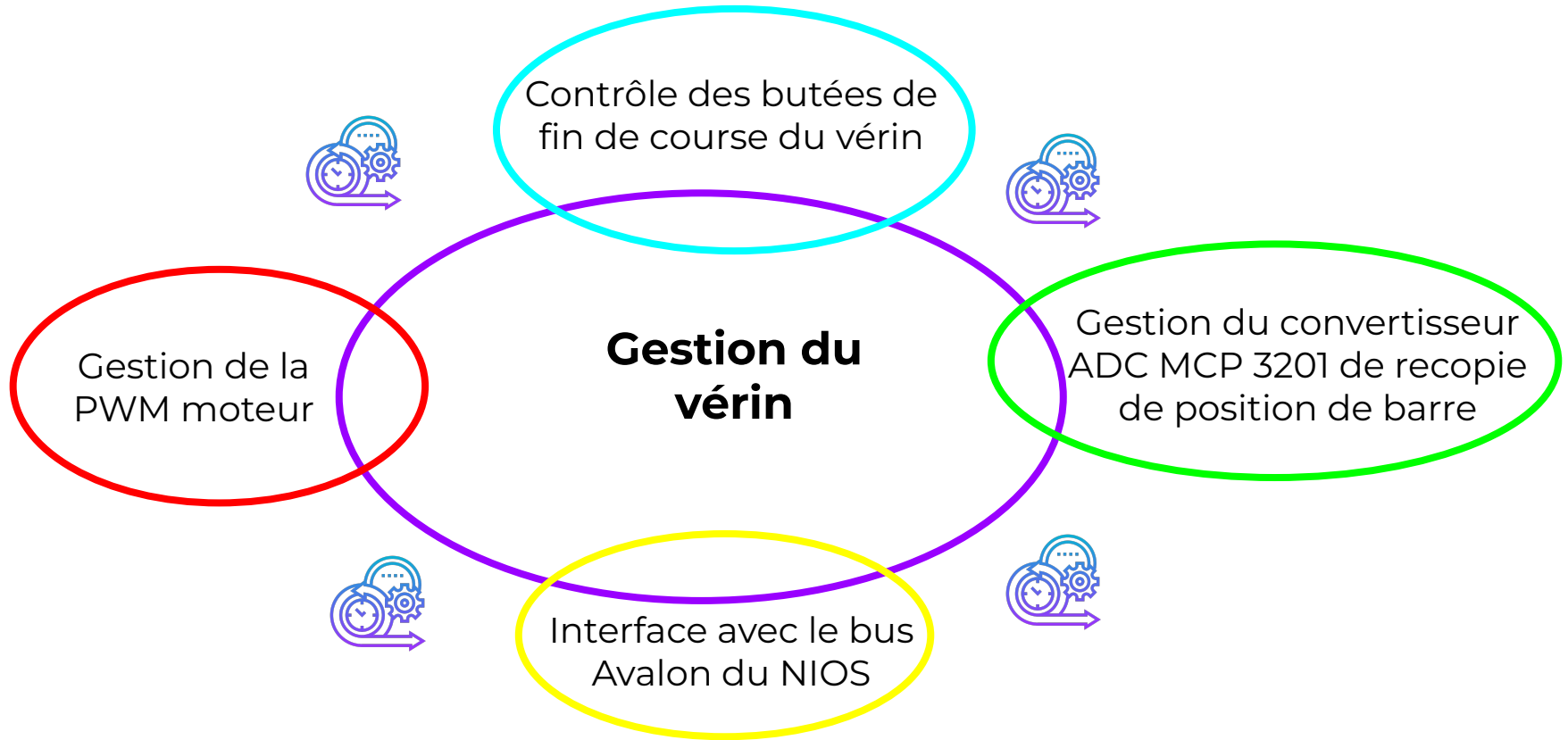
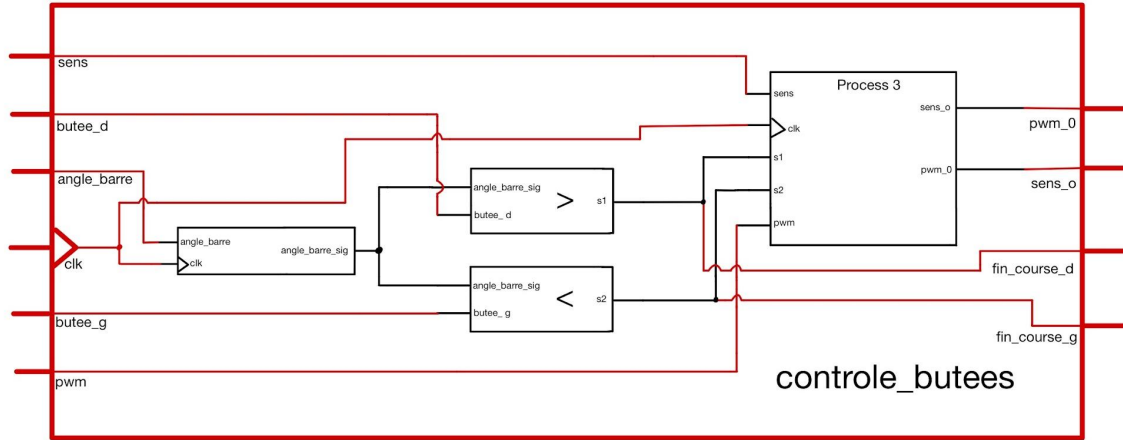


Schéma fonctionnel code VHDL
Avalon fonction 1

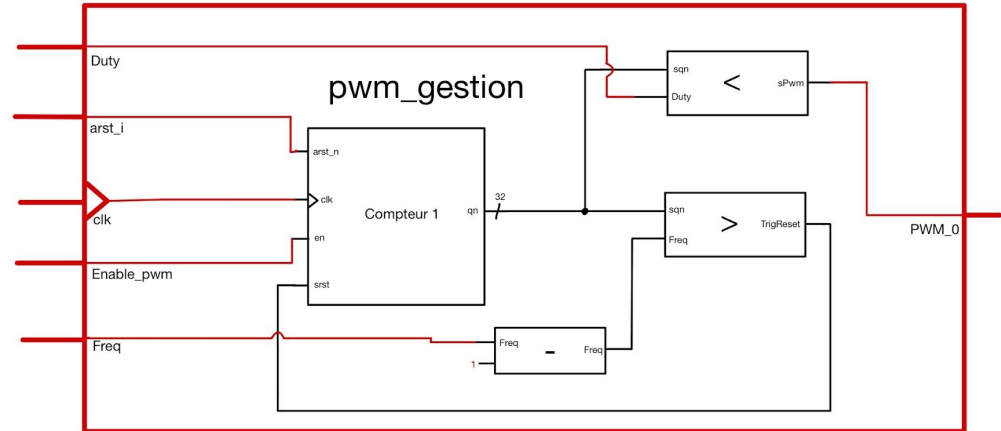
Fonction 6 : Gestion d'un vérin



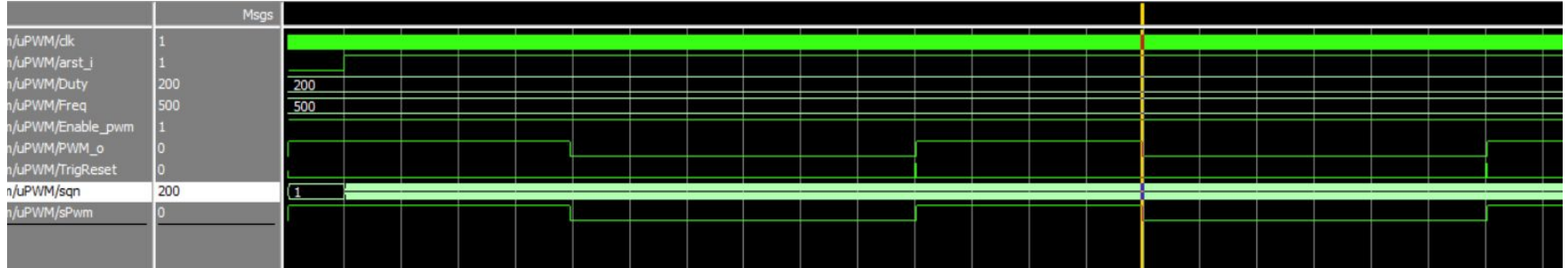


Surveiller position de l'angle de la barre, si l'angle en dehors des butées, mettre PWM à 0

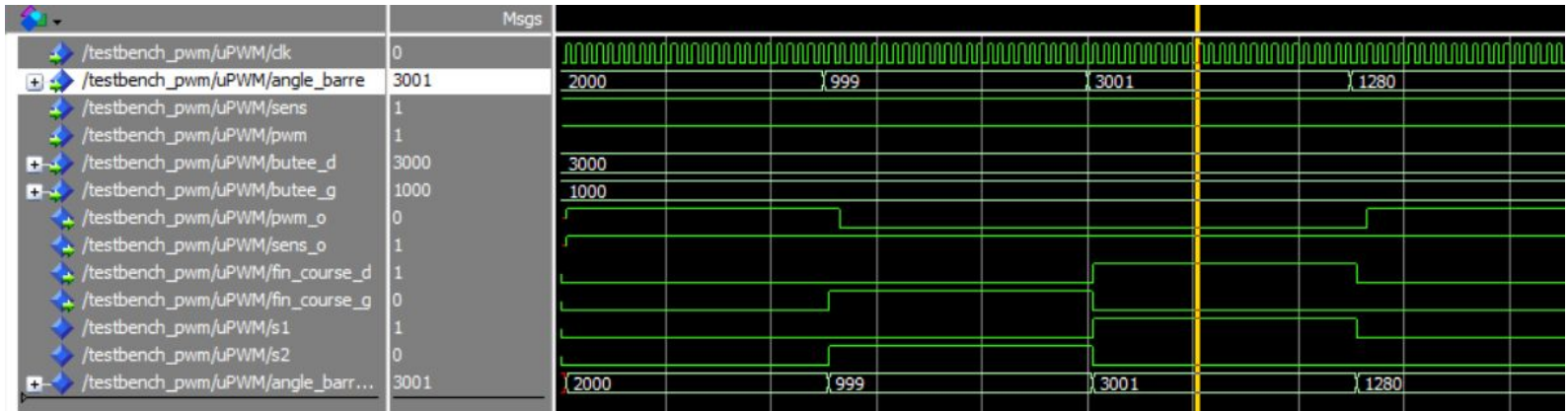
Générer un signal PWM variable selon une Fréquence et un rapport cyclique choisis



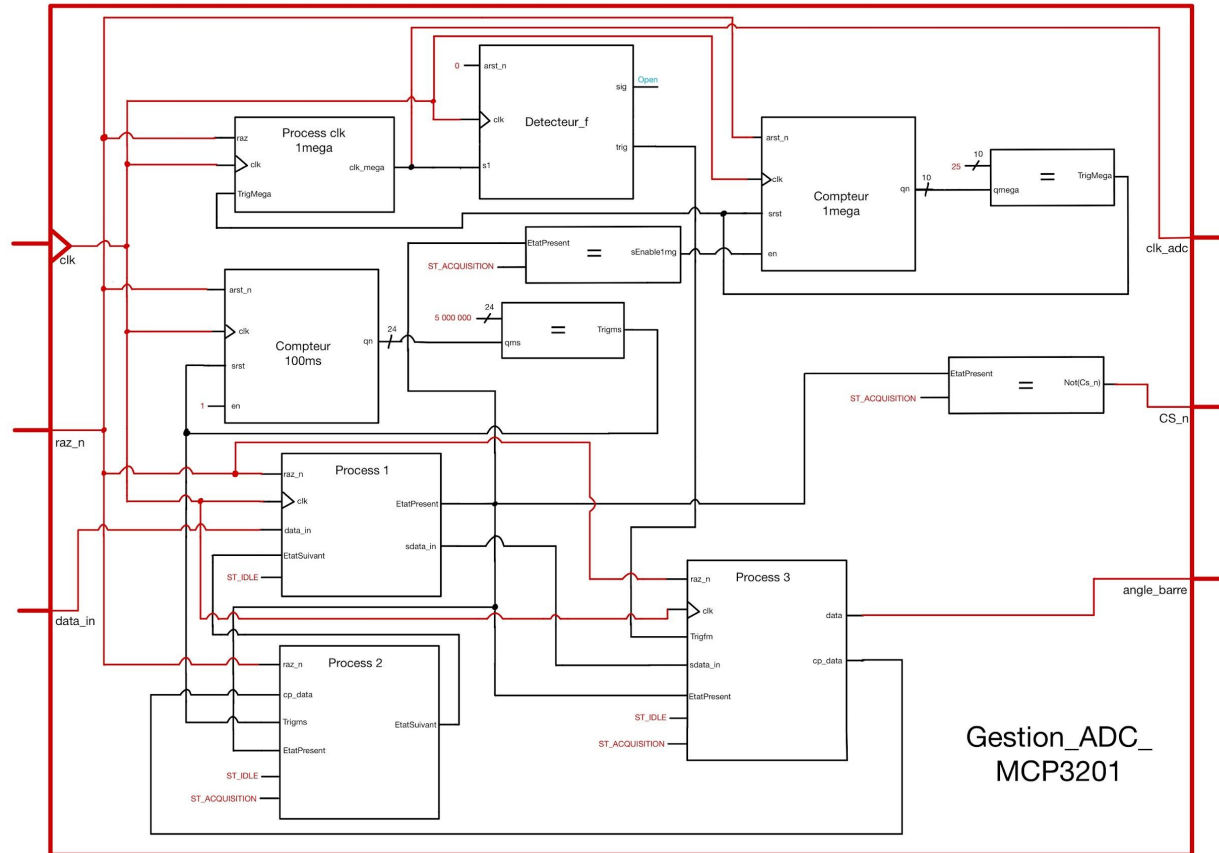
Gestion PWM



Contrôle des butées

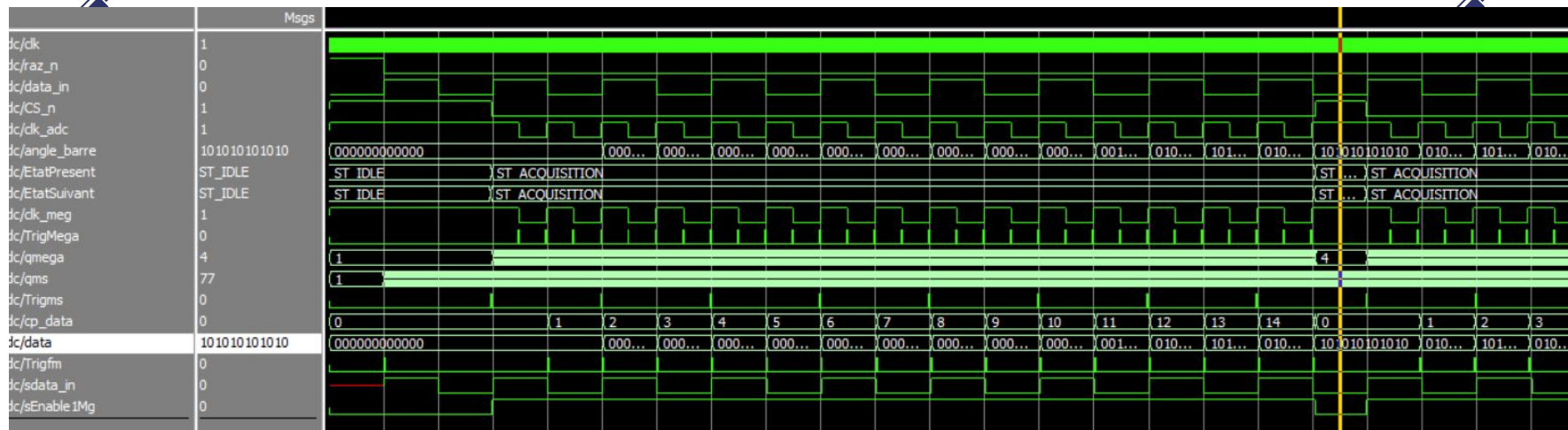


Gestion du convertisseur ADC MCP 3201 de recopie de position de barre

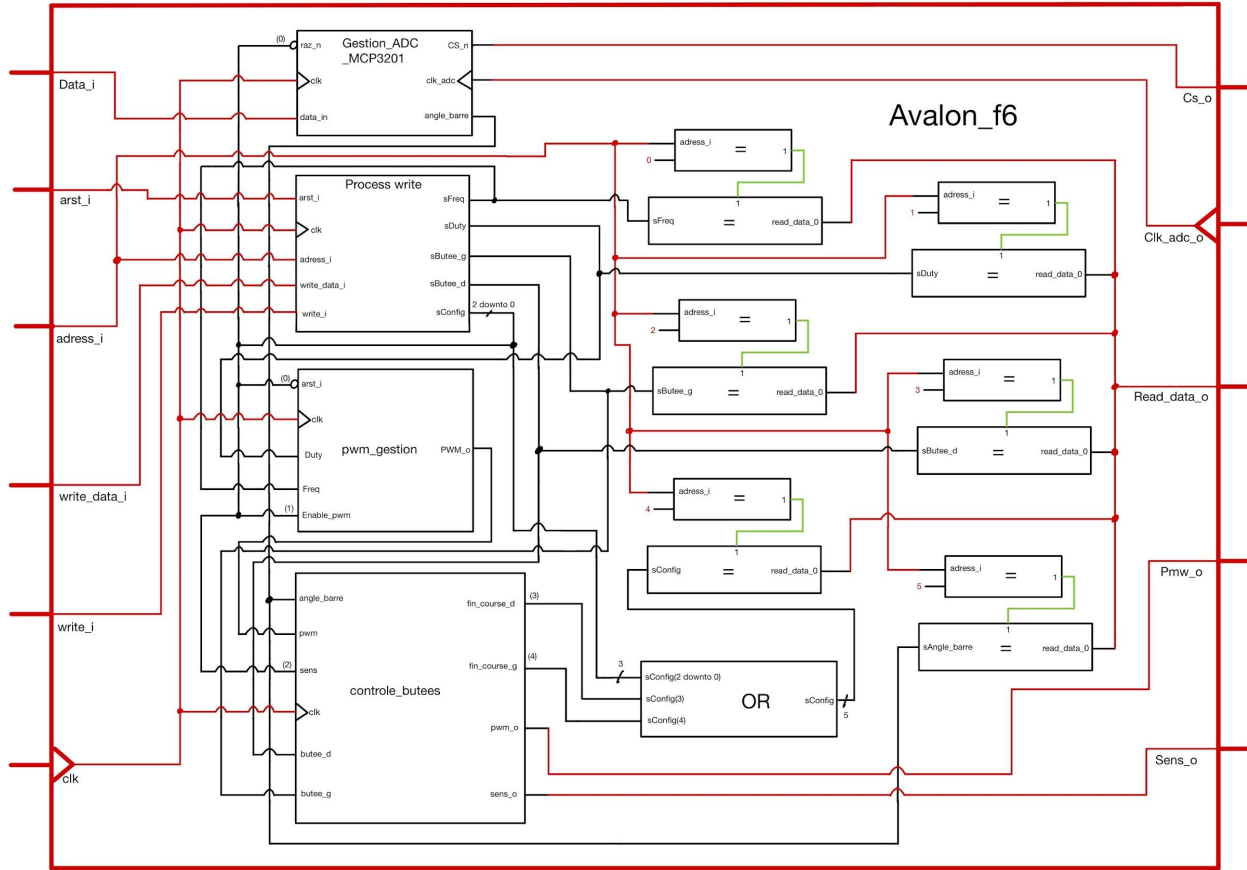


Gestion_ADC_
MCP3201

Gestion du convertisseur ADC MCP 3201 de recopie de position de barre



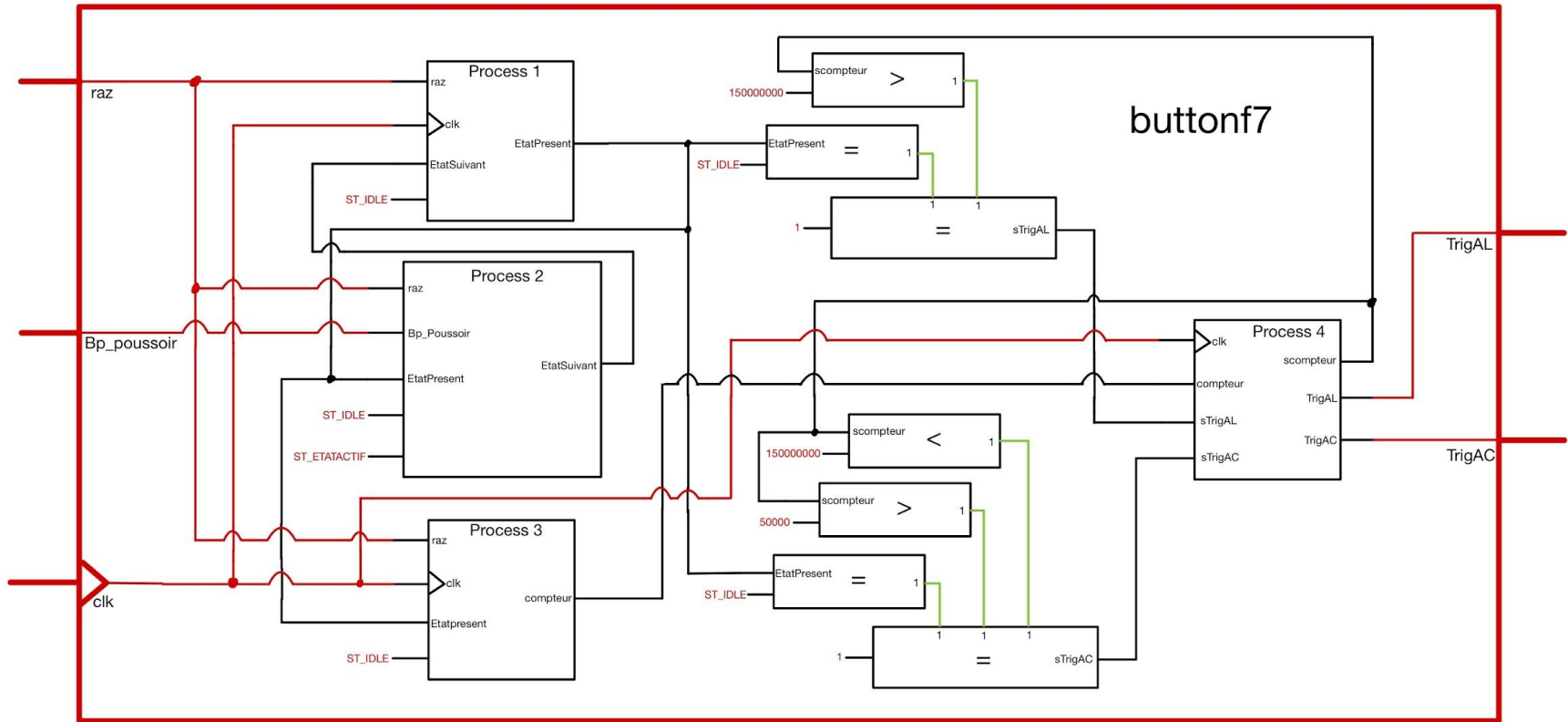
Interface avec le bus Avalon du NIOS



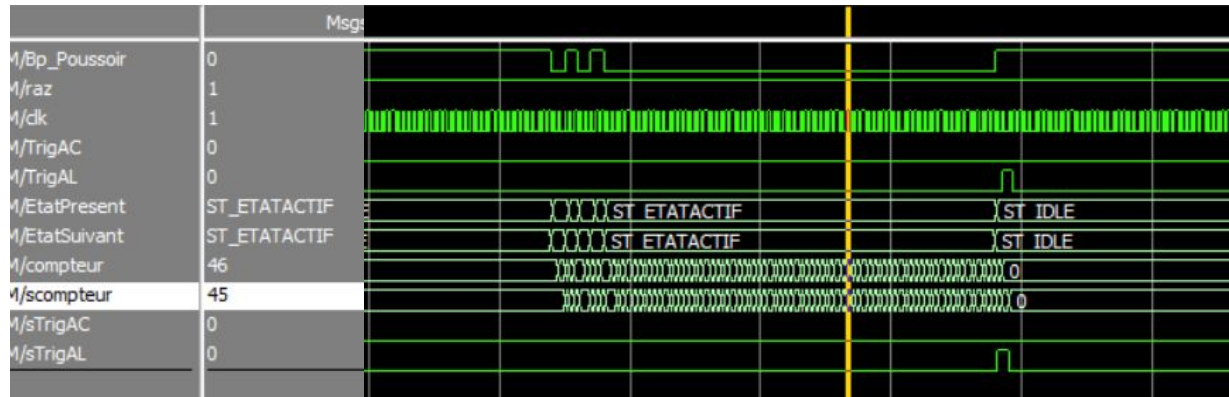
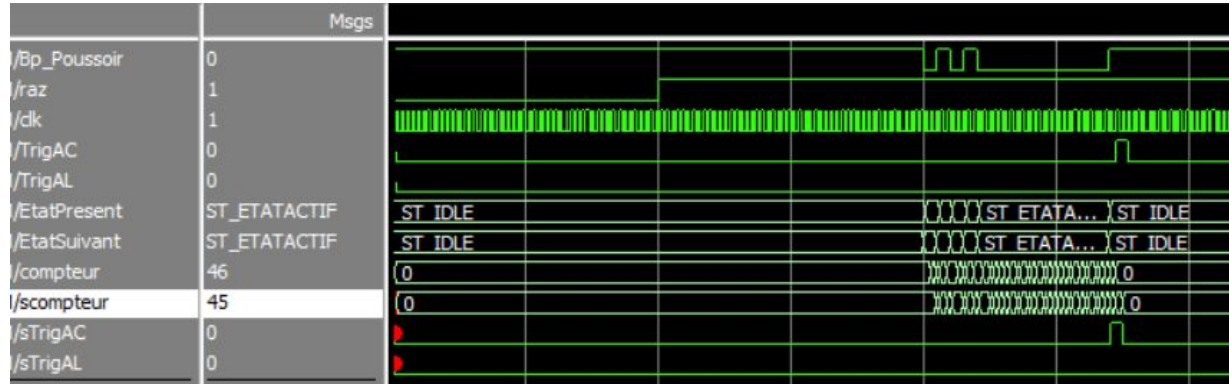
Programme Soft



Fonction 7 : Interface et IHM



Fonction 7 : Interface et IHM





CONCLUSION

