**EC 413 Lab 5 Report**

Brendan Shortall – U71270986 – 10/28/2022

**Datapath and Timing Diagrams:**

Graphical user interface

Description automatically generatedThese sections were tested by creating a testbench with multiple instruction inputs. By looking at the timing diagram you can see that the alu output (final out) would represent the instruction that was 2 clock cycles previously. This makes plenty of sense since the data has to flow through each stage. I also included the write/read selects at certain stages of the pipeline to ensure that the data was flowing properly.

In this timing diagram you can see the write select value iterating through each stage every clock cycle. You can also see that the ALU\_out of a particular instruction doesn’t register until 2 clock cycles after. This information shows that the datapath and timing diagram works well.

**ALU:**

The ALU was tested by creating a testbench with multiple kinds of operands. Including I-type and R-type add, sub, srt. As well as the logical operations like AND OR, etc. All of the ALU functions were tested and gave accurate results that can be viewed from the ALUOut 2 clock cycles after the instruction is input.

**Register File:**

The register file was tested in multiple ways. One way was just executing a particular instruction and making sure that the operation yields the expected values for what should be in each register. Another way is by doing subsequent operations on a single register. This ensures that both the read and write function of the register file are working properly.