

```
1 module fsm(  
2     input restart,  
3     input clk,  
4     input rst,  
5     input pause,  
6     input goto_third,  
7     output [2:0] out1,  
8     output [2:0] out2,  
9     output even,  
10    output odd,  
11    output terminal  
12 );  
13 //                                state out1, out2, even, odd, terminal  
14 reg [11:0] state;  
15 parameter [11:0] FIRST = 12'b000_011_010_1_0_0;  
16 parameter [11:0] SECOND = 12'b001_101_100_0_1_0;  
17 parameter [11:0] THIRD = 12'b010_010_111_1_0_0;  
18 parameter [11:0] FOURTH = 12'b011_110_011_0_1_0;  
19 parameter [11:0] FIFTH = 12'b100_101_010_1_0_1;  
20  
21 assign out1 = state [8:6];  
22 assign out2 = state [5:3];  
23 assign even = state[2];  
24 assign odd = state[1];  
25 assign terminal = state[0];  
26  
27 always_ff @(posedge clk, posedge rst)  
28 begin  
29     if (rst) state <= FIRST;  
30     else  
31     begin  
32         case(state)  
33             FIRST: if (restart | pause) state <= FIRST;  
34                     else state <= SECOND;  
35             SECOND: if (restart) state <= FIRST;  
36                      else if (pause) state <= SECOND;  
37                      else state <= THIRD;  
38             THIRD: if (restart) state <= FIRST;  
39                     else if (pause) state <= THIRD;  
40                     else state <= FOURTH;  
41             FOURTH: if (restart) state <= FIRST;  
42                      else if (pause) state <= FOURTH;  
43                      else state <= FIFTH;  
44             FIFTH: if (goto_third) state <= THIRD;  
45                     else if (restart) state <= FIRST;  
46                     else if (pause) state <= FIFTH;  
47             default: state <= FIRST;  
48         endcase  
49     end  
50 end  
51 endmodule
```