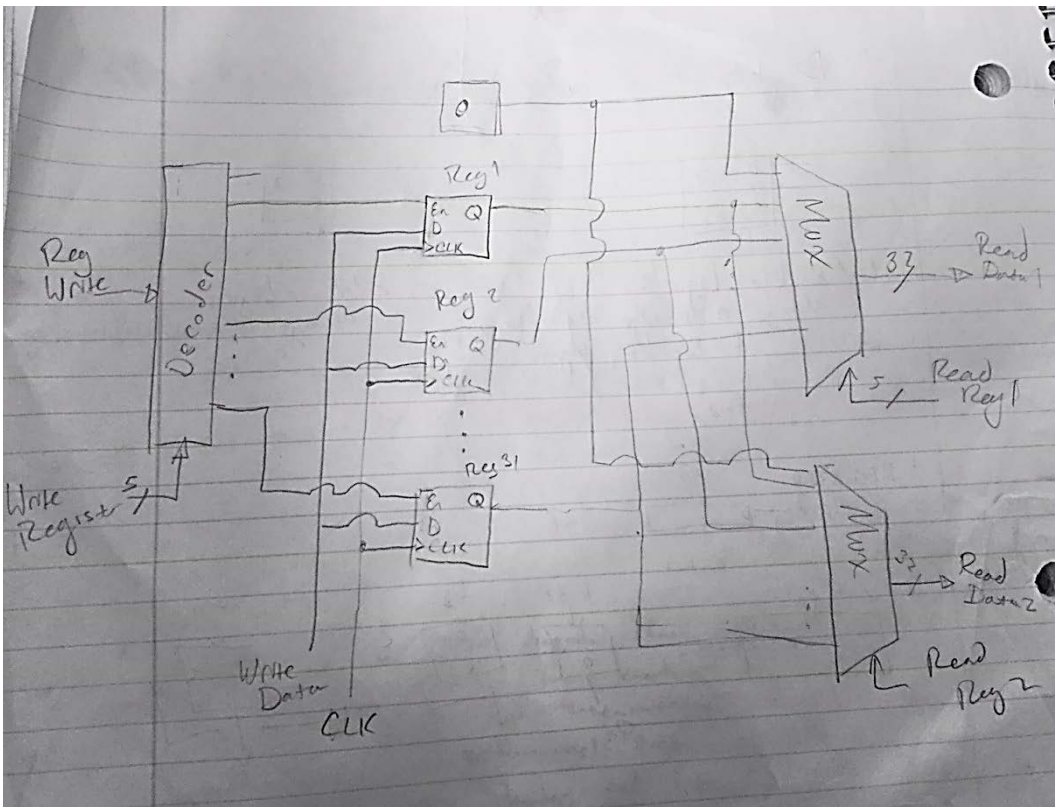
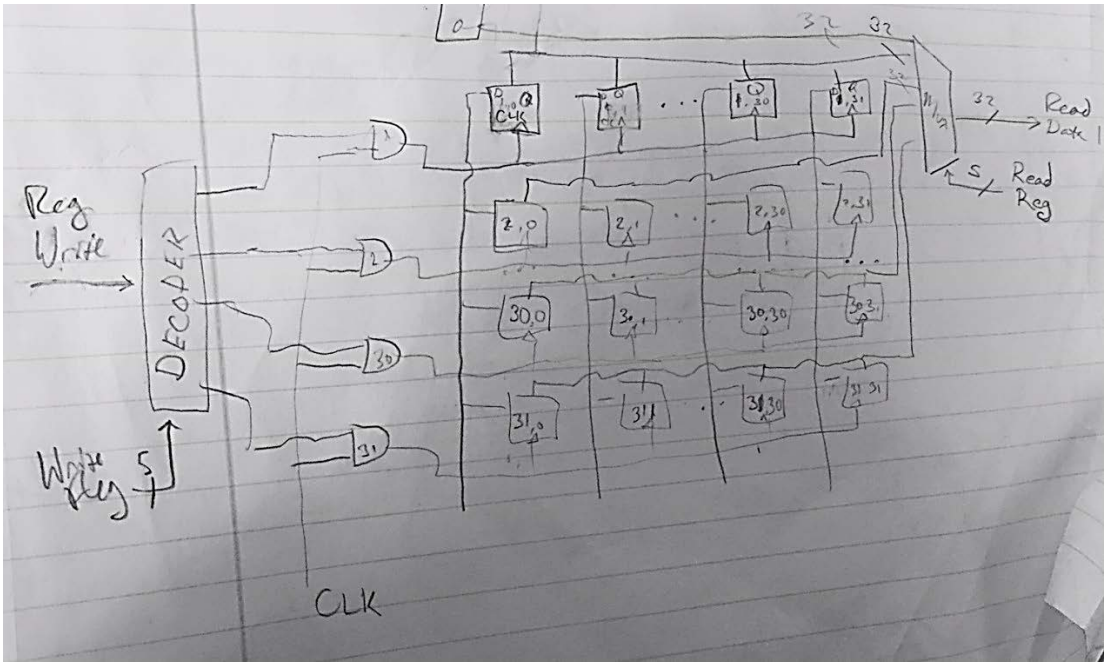
Brenna Manning CompArch HW4 Deliverable 1:

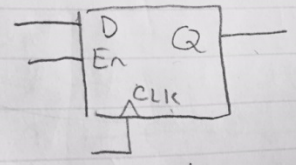
OPTION 1:

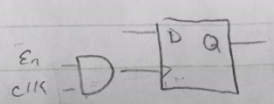


OPTION 2:



D Flip-Flop w/ Enable





1st Enable Logic :

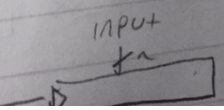
```
always @(posedge clk) begin
    if (wrenable) begin
        q = d
    end
end
```

2nd Enable Logic :

```
always @(posedge (clk & wrenable)
    q=d;
end
```

Only at positive edge of both

REGISTER



P0