11-20-15
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OUR CURRENT STATUS:

- Assembly test completed and submitted
- CPU design completed *see Figure 1.
- All modules completed, and tested with individual test benches.
- Master test script that runs all test benches completed and tested.
- Plan for how to implement all modules together with .data from assembly and passing of information completed *see [Instruction Flow Spreadsheet]

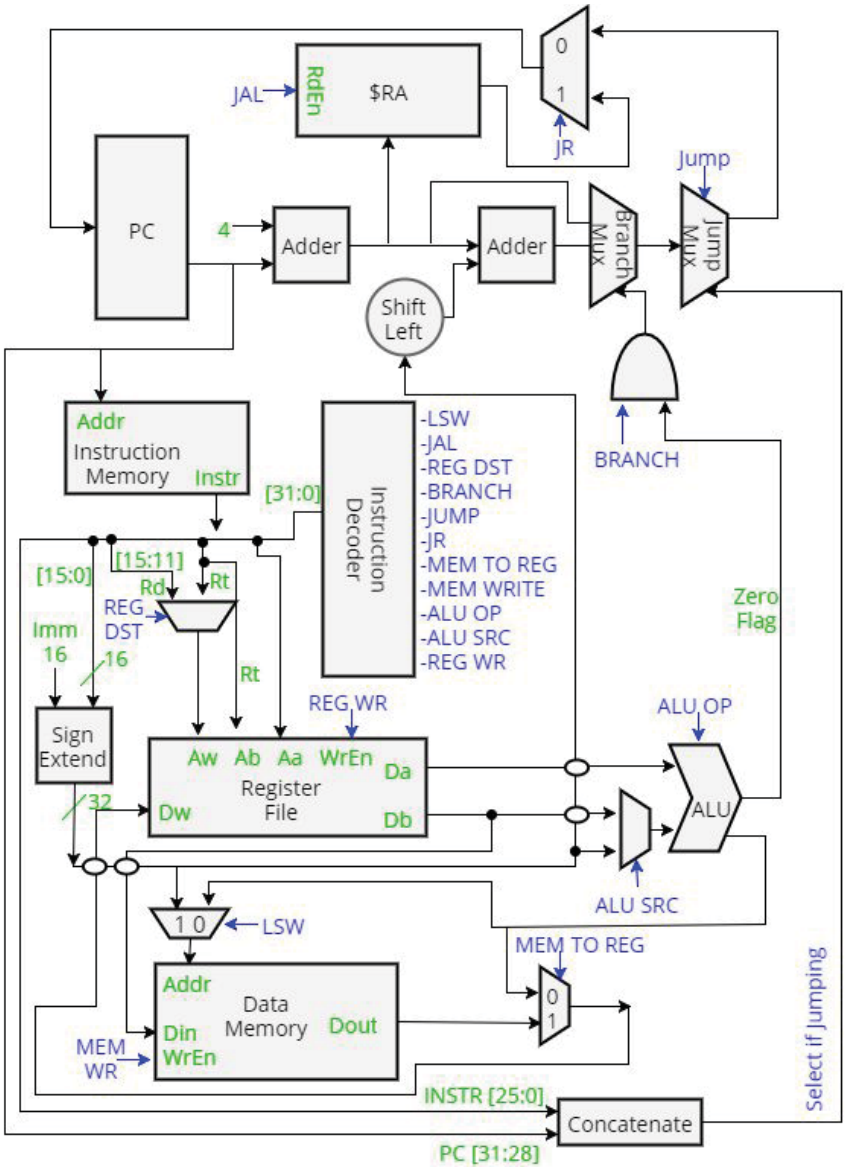

Figure 1: A schematic representation of our full single cycle CPU.