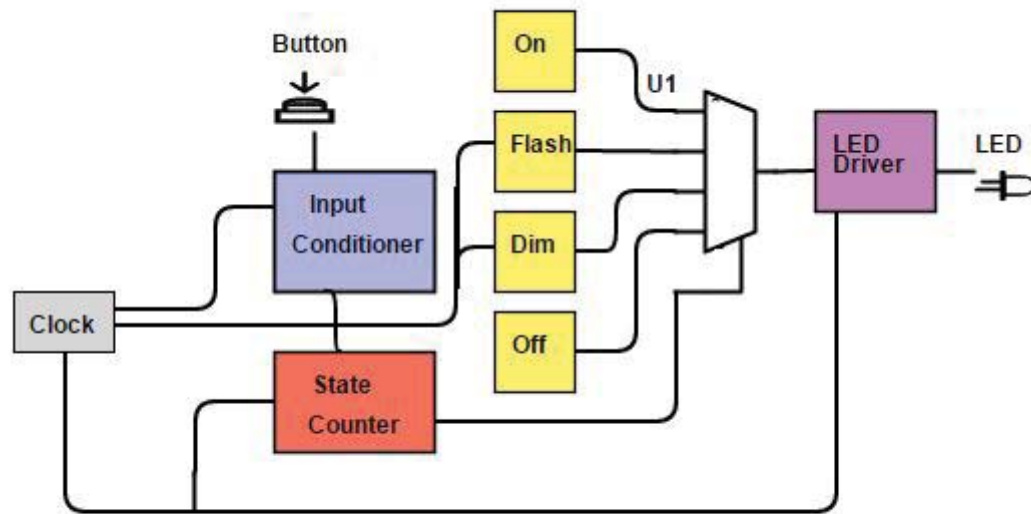


## BLOCK DIAGRAM AND SCHEMATICS



The block diagram for the controller is shown here. When the button is pressed, the Input Conditioner block debounces and conditions the signal to account for noise, etc, so that the state counter is only updated when the button is pressed. The schematic for the input conditioner is shown below. I chose to use a 5-bit counter to account for a wait time of 1 ms, because  $P=(2^N)/f$ , such that P is equal to the desired wait time of 1ms, and f is equal to the frequency of the clock, 32,768hz. N represents the number of bits needed for the Up Counter being used.

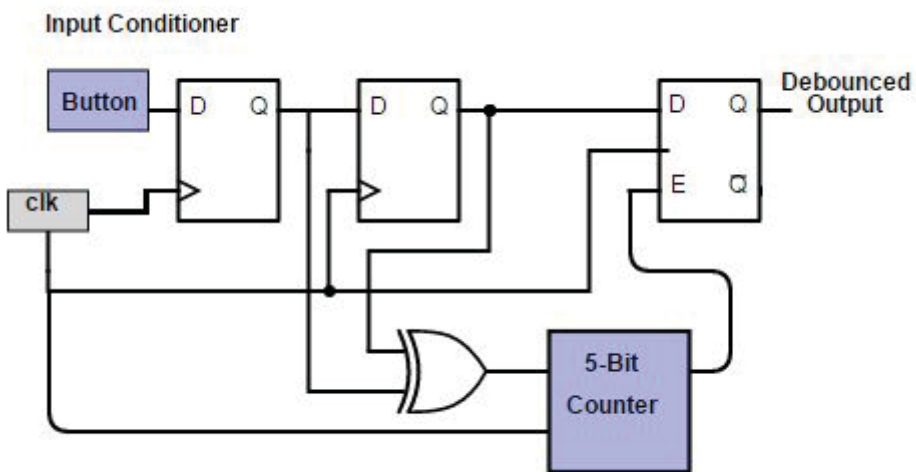
### COST:

The two D-flip flops without an enable cost 13 each, and the flip flop that does have an enable costs 20. The XOR gate has a cost of 8, being made up of a two input OR gate (cost=3), a two input AND gate(cost = 3) and a two input NAND gate (cost=2).

Within the counter there are 5 JK Flip Flops, 3 2-input AND gates, and 1 5-input AND gate. Each JK Flip Flop is made up of 4 two input NAND gates, so they cost 8 each, for a cost of 40. Each 2-input AND gate costs 3, so the 3 AND gates cost 9. The 5 input AND gate costs 6. The counter inside the Input Conditioner has a cost of 55. The Input Conditioner has a total cost of 109 GIE.

| Gate             | Cost         |
|------------------|--------------|
| D-Flip Flops(x2) | 26 (13 each) |

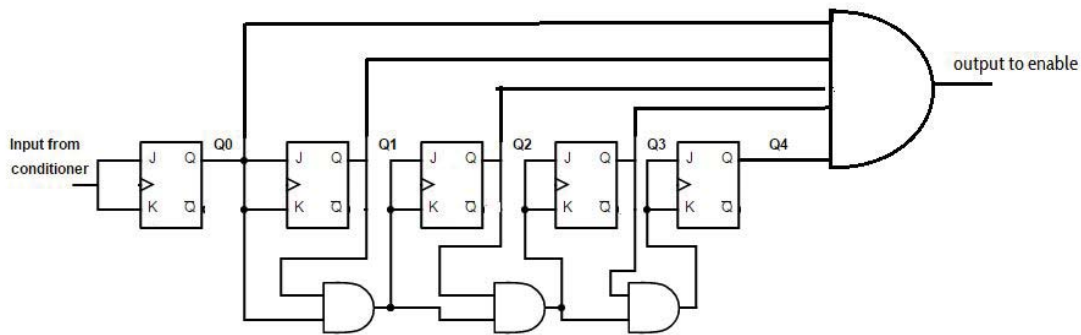
|                                  |             |
|----------------------------------|-------------|
| D-Flip Flop with Enable          | 20          |
| XOR                              | 8           |
| JK Flip Flops (x5)               | 40 (8 each) |
| 2-Input AND gates (x3)           | 9 (3 each)  |
| 5-Input AND gate                 | 6           |
| Total Cost for Input Conditioner | 109         |



The inputs to the Input Conditioner are the Button signal and the clock pulse. The output is a debounced signal from the button.

Here is the schematic of what is going on inside of the 5-bit counter.

## 5-Bit Counter

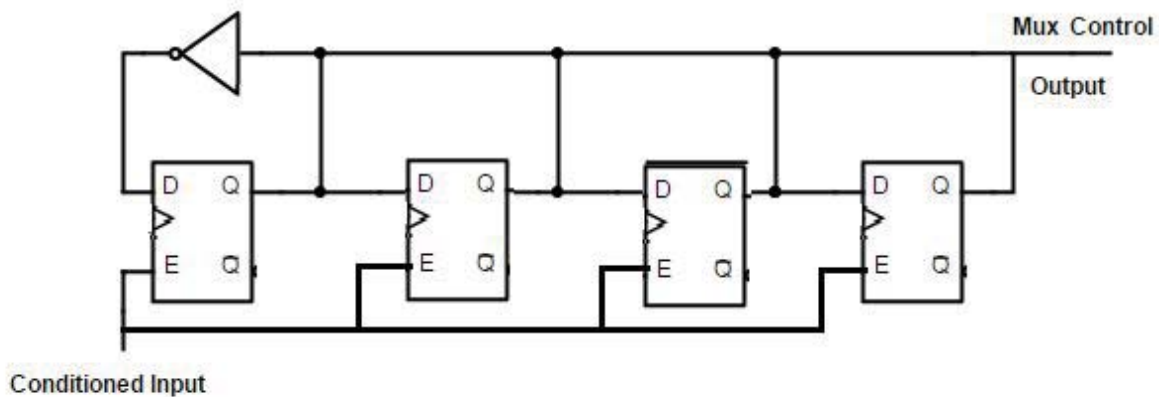


The state counter below was necessary for this design to keep track of what mode the light should be in, and control which light pattern is being displayed.

The inputs are the conditioned output from the Input Conditioner, and the clock pulse.

The output is a 4bit 1 hot number that controls the multiplexer which selects which light pattern to drive to the LED.

## State Counter

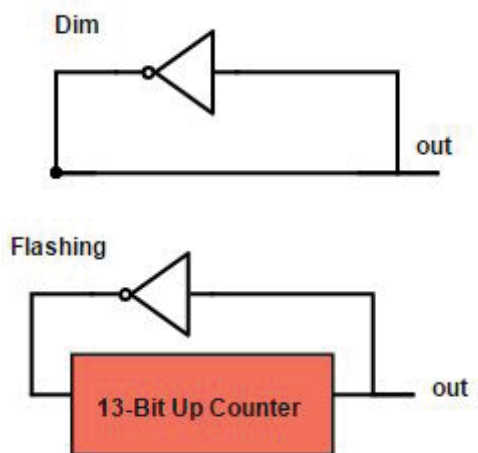


### COST:

Each of the 4 D-FlipFlops with Enables has a cost of 20, and the NOT gate has a cost of 1, for a total cost of 81 for the State Counter.

| Gate                          | Cost         |
|-------------------------------|--------------|
| NOT                           | 1            |
| D-Flip Flops with Enable (x4) | 80 (20 each) |

|                     |    |
|---------------------|----|
| Total State Counter | 81 |
|---------------------|----|



The four modes:

“On” is always 1

“Off” is always 0

“Dim” is always alternating between on and off each clock cycle. (50% duty cycle)

“Flashing” uses a 13 bit up counter controlling when it changes between on and off, so that the light will flash at a frequency of 3Hz. (Calculated with  $P=(2^N)/f$ ). The 13 bit Up Counter is constructed exactly the same way as the 5 bit Up Counter was above.

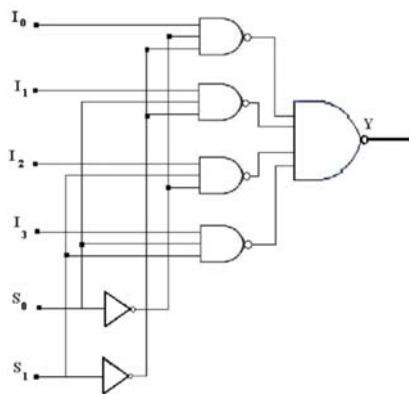
Each mode is an input to a multiplexer, and the output from the state counter will control which of the mux inputs goes to the LED Driver: either on, off, flashing, or dim.

#### COST:

Each NOT gate only has a cost of 1. The counter is made up of 13 JK Flip Flops which each have a delay of 8, 11 2-Input AND Gates which each have a delay of 3, and a 13-Input AND Gate, which has a cost of 14.

| Gate              | Cost |
|-------------------|------|
| NOT (for Dim)     | 1    |
| NOT(for Flashing) | 1    |

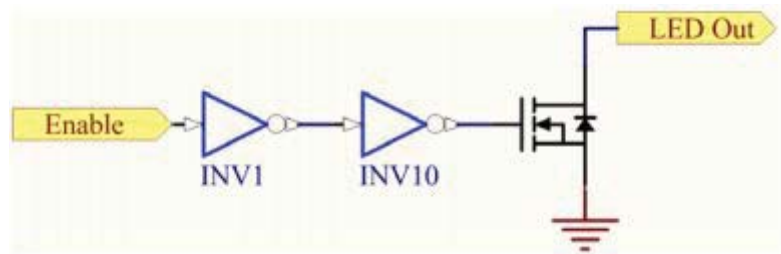
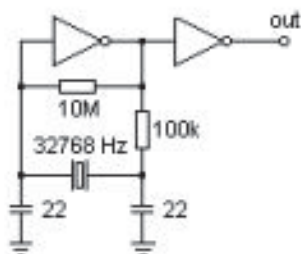
|                                       |              |
|---------------------------------------|--------------|
| JK Flip Flop(x13)                     | 104 (8 each) |
| 2-Input AND Gate(x11)                 | 33(3 each)   |
| 13-Input AND Gate                     | 14           |
| Total Cost of DIM and FLASH Functions | 153          |



The multiplexer used is made up of 4 3-Input NAND gates, two NOT gates, and one 4-Input NAND gate. Each 3-Input NAND Gate has a cost of 3, each NOT gate has a cost of 1, and the 4-Input NAND has a cost of 4.

| Gate             | Cost       |
|------------------|------------|
| 3-Input NAND(x4) | 12(3 each) |
| NOT(x2)          | 2(1 each)  |
| 4-Input NAND     | 4          |
| MUX Total Cost   | 18         |

The Clock and the LED Driver schematics were both provided for this assignment.



**CLOCK Cost:**

The clock has a total cost of 2, because each of the two NOT gates has a cost of 1.

**LED Driver Cost:**

The LED Driver has a total cost of 211, because the INV1 NOT gate has a cost of 1, the INV10 NOT gate has a cost of 10, and the Drive Transistor has a cost of 200, as stated in the assignment.

**Cost Estimation:**

| BLOCK             | COST |
|-------------------|------|
| Input Conditioner | 109  |
| State Counter     | 81   |
| On                | 0    |
| Off               | 0    |
| Flash             | 152  |
| Dim               | 1    |
| MUX               | 18   |
| LED Driver        | 211  |
| Clock             | 2    |
| TOTAL Cost        | 574  |