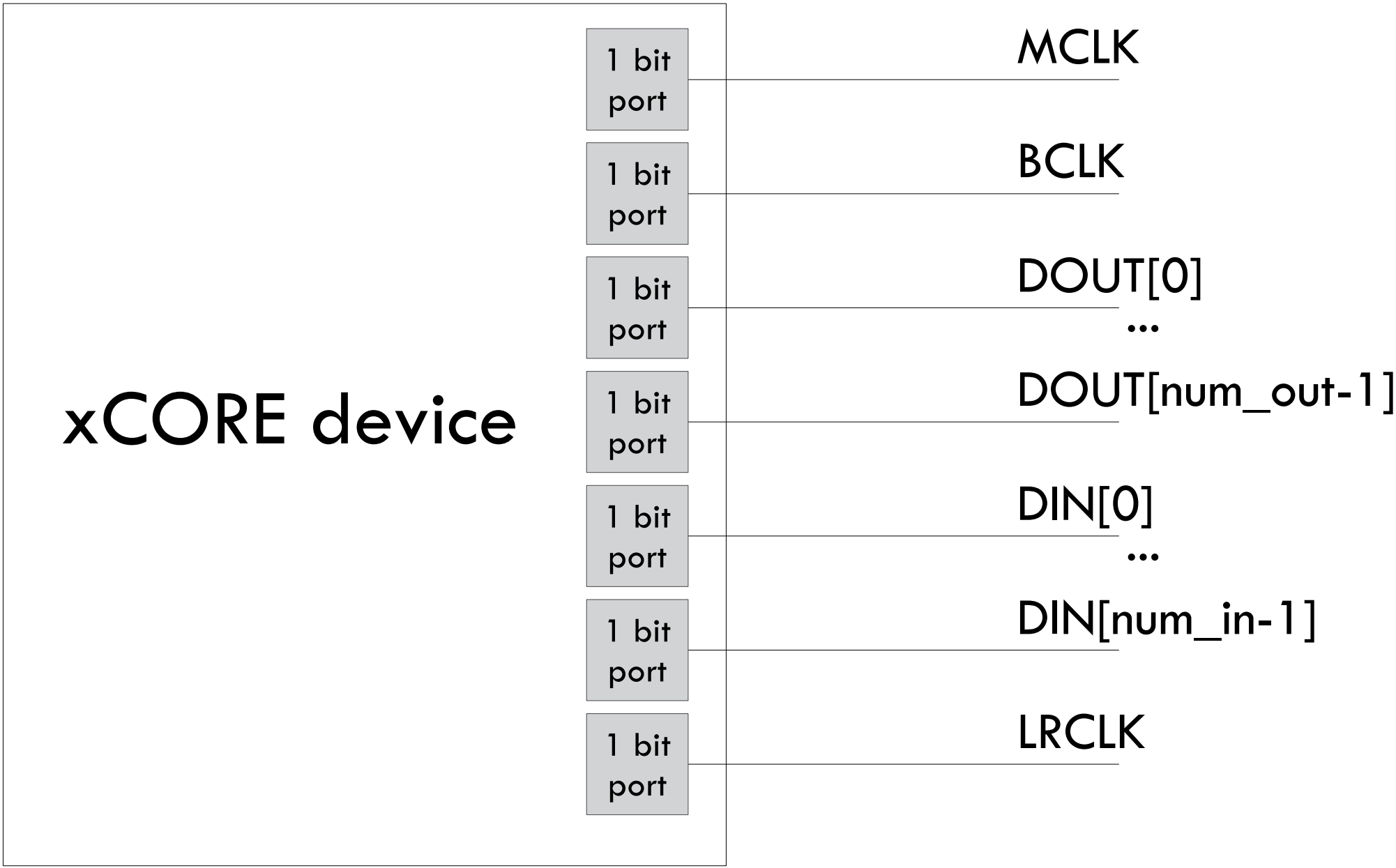
xCORE device
1 bit port
1 bit port
1 bit port
1 bit port
1 bit port
1 bit port
1 bit port
MCLK
BCLK
DOUT[0]
...
DOUT[num_out-1]
DIN[0]
...
DIN[num_in-1]
LRCLK