

xCORE device

1 bit
port

MCLK

1 bit
port

BCLK

1 bit
port

DOUT[0]

...

1 bit
port

DOUT[num_out-1]

1 bit
port

DIN[0]

...

1 bit
port

DIN[num_in-1]

1 bit
port

LRCLK