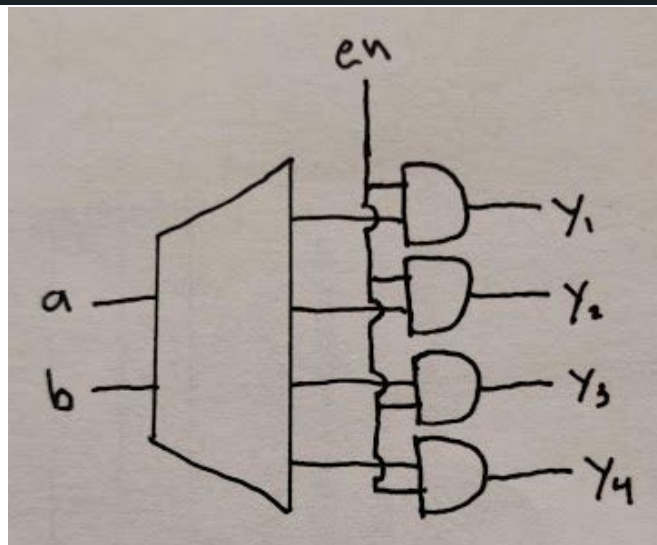# Assignment 2

Brennan McDonald - 8195614

Question 1

```vhdl
LIBRARY IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity quetsion_1 is
    port(
        a: in std_logic;
        b: in std_logic;
        en: in std_logic;
        y: out std_logic_vector(3 downto 0)
    );
end quetsion_1;
architecture arch of quetsion_1 is
begin
    op := a & b;
    case op is
        when "00"   =>  y <= "1000" and en;
        when "01"   =>  y <= "0100" and en;
        when "10"   =>  y <= "0010" and en;
        when "11"   =>  y <= "0001" and en;
    end case
end arch;
```
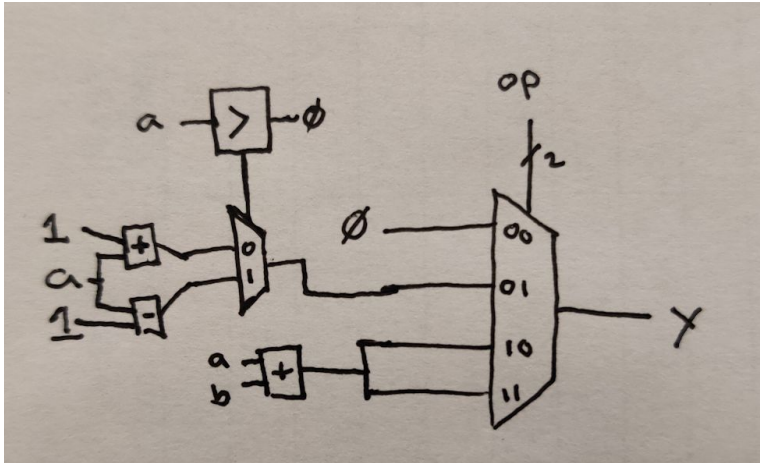
Question 2

```vhdl
LIBRARY IEEE;
use IEEE.STD_LOGIC_1164.ALL;


entity quetsion_2 is
    port(
        CTRL: in std_logic_vector(1 downto 0);
        X: in std_logic_vector(1 downto 0);
        Y: out std_logic_vector(1 downto 0)
    );
end quetsion_2;


architecture arch of quetsion_2 is
    signal temp: std_logic;
begin
    temp <= X(to_integer(unsigned(Y(0))));
    begin procedure is
        if (CTRL = "00" || CTRL = "11") {
            Y <= X(1) & temp;
        } else {
            Y <= X(0) & temp;
        }
    end procedure
end arch
```

Question 3

a)

b)

```
architecture arch of quetsion_3 is
begin
    y <= "0000" when (en = "00") else
        (a - 1) when (en = "01" and a < 0) else
        (a + 1) when (en = "01" and a >= 0) else
        (a + b)
end arch
```

Question 4

```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity question_4 is
    port(
        in: in std_logic_vector(3 downto 0);
        op: in std_logic_vector(1 downto 0)
        out: out std_logic
    );
end question_4;

architecture question_4_estr of question_4 is
begin
    case op is
        when "00" =>
            out <= in(0);
        when "01" =>
            out <= in(1);
        when "10" =>
            out <= in(2);
        when "11" =>
            out <= in(3);
    end case;
end question_4_estr;
```