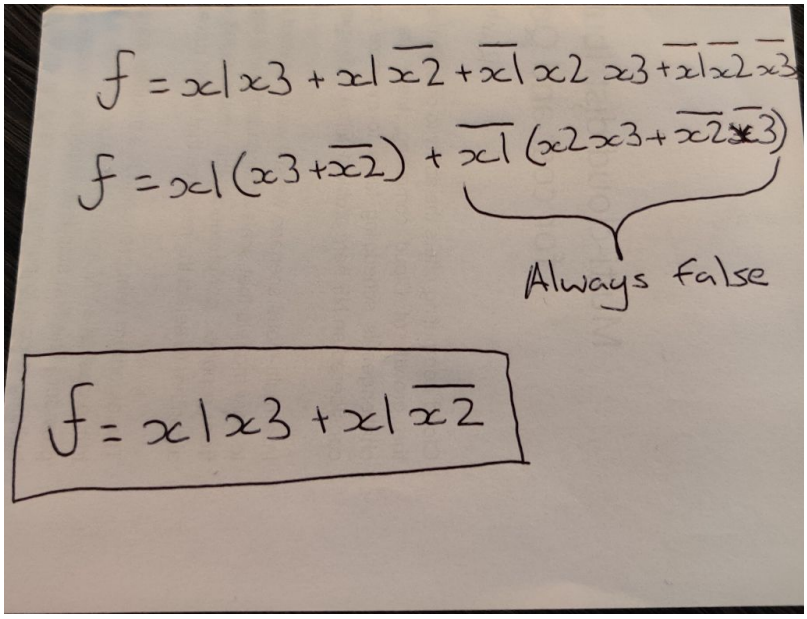
Assignment 1

Question 1

Question 2



Question 3

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity multiplexer is
  port (
    a  : in std_logic;
    b  : in std_logic;
    en : in std_logic;
    x : out std_logic_vector(3 downto 0)
    );
end multiplexer;

architecture output of multiplexer is
begin
    x(0) <= 1 when (not a) and (not b) and en else
    x(1)<= 1 when (not a) and b and en else
    x(2) <= 1 when a and (not b) and en else
    x(3) <= 1 when a and b and en else
    x <= "0000";
end output;
```

Question 4

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity comparator is
port (
      a: in std_logic_vector(7 downto 0);
      b: in std_logic_vector(7 downto 0);
      agtb: out std_logic
 );
end comparator;

architecture output of comparator is
    signal agtb: std_logic_vector(7 downto 0);
    signal Result: std_logic;
begin
    AB(0) <= a(0) and b(0)
    AB(1) <= a(1) and b(1)
    AB(2) <= a(2) and b(2)
    AB(3) <= a(3) and b(3)
    AB(4) <= a(4) and b(4)
    AB(5) <= a(5) and b(5)
    AB(6) <= a(6) and b(6)
    AB(7) <= a(7) and b(7)
    agtb <= 1 when AB = "11111111" else 0 ;
end output;
```

Question 5

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity LED_SWITCH is
port (
      PB: in std_logic;
      LED: out std_logic(3 downto 0)
 );
end LED_SWITCH;

architecture output of LED_SWITCH is
begin
    if PB = 1 then
        LED(0) <= 1
        LED(1) <= 0
        LED(2) <= 1
        LED(3) <= 0
    else
        LED(0) <= 0
        LED(1) <= 1
        LED(2) <= 0
        LED(3) <= 1
    end if;
end output;
```