Lab 1: Logic Gates

ITI 1100 C - Digital Systems

Winter 2016

School of Electrical Engineering and Computer Science

University of Ottawa

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Group # L2 Friday 31

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Experiment Date: Friday February 5th, 2016

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Objectives

- Construct simple combinational logic circuits from a schematic.
- Experimentally determine the functional operation of simple combinational logic circuits.
- Identify equivalent logic gates to those produced by various circuit configurations from the resulting truth table.
- Connect various gates together to create simple logic functions.
- Analyse combinational logic circuits and predict their operation.
- Construct and test more complex combinational logic circuits.

Equipment & Components

- Quartus II 13.0 Service-Pack 1
- Altera DE2-115 card

Circuit Diagrams

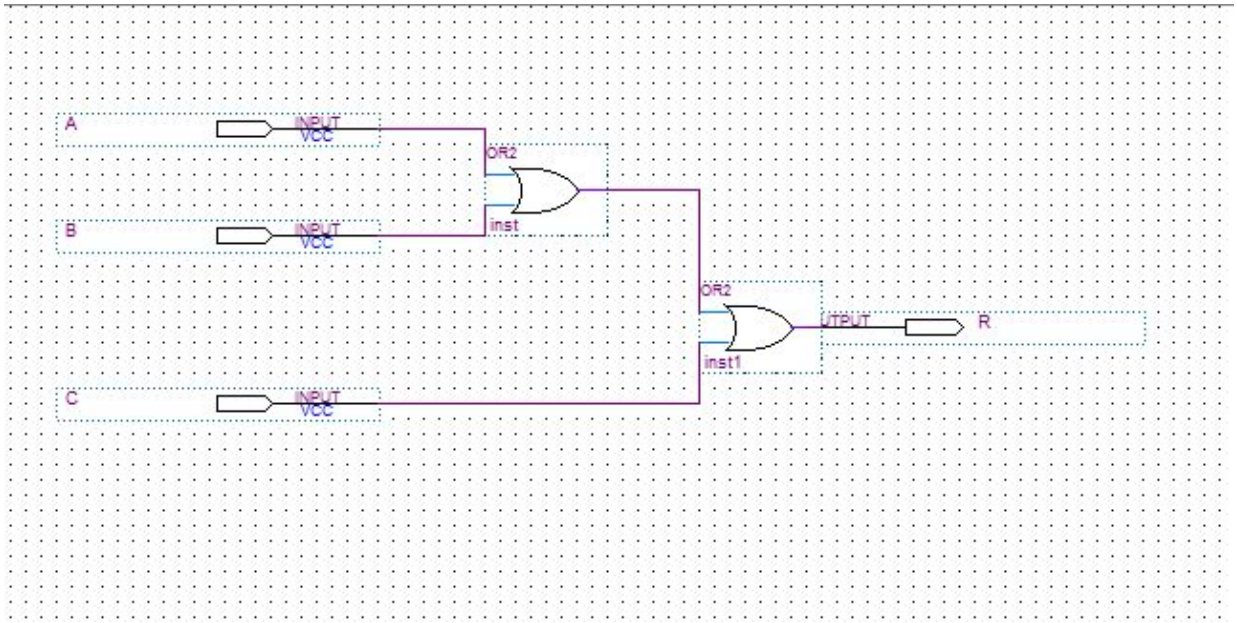
Include screen-shots of schematic design diagrams which shows all gates and other components with pin names clearly

Clearly specify to which part or section the figure is belong to, by following same title/sub-title structure used in lab manual.

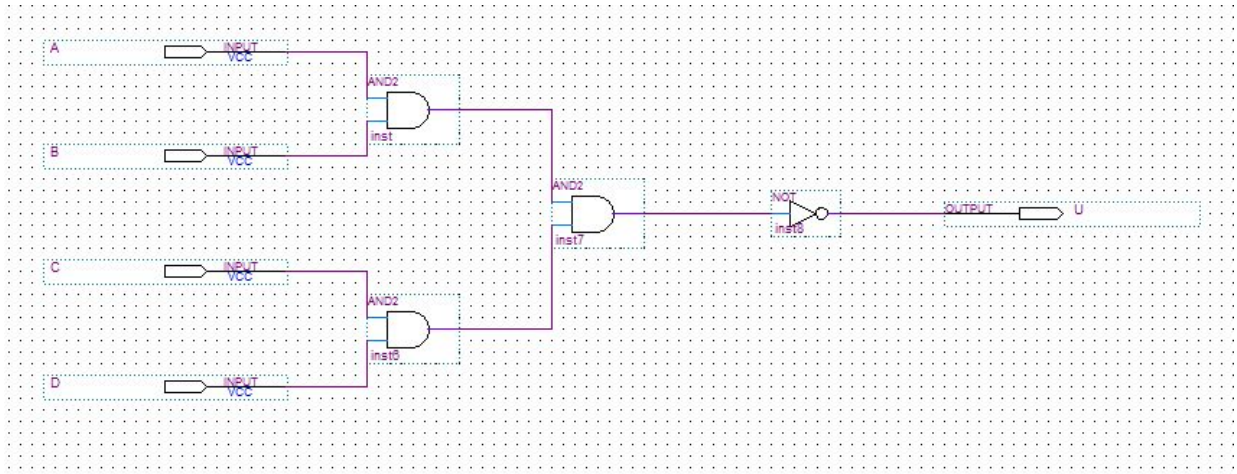
Clearly Name and number Circuit Diagrams

Example:

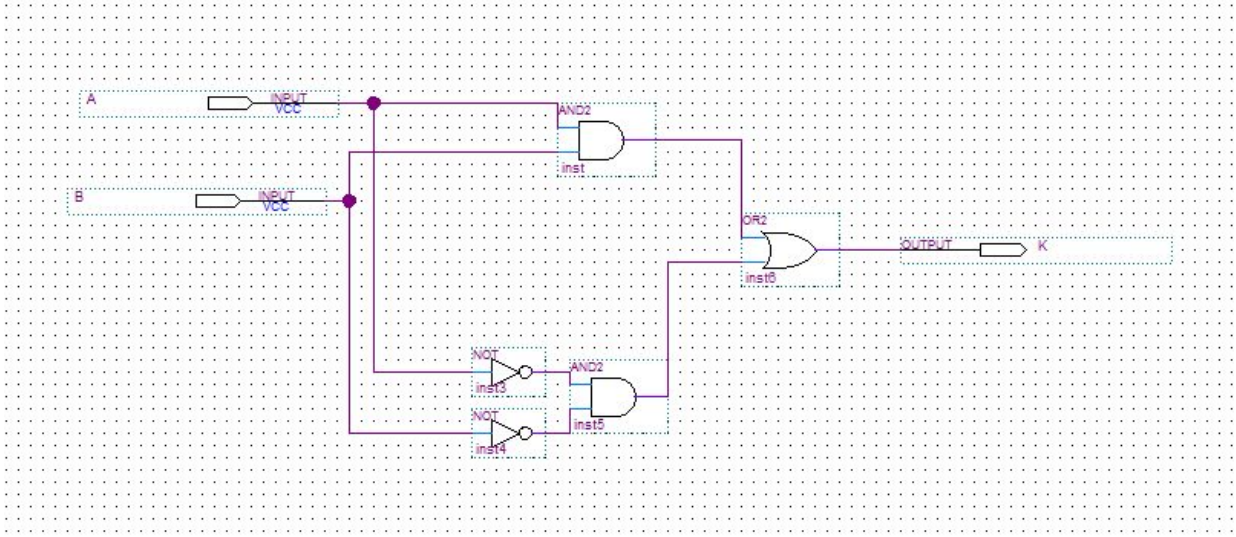
Part I – Combinational Logic Circuits Construction



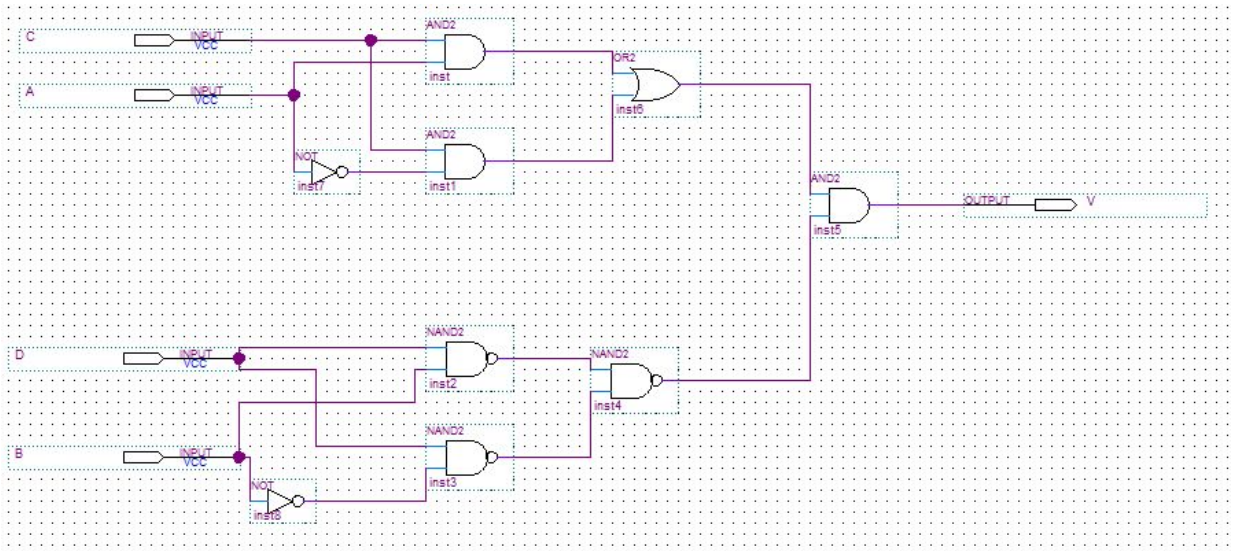
One-Chip Logic Circuit (Figure 5.1.1 from manual)



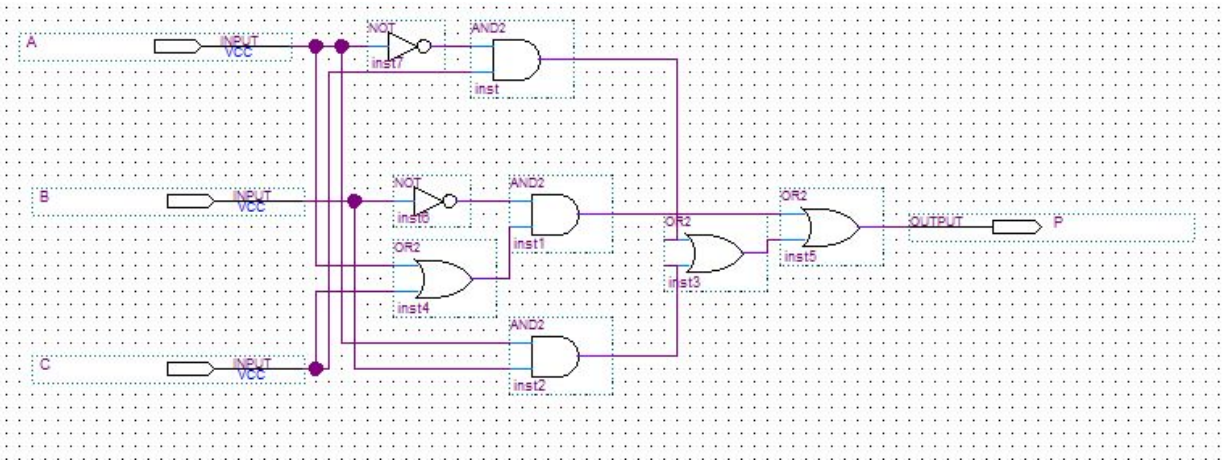
Two-Chip Logic Circuit (Figure 5.1.2 from manual)



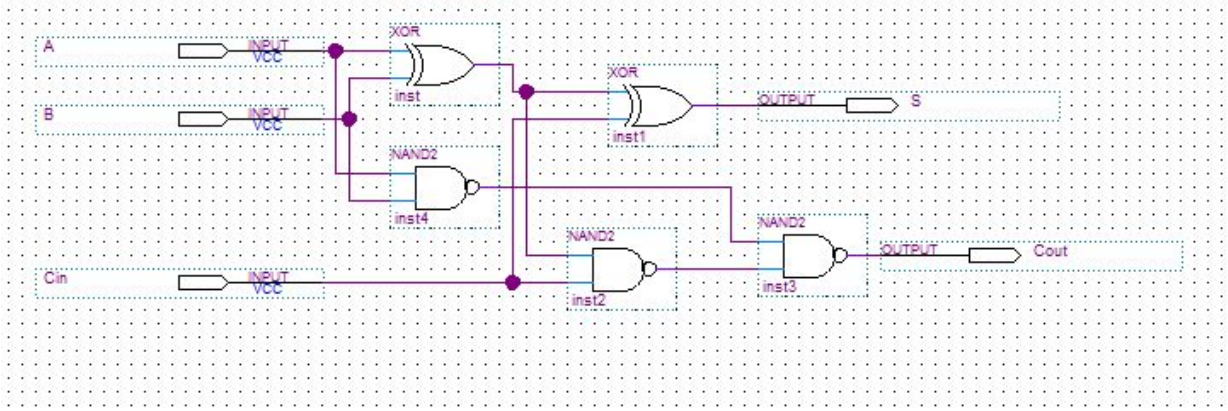
Three-Chip Logic Circuit (Figure 5.1.3 from manual)



AND Circuit (Figure 5.1.6 from manual)



OR Circuit (Figure 5.1.7 from manual)



Multiple Output Circuit (Figure 5.1.8 from manual)

Experimental Data and Data Processing

Part I – Combinational Logic Circuits Construction

One Chip Logic Circuit

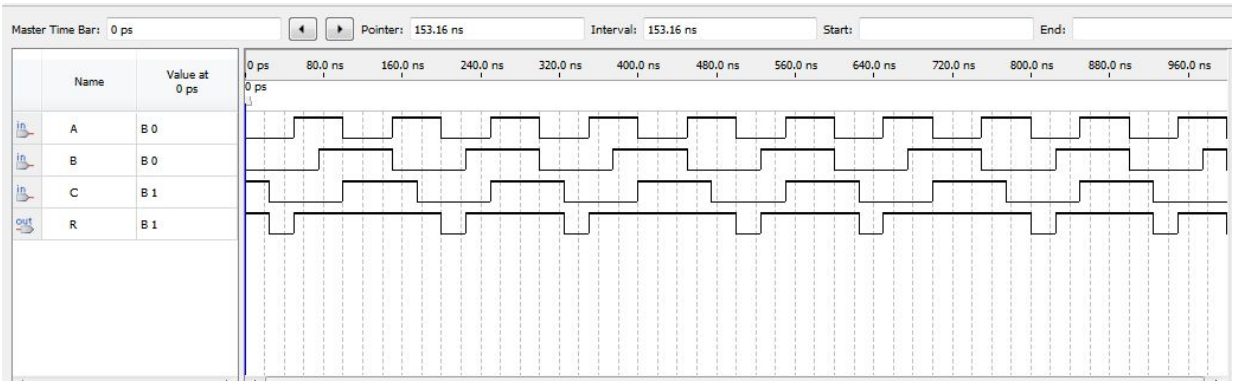


Figure 2 : Simulation output waveform of one chip circuit

Table 1 : Experimental data observed from MAX 7000 circuit board**

A	B	C	R
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Two Chip Logic Circuit

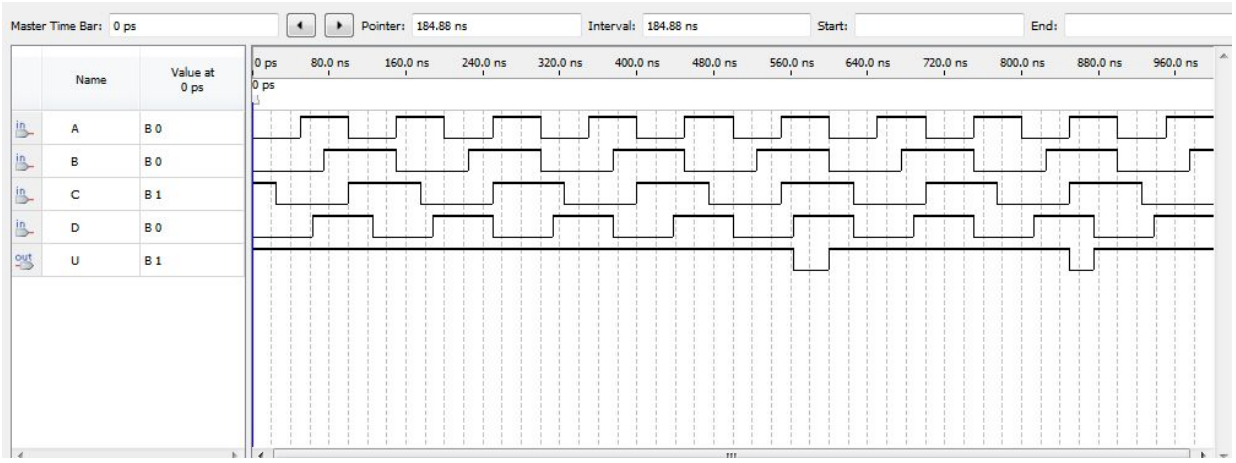


Figure 3 : Simulation output waveform of two chip circuit

Table 2 : Experimental data observed from MAX 7000 circuit board

A	B	C	D	U
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Three Chip Logic Circuit

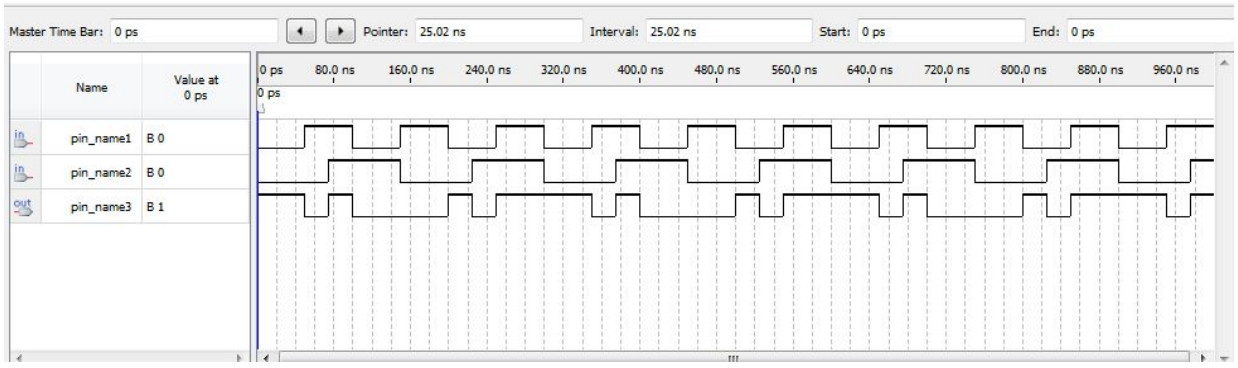


Figure 4 : Simulation output waveform of three chip circuit

Table 3 : Experimental data observed from MAX 7000 circuit board

A	B	K
0	0	1
0	1	0
1	0	0
1	1	1

Part II – Combinational Logic Circuits Analysis

AND Circuit

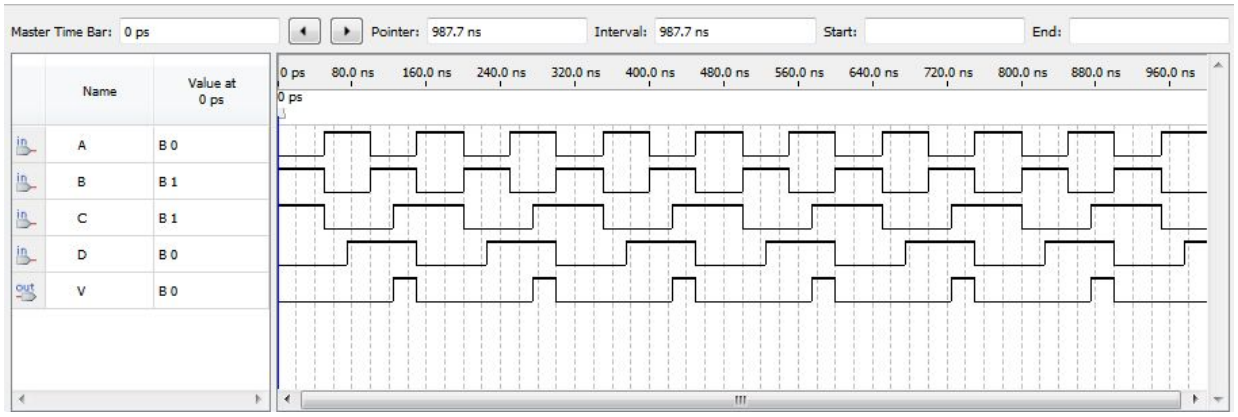


Figure 5 : Simulation output waveform of AND circuit

Table 4 : Experimental data observed from MAX 7000 circuit board

A	B	C	D	V
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

OR Circuit

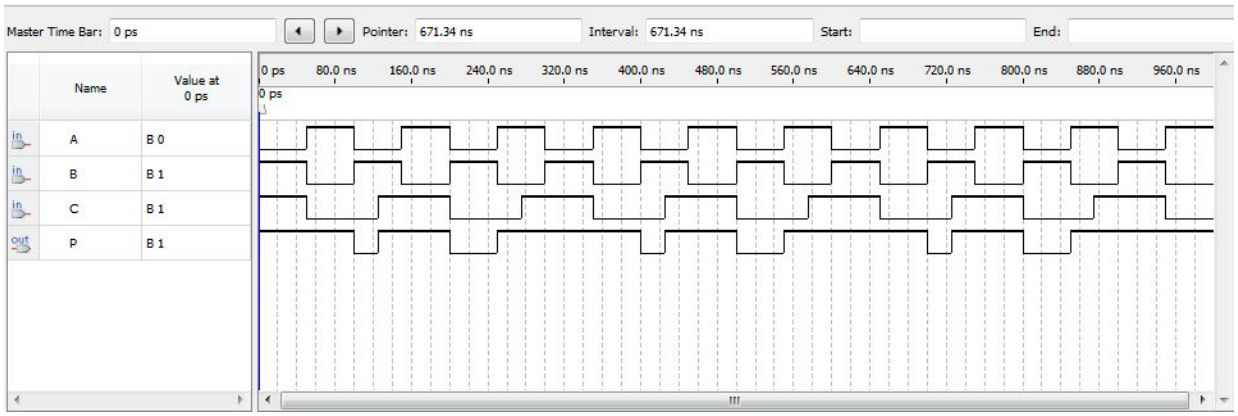


Figure 6 : Simulation output waveform of OR circuit

Table 5 : Experimental data observed from MAX 7000 circuit board

A	B	C	P
0	0	0	0

0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Multiple Output Circuit

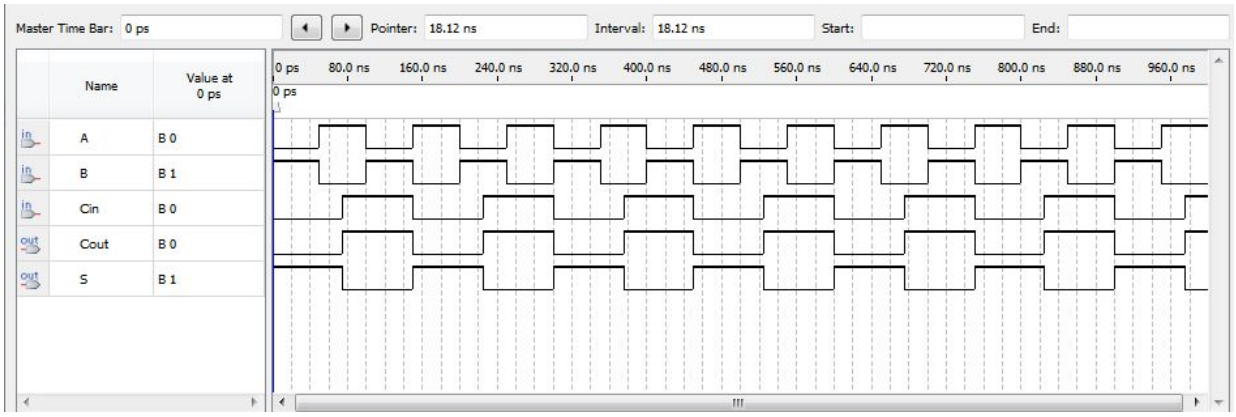


Figure 7 : Simulation output waveform of Multiple Output circuit

Table 6 : Experimental data observed from MAX 7000 circuit board

A	B	C	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Comparison of Theoretical Data and Experimental Data

Part I – Combinational Logic Circuits Construction

One Chip Logic Circuit

Table 1 : Experimental data observed from MAX 7000 circuit board**

A	B	C	Theoretical R	Actual R
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

Two Chip Logic Circuit

Table 2 : Experimental data observed from MAX 7000 circuit board

A	B	C	D	Theoretical U	Actual U
0	0	0	0	1	1
0	0	0	1	1	1
0	0	1	0	1	1
0	0	1	1	1	1
0	1	0	0	1	1
0	1	0	1	1	1
0	1	1	0	1	1
0	1	1	1	1	1
1	0	0	0	1	1
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	1	1

1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	0	0

Three Chip Logic Circuit

Table 3 : Experimental data observed from MAX 7000 circuit board

A	B	Theoretical K	Actual K
0	0	1	1
0	1	0	0
1	0	0	0
1	1	1	1

Part II – Combinational Logic Circuits Analysis

AND Circuit

Table 4 : Experimental data observed from MAX 7000 circuit board

A	B	C	D	Theoretical V	Actual V
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	0	0
1	0	1	1	0	0
1	1	0	0	0	0

1	1	0	1	0	0
1	1	1	0	1	1
1	1	1	1	1	1

OR Circuit

Table 5 : Experimental data observed from MAX 7000 circuit board

A	B	C	Theoretical P	Actual P
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

Multiple Output Circuit

Table 6 : Experimental data observed from MAX 7000 circuit board

A	B	C	Theoretical S	Theoretical C_o	Actual S	Actual C_o
0	0	0	0	0	0	0
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	1	0	1
1	1	0	0	1	0	1
1	1	1	1	1	1	1

Discussion & Conclusions

The objective of this lab was to observe logic gates when they are combined into a circuit. These circuits took inputs and provided useable outputs that had been logically manipulated. Our data that we found matched all of the expected data calculated from the prelab.