CEG2136 Lab 1

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Introduction

This lab was provided to familiarize students with the Altera FPGA board who previously didn't know how to use it. For those students who already knew how to work the board this lab provided practice on the software. Problems provided in this lab were designing a circuit, running a simulation and programming the board. The specific problem provided in this lab was to model a basic circuit in the Quartus software, simulate it and upload it to the board. This circuit consisted of a NAND, NOR and AND gate arranged so the NAND and NOR's output are sent through an AND gate to the output. The algorithm used to solve this problem as provided by the lab manual. The algorithm provided a series of steps to successfully using the Quartus software.

Design

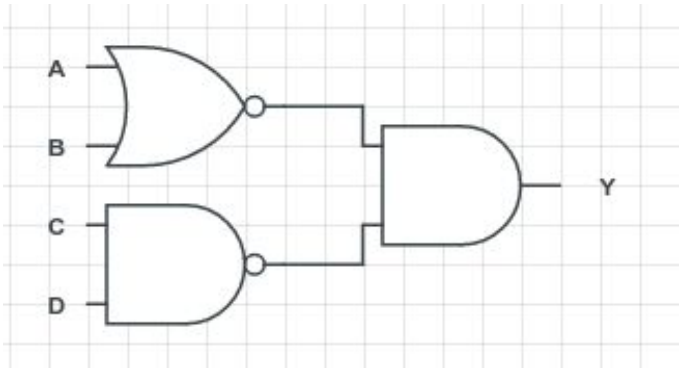

Fig. 1. Circuit Diagram.

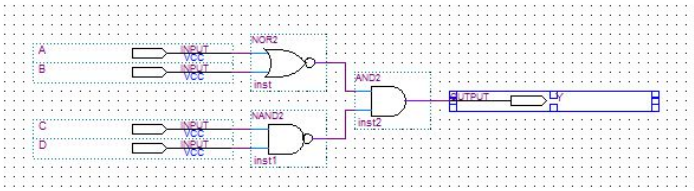

Fig. 2. Block Diagram

AB\CD	00	01	11	10
00	1	1	0	1
01	0	0	0	0
11	0	0	0	0
10	0	0	0	0

Fig. 3. Karnaugh Map

A	B	C	D	out
0	0	0	0	1
1	0	0	0	0
0	1	0	0	0
1	1	0	0	0
0	0	1	0	1
1	0	1	0	0
0	1	1	0	0
1	1	1	0	0
0	0	0	1	1
1	0	0	1	0
0	1	0	1	0
1	1	0	1	0
0	0	1	1	0
1	0	1	1	0
0	1	1	1	0
1	1	1	1	0

Simulation and Verification

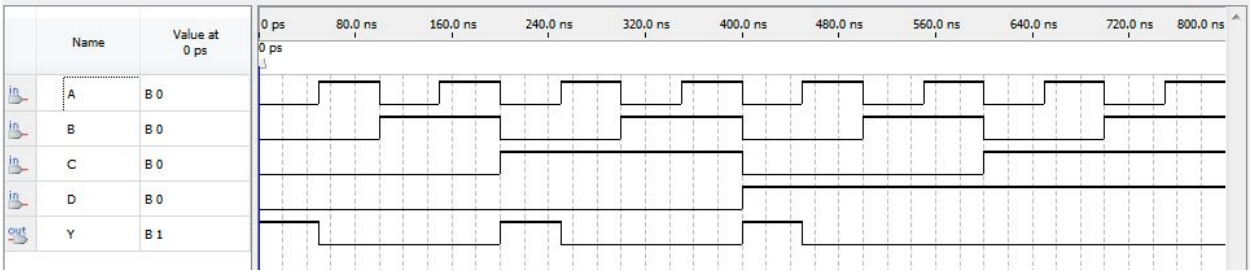

Fig. 4. Waveform Diagram with A as the least significant bit

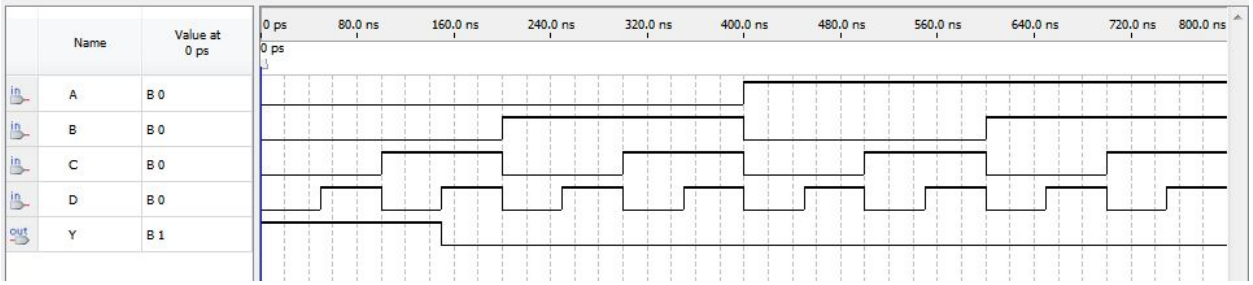

Fig. 4. Waveform Diagram with A as the most significant bit

Discussion

This lab provided a good review of the Altera board and Quartus software. I encountered 2 issues when working on this lab, mainly the fact that I did not remember how to perform the wave simulation. Due to me forgetting to switch the simulation to “Quartus II”, my simulation kept failing due to an unknown error. After switching to the proper simulator my simulation worked.

Prelab

2 $(\overline{A+B})(\overline{CD})$

3

NAND:

A	B	out
0	0	1
0	1	1
1	0	1
1	1	0

NOR:

A	B	out
0	0	1
0	1	0
1	0	0
1	1	1

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A	B	C	D	out
0	0	0	0	1
1	0	0	0	0
0	1	0	0	0
1	1	0	0	0
0	0	1	0	1
1	0	1	0	0
0	1	1	0	0
1	1	1	0	0
0	0	0	1	1
1	0	0	1	0
0	1	0	1	0
1	1	0	1	0
0	0	1	1	0
1	0	1	1	0
0	1	1	1	0
1	1	1	1	0