DIGITAL SYSTEMS II

LAB 4 REPORT

1st student name: Brennan McDonald. ID: 8195614.

2nd student name: Akif Manzoor. ID: 8298086

The Lab's date: November 4th

CHAPTER 6 (Sequential Circuits)

6.1) Circuit Description

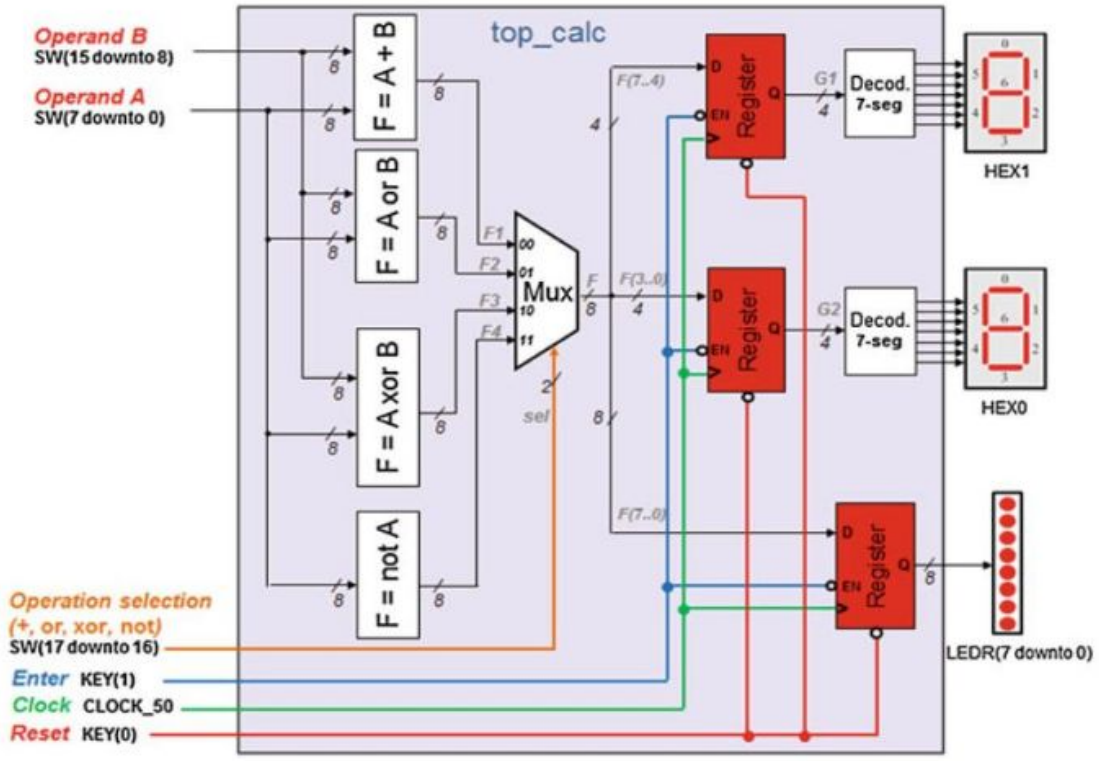

Fig. 6.14 Inserting registers in the calculator to store operation results

SW	Y	HEX0	HEX1	LEDR
00 00000010 00000001	0001	0110000	1000000	000000000000000011
11 00000010 00000001	0001	0000110	0001110	000000000011111110
10 00000010 00001001	0001	0000011	1000000	000000000000001011
00 00001010	0001	0001110	1000000	000000000000001111

00000101				
01 00000010 00000011	0001	0000011	1000000	000000000000000011

CHAPTER 7 (Finite State Machines)

7.1) Circuit Description

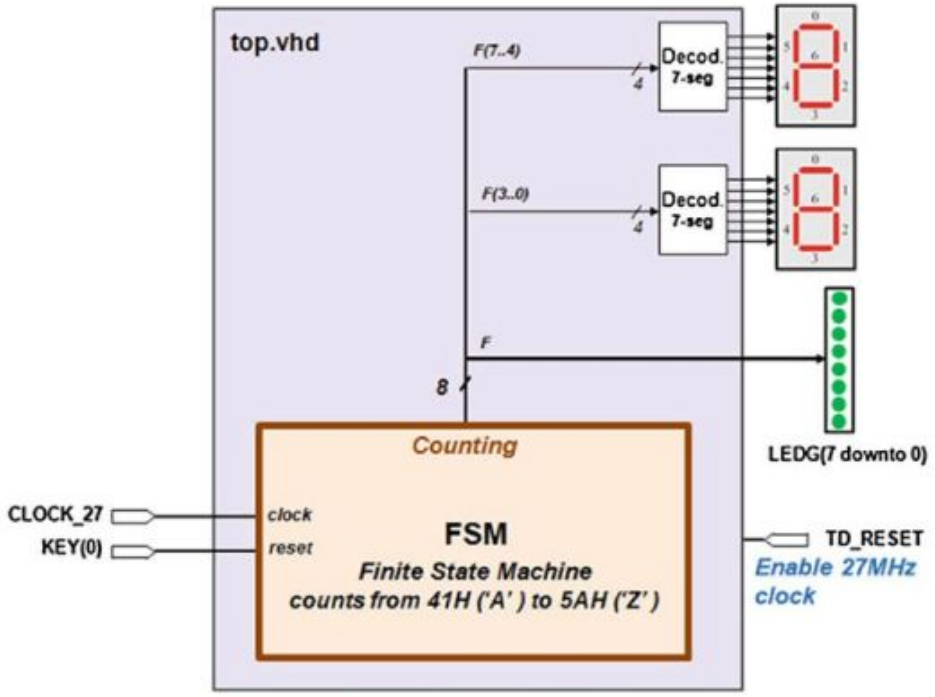

Fig. 7.11 'A' to 'Z' ASCII counter block diagram

50Mhz clock = 50 million cycles per second
= 5 million cycles per ms
= 5.0*10^6 * 5 ms
= 25.0*10^6

= 17D7840