Digital Systems II - DGD 1

ALU: Arithmetic Logic Unit
Memory System: Storage

Combinational Logic

Only the circuits that do logic, there is no state of the circuit. The chip takes the inputs and gives an output

Sequential Logic

Has memory, stateful circuit. There is a history of previous results and can be modelled using a FSM (Finite state machine)

IEEE1164 Standard

Formerly ulogic was used and was represented by 1s and 0s

IEEE1164 is a multi level standard which now maps to multiple types. (Weak zero, weak one, DNC). There is a package available for using this ‘std_logic_1164’

Examples:

Strong 0/1, means inputs are connected directly to Vcc +5v or Ground
Weak 0/1, Means there is a passive component between the Vcc/Ground and the input. The input isn't exactly +5V but it is close.

A) 0000 0110 + 0000 1101 = 0001 0011
B) = 1111 1010 - 1111 0011
   = 1111 1010 + 0000 1101
   = 0000 0111
C) 1100 - 1010
   1100 + 0110 = 1 0010
   = 0010 = 2
D) 1000 + 1110
   1 0110, this isnt the right answer, we underflowed
   -10 can not be represented in a 2s complement signed 4 bit integer.

x1’*x2’*x3’ + x1’x2x3 + x1x2’x3 + x1x2x3’

Using a kmap